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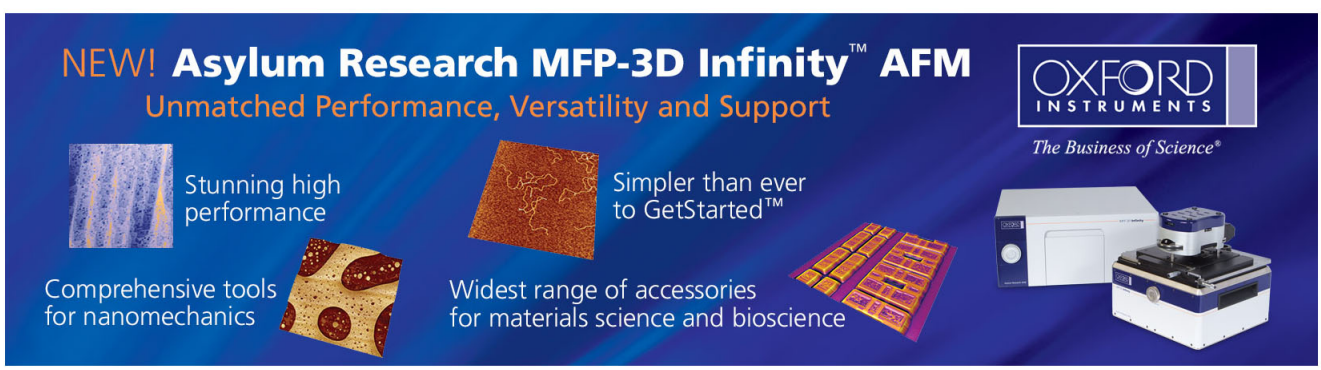

# Temperature-dependent characteristics of junctionless bulk transistor

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The temperature-dependent performance, including drain current ($I_d$) and gate capacitance ($C_{gg}$) of multi-gate junctionless (JL) bulk transistor for temperature (T) ranging from 150 K to 500 K, was investigated using 3D thermodynamic quantum-corrected device simulation. The combination effect of impurity scattering and phonon scattering is observed owing to the different temperature-dependent of mobility at low and high temperature. Since the $C_{gg}$ of the JL device consists of a series combination of oxide capacitance ($C_{ox}$) and semiconductor channel capacitance ($C_S$) due to bulk conduction of the current, the $C_{gg}$ at on-state ($V_g = 1$ V) shows much sensitive to the temperature than a conventional inversion-mode transistor.
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Silicon-based devices are being continuously scaled down to increase density and speed. Short channel metal-oxide-semiconductor field-effect-transistors (MOSFET) face various challenges, such as leakage currents and the short-channel effect (SCE) because gate controllability declines over the channel.[1–3] SCE and drain-induced barrier lowering (DIBL), which cause source and drain junctions to be highly confined, are challenges to doping techniques and thermal budget. The ultra-shallow junction is indispensable in the design of devices as they shrink further.[3] Recently, the concept of the junctionless (JL) nanowire transistor, which contains a single doping species at the same level in the source, drain, and channel, has been investigated.[4–14] JL devices provide such advantages as improved SCE control, favorable subthreshold swing, and simpler fabrication processes. Additionally, a multi-gate JL transistor with a bulk substrate, which does not require an SOI wafer, has a lower cost and is fully compatible with the industry standard bulk CMOS process flow, has also been proposed.[8] To ensure the stability of circuit with JL bulk transistor operating at extreme high/low temperature, it is important to evaluate the temperature characteristics of such device. This work studies the n-type multi-gate JL bulk transistor performance, including the on-current ($I_{on}$), threshold voltage ($V_{th}$), and the gate capacitance ($C_{gg}$) with respect to different temperature by using 3D thermodynamic quantum-corrected device simulation.

Figure 1 presents the structure of the simulated devices and the relevant parameters. The device has an $HfO_2$ high-k gate oxide with an equivalent oxide thickness (EOT) of 1 nm, a gate length ($L_g$) of 15 nm, and a Fin height (H) of 10 nm. The gate material is TiN with a work-function of 4.76 eV,[15] which the linear threshold voltage ($V_{th}$) is adjusted to about 300 mV. The doping concentrations in the source/drain/channel are all set to $1.5\times10^{19}\text{cm}^{-3}$. The substrate doping is opposite type with $5\times10^{18}\text{cm}^{-3}$, which can be obtained easily by the typical well implantation process. To discuss the difference of physics between JL and conventional inversion-mode (IM) MOSFET, the multi-gate IM bulk transistor with the same geometry are obtained and compared. The design of multi-gate IM bulk transistor is based on the prediction of International Technology Roadmap for Semiconductors (ITRS) 2011, in which the source/drain doping concentrations are constant with $1\times10^{20}\,\text{cm}^{-3}$, the channel doping is opposite type with $1\times10^{15}\,\text{cm}^{-3}$, and the well doping with opposite type $5\times10^{18}\,\text{cm}^{-3}$ is used, as listed in Fig. 1. To obtain accurate numerical results for a nanometer-scale device, the device is performed by 3D quantum-corrected simulation using the commercial tool, Synopsys Sentaurus Device.[16] In the quantum-corrected simulation, a density gradient model is used. The bandgap narrowing model, the band-to-band tunneling model, and Shockley-Read-Hall recombination with the doping dependent model are also considered. To analyze the performance in different temperature (T), the thermodynamic model is used. In this model, the relations of Poisson equation and electron/hole continuity equations are generalized to include the temperature gradient as a driving term,

$$\begin{aligned}\vec{J}_n &= -nq\mu_n\,(\nabla\Phi_n + P_n\nabla T),\\ \vec{J}_p &= -pq\mu_p(\nabla\Phi_p + P_p\nabla T),\end{aligned} \tag{1}$$

where $\Phi_n$ and $\Phi_p$ are quasi-Fermi potentials and $P_n$ and $P_p$ are thermoelectric powers, for electron and hole, respectively. The mobility model used in device simulation is according to Mathiessen's rule, expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{imp}}, \tag{2}$$

where D = exp(x/l_crit), x is the distance from the interface, and l_crit is a fitting parameter. The mobility consists of four parts: surface acoustic phonon scattering ($\mu_{surf\_aps}$), surface roughness scattering ($\mu_{surf\_rs}$), bulk phonon scattering ($\mu_{bulk}$), and impurity scattering ($\mu_{imp}$). The mobility change with impurity scattering is based on continuous doping concentration using Masetti model,

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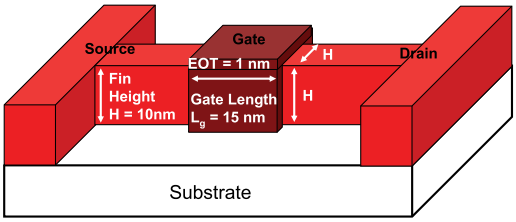



| Device Structure | N-type JL Bulk Transistor | N-type IM Bulk Transistor |
|---|---|---|
| Gate Workfunction | 4.76eV | 4.44eV |
| Source/Drain Doping Concentration | $1.5\times10^{19}cm^{-3}$ N-type | $1\times10^{20}cm^{-3}$ N-type |
| Channel Doping Concentration | $1.5\times10^{19}cm^{-3}$ N-type | $1\times10^{15}cm^{-3}$ P-type |
| Substrate Doping Concentration | $5\times10^{18}cm^{-3}$ P-type | $5\times10^{18}cm^{-3}$ P-type |

FIG. 1. The device structure and parameters of simulated n-type multi-gate junctionless (JL) bulk and inversion-mode (IM) bulk transistors.

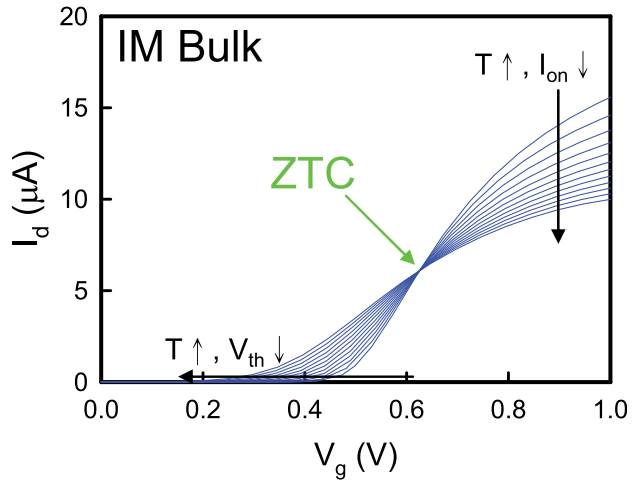
$$\mu_{imp} = \mu_{\min 1}\exp\left(-\frac{P_c}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{const}-\mu_{\min 2}}{1+((N_{A,0}+N_{D,0})/C_r)^{\alpha}} - \frac{\mu_1}{1+(C_s/(N_{A,0}+N_{D,0}))^{\beta}}, \quad (3)$$

where $\mu_{min1}$, $\mu_{min2}$, $\mu_1$, $P_c$, $C_r$, $C_s$, $\alpha$, and $\beta$ are accessible parameters. Additionally, the incomplete ionization is also considered to accurately obtain the device performance at low temperature, the ionized impurity atoms are given by

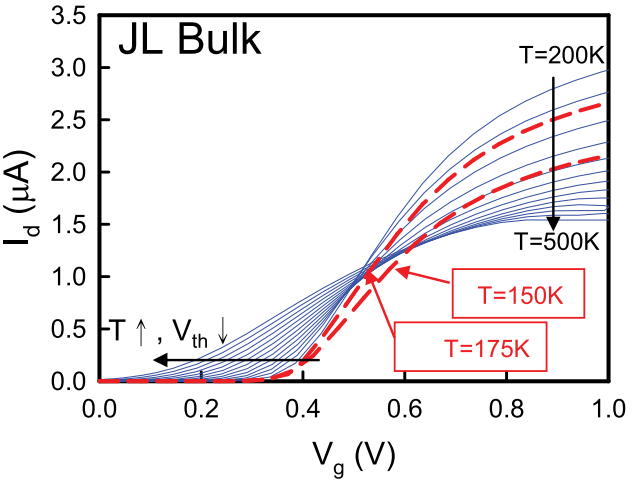
$$N_D = \frac{N_{D,0}}{1+g_D\exp(\frac{E_{F,n}-E_D}{kT})}, \quad N_A = \frac{N_{A,0}}{1+g_A\exp(\frac{E_A-E_{F,p}}{kT})}, \quad (4)$$

where $N_{D,0}$ and $N_{A,0}$ are the substitutional donor and acceptor concentrations, $g_D$ and $g_A$ are the degeneracy factors for the impurity levels, and $E_D$ and $E_A$ are the ionization energies. The details of these models and their parameters are described in Ref. 16.

Figure 2 plots the drain current ($I_d$) as a function of gate voltage ($V_g$) at drain voltage ($V_d$) 0.05 V for temperature (T) ranging from 150 K to 500 K in IM and JL bulk transistors. In IM device, the $V_{th}$ decreases and the off-current increases as T are increased. The on-current ($I_{on}$, at $V_g = 1$ V) decreases as the T increases due to mobility degradation by severe phonon scattering at high temperature. The decrease of $V_{th}$ with temperature tends to increase $I_d$, and the reduction of mobility with temperature tends to decrease $I_d$, there exists a $V_g$ which compensate these effects, called the zero-temperature-coefficient (ZTC) point.[11–14,17,18] In JL bulk transistor, since the studied device is made on heavily doped bulk substrate, the results are different from the temperature dependency proposed in literature.[11–14] When T is larger than 200 K, as T increases, the $I_{on}$ decrease. The ZTC point is observed, which is similar to that in the IM device. However, if we compare the $I_d$-$V_g$ curves of T = 150 K, 175 K, and 200 K, the $I_{on}$ monotonically increases with T, there is no ZTC point in this temperature range. To understand the reason of the results, the effective mobility ($\mu_{eff}$) for different T is extracted,[19] and the extracted mobility is about 90 $cm^2$/Vs at T = 300 K, which are confirmed with experimental mobility data,[10] as shown in Fig. 3(a). Usually, the value of mobility is dominated by the phonon scattering,




(a)




(b)

FIG. 2. The drain current ($I_d$) as a function of gate bias at $V_d = 0.05$ V in (a) IM bulk transistor and (b) JL bulk transistor.

impurity scattering, and surface roughness scattering.[1–3] However, since the current in JL device exhibits bulk conduction, the third term is diminished.[4–9] Mobility varies with $T^{-3/2}$ if it is limited by phonon scattering and $T^{3/2}$ if it is limited by impurity scattering. In Fig. 3(a), the combined effect of impurity scattering and phonon scattering is obviously observed owing to the heavily doped channel in the proposed JL bulk transistor, and the peak value of $\mu_{eff}$ is located at T = 200 K. Since the sensitivity of $V_{th}$ (defined as the gate voltage at drain current $I_d = W/L\times10^{-7}A = 2\times10^{-7}A$) with T perform similarly in JL and IM bulk transistors, as displayed in Fig. 3(b), the origin of the absence of ZTC in JL bulk transistor is thus determined by the scattering phenomenon in the device. Figure 4 presents total gate capacitances ($C_{gg}$) for various gate biases at $V_d = 0.05$ V in both IM and JL bulk transistors. In JL bulk transistor at low gate bias, the device operates at depletion region, the $C_{gg}$ is dominated by the depletion capacitance ($C_{dep}$). The increase of T reduces the surface potential ($\phi_S$) and increases $C_{dep}$, this trend is similar to that in IM MOSFET.[1,16,17] On the other hand, when the device operate at high $V_g$, the $C_{gg}$ of an IM device is usually determined by the gate oxide capacitance ($C_{ox}$),

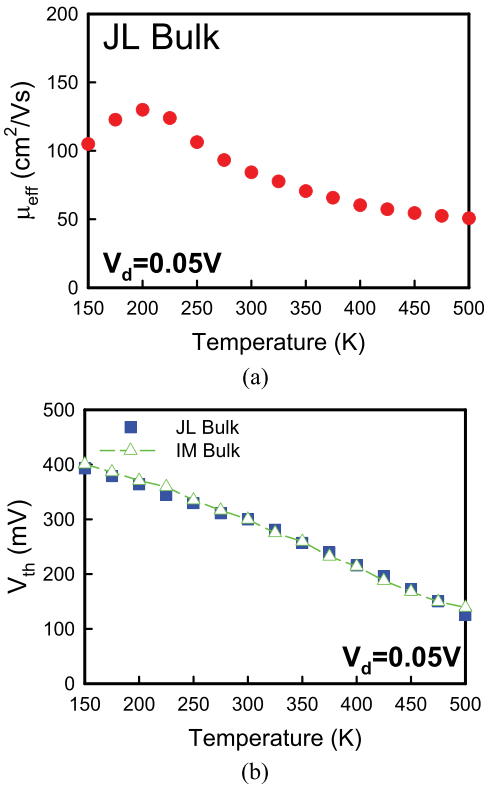



FIG. 3. (a) The effective mobility ($\mu_{eff}$) of JL bulk transistor for different temperature at $V_d = 0.05$ V. (b) The threshold voltage ($V_{th}$) of JL and IM bulk transistors as a function of temperature at $V_d = 0.05$ V.

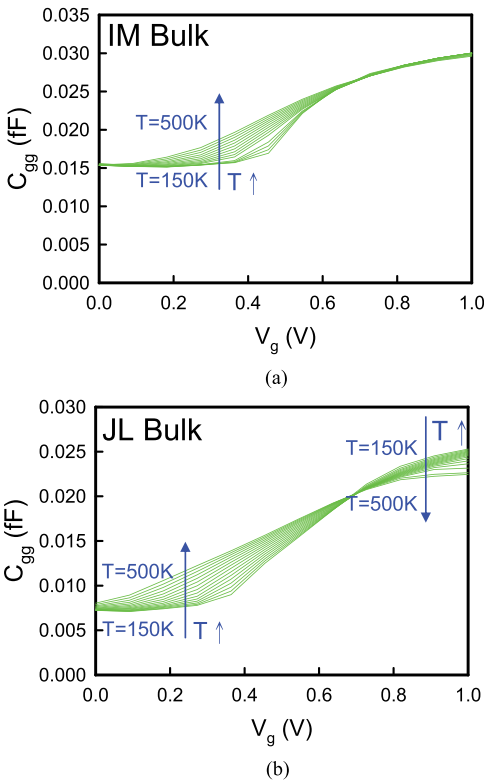



FIG. 4. The total gate capacitance ($C_{gg}$) as a function of gate bias at $V_d = 0.05$ V in (a) IM bulk transistor and (b) JL bulk transistor.

which shows less sensitive to the temperature. However, the $C_{gg}$ of the JL device consists of a series combination of $C_{ox}$ and semiconductor channel capacitance ($C_S$) because of the bulk conduction of the current.[9] Since the $\phi_S$ of a JL device operate at on-state is near flat-band condition, in which the $C_S$ can be described by[1]

$$C_S = \sqrt{qN_{ch}\frac{q}{kT}\varepsilon_S}, \tag{5}$$

where q is the elementary charge, k is the Boltzmann constant, $N_{ch}$ is the channel doping concentration, and $\varepsilon_S$ is the dielectric constant of silicon. As T increases, the $C_S$ is decreased because it is inversely proportional to the square root of T, resulting in the decrease of the $C_{gg}$. Therefore, the $C_{gg}$ at $V_g = 1$ V shows higher sensitivity to T than an IM device. To reduce such unfavorable property, we have to diminish the $C_S$ part in $C_{gg}$, the increase of $N_{ch}$ or accumulation-mode operation[10,11] are suggested.

This work studies the temperature-dependent performance of JL bulk transistor at the range of temperature from 150 K to 500 K. Owing to the high channel doping concentration is used in the proposed JL bulk transistor, the impurity scattering dominates at low temperature, thus the absence of ZTC point is observed. The $C_{gg}$ operate at on-state in JL bulk transistor is more sensitive to the temperature than an IM bulk transistor because of the $C_S$ at flat-band condition is a function of temperature.

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