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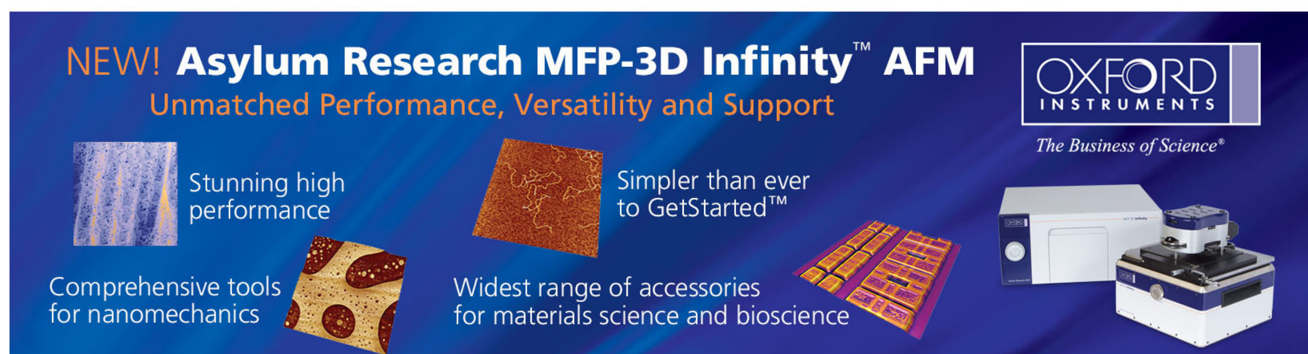

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High voltage characteristics of junctionless poly-silicon thin film transistors

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The breakdown voltage (V_{BD}) and breakdown mechanism of junctionless (JL) poly-Si thin film transistor (TFT) were compared to the conventional inversion-mode (IM) TFT using fabricated devices and 3D quantum-corrected hydrodynamic transport device simulation. The simulated results are correspondent with experimental ones. The analyses of electric field distributions in on-state show that the channel of JL devices can equally share the voltage like a resistor, because there are no junctions formed between channel and source/drain. The JL TFT shows excellent breakdown characteristics; the off-state V_{BD} of 53.4 V is several times larger than V_{BD} of 9.5 V in IM TFT with same device size. JL devices have large potential for high voltage power metal-oxide-semiconductor devices and circuit applications. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4821856]

The scaling of the channel lengths in conventional metal-oxide-semiconductor (MOS) field-effect-transistors (FET) shrink to the order of nanometers, several critical challenges, such as the need to reduce short-channel effect (SCE), to deliver a higher on-current, to reduce power consumption, and to eliminate intrinsic parameter fluctuations, must be addressed.[1–4] Numerous approaches for addressing these issues have been introduced in the past ten years. These include the use of high-k/metal-gate technology to suppress the direct tunneling current in gate oxides; to enhance mobility using strain, and to develop multi-gate structure such as FinFET and nanowire (NW) structures to reduce SCE.[5,6] Recently, the concept of the junctionless (JL) nanowire transistor, which contains a single doping species at the same level in its source, drain, and channel, has been investigated.[7–12] The junctionless device is basically a gated resistor, in which the advantages of junctionless devices include (1) avoidance of the use of an ultra shallow source/drain junction, which greatly simplifies the process flow; (2) low thermal budgets owing to implant activation anneal after gate stack formation is eliminated, and (3) the current transport is in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. However, most of studies have focused on the device design and performance estimation of JL transistors at low voltage for digital circuit application, but few have addressed the breakdown mechanism and breakdown voltage (V_{BD}) of such devices for power device and circuit application. In this work, the comparative study on V_{BD} between JL thin film transistor (TFT) to conventional inversion-mode (IM) TFT by using experimental measurement and 3D quantum-corrected hydrodynamic transport device simulation is addressed. The physical and electrical properties at high voltage of the JL and IM TFTs are presented.

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Figure 1(a) presents the schematic of single NW in the simulated device structure and relevant parameters. The parameters setting are fitted as the fabricated devices, in which the film length (L_f) and gate length (L_g) are 2μm and 1μm, respectively. The doping concentrations in the source/drain/channel of JL TFT are set to $2 \times 10^{19}\,cm^{-3}$. In IM TFT, the source/drain doping concentrations are $1 \times 10^{20}\,cm^{-3}$, and the channel doping is opposite type with $1 \times 10^{17}\,cm^{-3}$ concentrations. The gate material is poly-silicon with different doping concentration to tune an appropriate device threshold voltage (V_{th}) for JL and IM TFTs. The source/drain extension is used to prevent misalignment of e-beam lithography for gate patterning. Figs. 1(b) and 1(c) show the cross-sectional transmission electron microscopic (TEM) images of channel region for JL and IM TFTs, respectively. To obtain accurate numerical results for a nanometer-scale device at high voltage bias, the device is simulated by solving 3D quantum-corrected hydrodynamic transport equations using the commercial tool, Synopsys Sentaurus Device.[13] In quantum-corrected equations, a density gradient model is used in the simulation. Additionally, the bandgap narrowing model, the band-to-band tunneling model, and Shockley-Read-Hall recombination with the doping-dependent model are also considered. The detailed process flows in our fabricated devices are investigated in Refs. 14 and 15. Figure 2 shows transfer I_d–V_g characteristics of experimental and simulation results in JL and IM TFTs. The experimental subthreshold swing is 61 mV/dec for JL TFTs and is 304 mV/dec for IM TFTs. The experimental V_{th}, which is defined as the gate voltage at $I_d = 1 \times 10^{-10}$ A for JL TFTs and at $I_d = 1 \times 10^{-8}$ A for IM TFTs, are 0.2 V and 0.3 V, respectively. The simulated data well fit the experimental data. Figure 3 plots electric field distributions along the line of interaction between AA′ and BB′ plane (indicated in Fig. 1) for JL and IM TFTs at on-state ($V_g = 10$ V, $V_d = 10$ V) and off-state ($V_g = 0$ V, $V_d = 10$ V). Because the JL device is a gated resistor, there are no junctions formed at source and drain sides; the potential trends to equally shares

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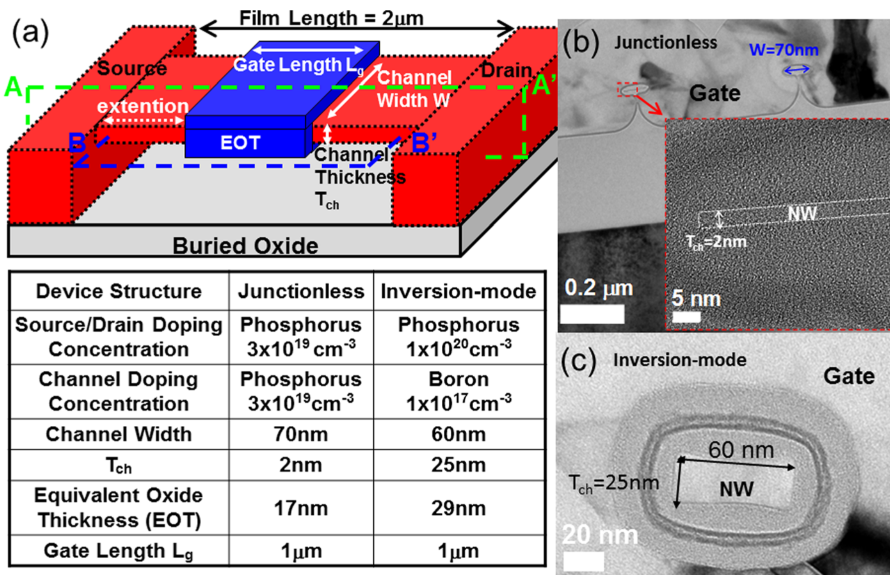

Device Structure	Junctionless	Inversion-mode
Source/Drain Doping Concentration	Phosphorus 3×10^{19} cm^{-3}	Phosphorus 1×10^{20}cm^{-3}
Channel Doping Concentration	Phosphorus 3×10^{19}cm^{-3}	Boron 1×10^{17}cm^{-3}
Channel Width	70nm	60nm
T_{ch}	2nm	25nm
Equivalent Oxide Thickness (EOT)	17nm	29nm
Gate Length L_g	1μm	1μm

FIG. 1. The simulated device structure and parameters of simulated JL TFT and IM TFT. The experimental cross-sectional TEM images of (b) JL TFT and (c) IM TFT in the gate width direction.

in whole film like a resistor. However, the situation only happens at turned-on state or floating-gate voltage state, in which the current flows from source to drain through the whole cross-section of silicon film and the behavior of JL devices indeed acts as a resistor. In Fig. 3(a), the electric field of IM devices concentrates at the two side edges of the gate, where are the depletion region between channel and source/drain p-n junction. In contrast, the electric field in JL devices is averagely distributed like a resistor, thus, the maximum electric field in JL device is significantly smaller than in IM device. In addition, Fig. 3(a) also indicates that silicon film can be treated as the series of three resistors (source extension, channel, and drain extension regions). The resistance of the channel differs from that of source/drain extension regions because the carriers in the channel are controlled by the gate; therefore, the electric field is different between channel and source/drain extension regions. On the other hand, when the JL device turns off, the channel region is depleted and the increase of the drain voltage produces the larger depletion region than with zero bias, the behavior is the same as in IM devices. However, since the doping concentration gradient between channel and drain in JL devices

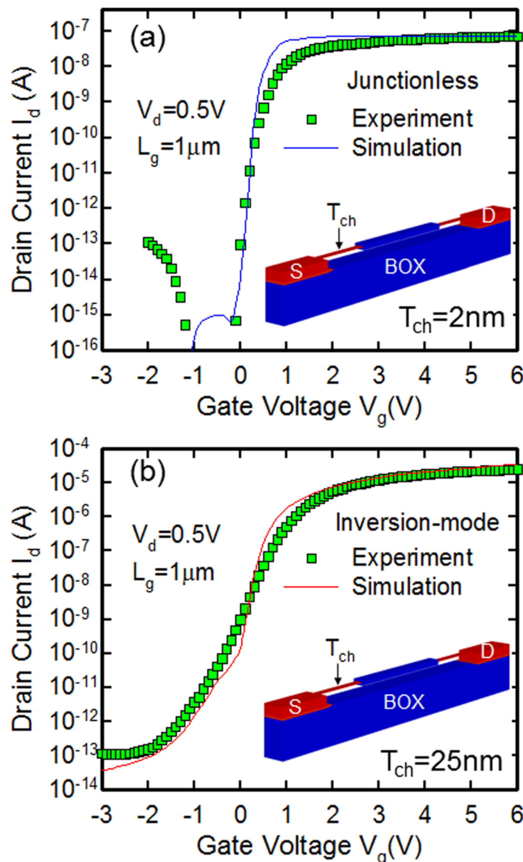

FIG. 2. Experimental and simulated I_d–V_g curves for (a) JL and (b) IM TFTs. The inset shows simulated devices with $L_g = 1$ μm.

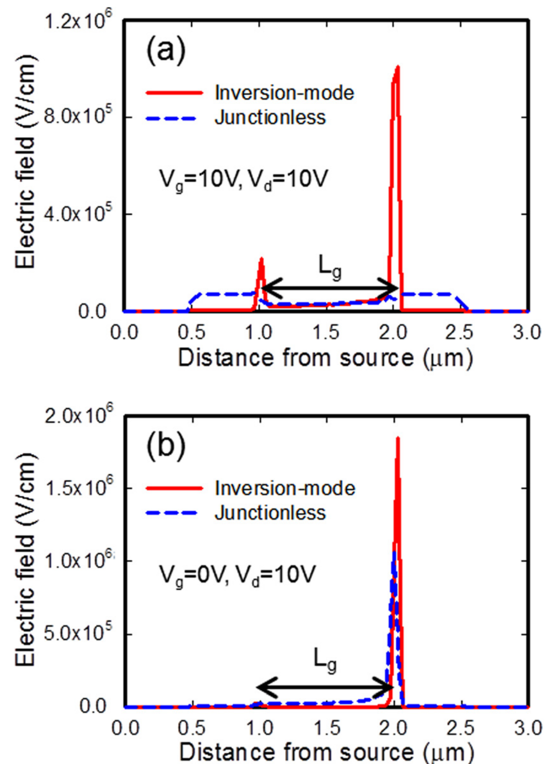

FIG. 3. The electric field distribution along the line of interaction between AA′ and BB′ plane in the middle of channel for JL and IM TFTs at (a) on-state ($V_g = 10$ V, $V_d = 10$ V) and (b) off-state ($V_g = 0$ V, $V_d = 10$ V).

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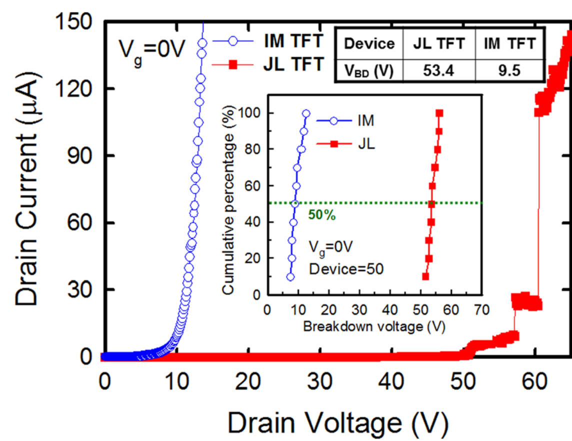

FIG. 4. The I_d-V_d curves comparison for JL and IM TFTs at $V_g = 0\,V$. The V_{BD} extracted form the curves are listed in the figure. The inset shows cumulative distributions of V_{BD} for JL and IM TFTs.

is intrinsically smaller than in IM devices, the maximum electric field is still smaller, as displayed in Fig. 3(b). Therefore, a high V_{BD} in JL device can be expected.

To confirm the simulation results, Fig. 4 compares the breakdown voltages of IM TFT and JL TFT with same size in the off-state ($V_g = 0\,V$). The V_{BD}, which is extracted from I_d-V_d curve at $I_d = 10\mu A$ of device with $L_g = 1\,\mu m$ and $V_g = 0\,V$, is 53.4 V for JL TFT and 9.5 V for IM TFT. The measurement V_{BD} of JL devices show much higher than that of IM devices owing to the reduced electric field in JL TFT, as simulated results in Fig. 3(b). The cumulative distributions of V_{BD} at $V_g = 0\,V$ for 50 devices are shown in the inset of Fig. 4. Fig. 5 plots the measured I_d-V_d curves for different gate voltage bias condition (on-state and off-state) of fabricated JL devices. The device breakdowns observed in fabricated devices are oxide breakdown, which is confirmed by the measured gate current equal to drain current when device breakdown. When the drain voltage increases, the potential in the channel also increases, the increased potential enhance the potential difference between channel and gate, resulting in the breakdown of the gate oxide. If the device is turned on ($V_g = 10\,V$), the channel is like a resistor and the electric field is uniformly distributed to alleviate impact-ionization rate. The V_{BD} in on-state is thus improved than that in off-state. In addition, If the gate electrode is floated, the vertical (gate to channel direction) electric field is also reduced, resulting in the largest V_{BD}. The inset of Fig. 5 shows cumulative distributions of V_{BD} for $V_g = 0\,V$ and $V_g = 10\,V$. The measurement results prove that the V_{BD} of the junction avalanche breakdown in JL TFT is very large, which is not seen before the oxide breakdown in our device.

We have studied the high voltage electrical and physical characteristics using the experimental measurement and 3D quantum-corrected hydrodynamic transport device simulations. In the on-state or floating-gate state, the electric field distributions along source to drain indicate that the potential in the film of JL TFT is equally distributed due to resistor-

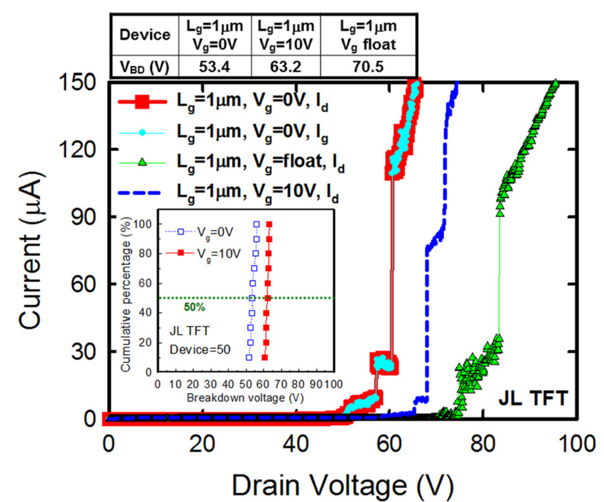

FIG. 5. The measured currents as a function of drain voltage for different bias conditions in JL TFTs. The V_{BD} is extracted from the curves, as listed in the figure. The inset shows cumulative distributions of V_{BD} for different bias conditions.

like structure of JL devices. In the off-state, the doping concentration gradient between channel and drain in JL devices is intrinsically smaller than in IM devices, the maximum electric field is thus still smaller. Therefore, the breakdown voltage in JL TFT is several times larger than IM TFT with same device size. This investigation explores its potential in JL TFTs for high voltage power MOS devices, system-on-panel and 3D stacked applications.

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