Anomalous Reverse Short-Channel Effect in p^+ Polysilicon Gated P-Channel MOSFET

Chun-Yen Chang, *Fellow, IEEE*, Chih-Yung Lin, *Student Member, IEEE*, Jih Wen Chou, Charles Ching-Hsiang Hsu, *Member, IEEE*, Hong-Tsz Pan, and Joe Ko, *Member, IEEE*

***Abstract*— The boron-penetration-dependent Reverse Short Channel Effect (RSCE) on the threshold voltage is observed for short channel p^+ poly-gate PMOSFET's. The RSCE is found to be more significant as the boron penetration becomes more severe. The RSCE is significant in BF_2 doped poly-gated MOS devices and is alleviated in buffered poly-gated MOS devices. Fluorine enhanced boron diffusion in the gate oxide during high temperature process is believed to account for the RSCE, which is also confirmed by using a two-dimensional process simulator.**

I. Introduction

THE anomalous Reverse Short Channel Effect (RSCE), i.e., the threshold voltage increases with decreasing channel length (L_G), has been reported [1]–[6] in submicrometer MOSFET devices. The observed threshold voltage enhancement of N- and P-MOSFET's has been explained by the effects of Oxidation-Enhanced impurity Diffusion (OED) during the poly-gate sidewall reoxidation after the gate pattering [1], vacancies injection during silicide formation [2], fixed oxide charges [3], [4], and damage created by the source/drain ion implantation [5], [6].

The RSCE for p^+ poly-gate PMOS has also been observed by Sung *et al.* [7], they suspected that H and/or OH radical during deposition of the TEOS gate spacer could induce this effect. Furthermore, it has been predicted by Pfiester *et al.* [8] that the RSCE may be attributed to poly-gate reoxidation step. In this paper, RSCE is found to be strongly dependent on the degree of boron penetration. The two-dimensional simulator, SUPREM-4 [9] is employed to investigate the mechanism of boron-penetration-dependent RSCE.

II. Experimental

P^+ poly-gate P-MOSFET's were fabricated using boron doped $\langle 100 \rangle$-oriented substrates with resistivity of $15 \sim 25\ \Omega$-cm by employing conventional CMOS twin-well technology. The n-well were formed by phosphorus ion implantation and high temperature drive-in to adjust the surface concentration to $5 \times 10^{16}\ cm^{-3}$. Double channel implants were formed by As and phosphorus implants to adjust the threshold voltage to about -0.8 V. A 11 nm-thick gate oxide was thermally grown by using dry oxygen and hydrogen chloride at 900 °C, followed by a 3000 Å deposition of undoped polysilicon. P^+ poly-gate was formed by ion implantation of BF_2 at various dosages and rapid thermal anneal (RTA) for 30 sec. prior to the gate etch. After patterning, oxide spacers were formed. The lightly-doped drain (LDD) was formed by P^- LDD and P^+source/drain implantations with BF_2 through a thin sacrificial thermal oxide grown at 900 °C. Then a LTO-BPSG deposition and a reflow of BPSG at 900 °C for 20 min. followed by a metal-1 deposition were consecutively performed. Finally received a plug anneal at 900 °C for 10 min. To suppress the boron penetration effect [10], [11], a proposed buffered poly-gate structure which composed of amorphous silicon layer and polysilicon layer was also fabricated.

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C.-Y. Chang, C.-Y. Lin, and J. W. Chou are with National Nano Device Laboratory and Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

C. C.-H. Hsu is with Microelectronics Laboratory, Semiconductor Application & Technology Research Group, Department of Electrical Engineering, National Tsing-Hua University, Hsinchu, Taiwan.

H. T. Pan and J. Ko are with United Microelectronics Corporation, Science-Based Industrial Park, Hsinchu, Taiwan.

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III. Results and Discussion

High frequency C-V analysis was performed on $100\ \mu m \times 200\ \mu m$ PMOS capacitors for examining the boron penetration phenomena. As shown in Fig. 1, the positive-shifts in the C-V curves are due to the boron penetration, i.e., the boron from the heavily doped p^+ polysilicon gate electrode diffuse through the thin gate oxide and into the underlying n-well region. However, the boron penetration is greatly alleviated in the devices with the buffered poly-gate. The under-laid amorphous silicon is found to retard boron penetration very effectively.

Fig. 2 shows the measured PMOS threshold voltages as a function of poly-gate lengths. The threshold voltage is determined by the extrapolation of the interception point on the V_{GS} axis of the linear I_{DS} versus V_{GS} slope at the maximum transconductance (at $V_{DS} = -0.1$ V) in the I_{DS} versus V_{GS} plot. Both types of samples (control and the buffered poly-gate) have a positive threshold voltage shift when dosage of boron implantation in the poly-gate increases from $2 \times 10^{15}\ cm^{-2}$ to $1 \times 10^{16}\ cm^{-2}$. However, smaller positive threshold voltage is observed for the buffered structure. In Fig. 2, by comparing the short-channel effect of p^+-poly P-MOSFET with n^+-poly P-MOSFET, it is observed that n^+-poly P-MOSFET shows threshold voltage "roll-off," while p^+-poly P-MOSFET illustrates threshold voltage "roll-up" as the channel length of devices become shorter. Particularly, the significant roll-up is observed in the devices with severe boron penetration.

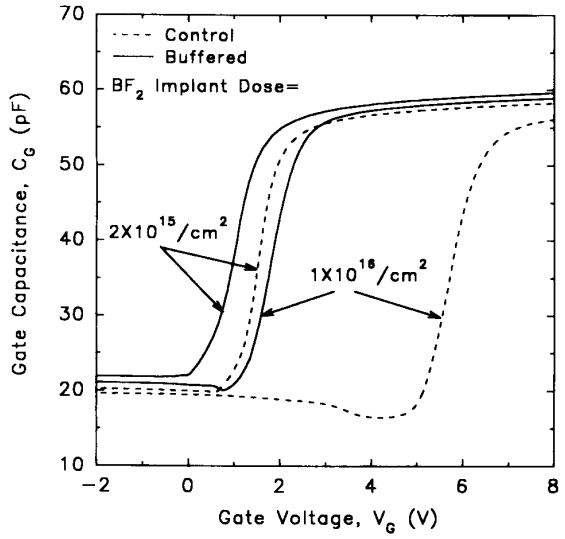

Fig. 1. High frequency C-V curves for both control- and buffered p^+ poly-gated PMOS capacitors ($100\ \mu m \times 200\ \mu m$).

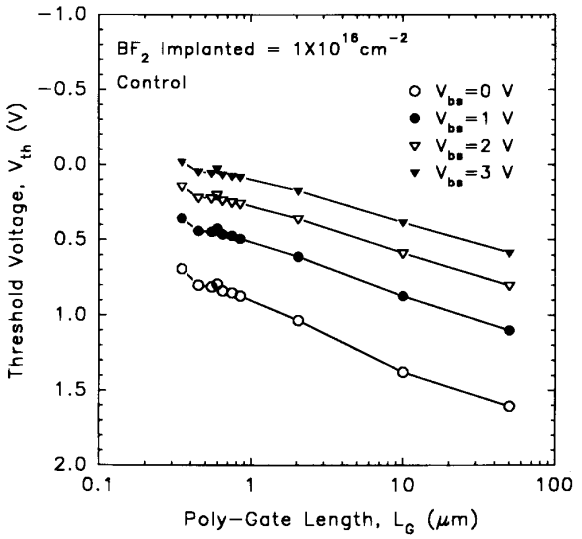

Fig. 3. The threshold voltage of PMOSFET's of the control sample as a function of the poly-gate length under various substrate bias.

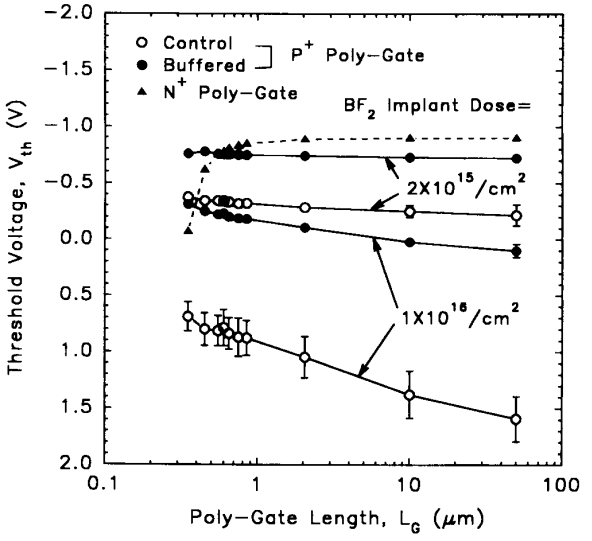

Fig. 2. Measured PMOSFET threshold voltage as a function of the poly-gate length for n-type and p-type polysilicon-gate device. The p^+ poly-gated PMOSFET's were implanted with BF_2 of 2×10^{15} cm^{-2} and 1×10^{16} cm^{-2}, respectively.

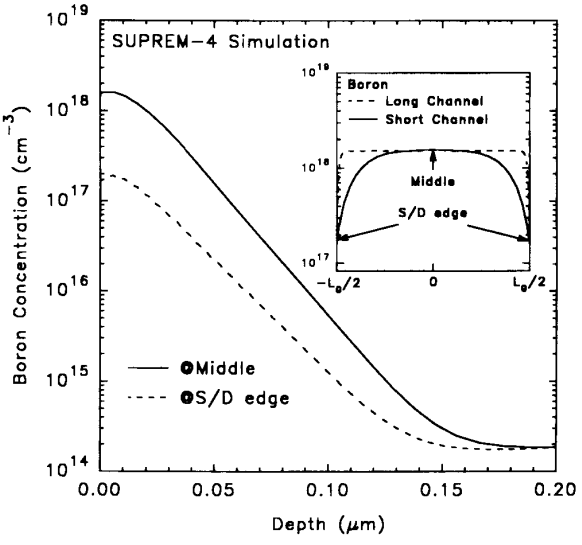

Fig. 4. Penetrated boron concentration in the channel region by SUPREM-4 simulator incorporated with enhanced boron diffusivity in the gate oxide (1000×). The solid line represents the vertical profile in the middle, while the dashed line represents the vertical profile at source/drain edges. The insert shows the simulated lateral channel profile of penetrated boron impurities for a long channel and a short channel cases.

Fig. 3 shows the channel length dependence of threshold voltage of the control samples under four different substrate bias (0, 1, 2, and 3 V) which were severely boron penetrated. The body effect is less severe for the shorter channel length devices. Since body effect depends only on the gate oxide thickness and channel doping distribution, it is evident that channel doping profile is modified as the channel length changes.

To explain the relationship between the modification of the channel profile and the boron penetration effect, SUPREM-4 simulator is used to examine enhanced boron penetration due to fluorine incorporation [7]. The enhancement of the boron diffusivity by as much as 1000 times in the thin gate oxide was assumed for fluorine enhanced boron diffusion. The simulated depth profiles of penetrated boron impurity in the middle of the channel and at the source/drain edges for the device are shown in Fig. 4 with an insert of a lateral profile for a short channel ($L_G = 0.5\ \mu m$) and a long channel ($L_G = 5\ \mu m$) case. The final penetrated boron doping concentration at the source/drain edges is shown to have smaller peak surface concentration than in the middle. Combined effects of enhanced boron diffusivity

and subsequent thermal processes after the gate etch, lateral non-uniformity in the doping profile is revealed, therefore substantial modification of the threshold voltages are present. The more boron concentration, the more severe non-uniform distribution along the channel is shown. As the channel length is reduced, effect from the S/D portions becomes more predominant. Thus, the RSCE is more significant in the highly boron penetrated samples. The threshold voltage shift, $V_{th}(L_G = 0.5\ \mu\text{m}) - V_{th}(L_G = 5\ \mu\text{m})$, is -166 mV for the proposed 1000 times enhancement, which is obtained from a two-dimensional device simulator, MEDICI [12], when the SUPREM-4 results are used as the input data.

IV. Conclusion

In this work, short-channel p^+ poly-gate PMOSFET's were fabricated. The reverse short channel effect (RSCE) was found to correlate to the boron penetration effect. More significant RSCE was observed in the devices with more severe boron penetration. Buffered poly-gate MOSFET has less boron penetration and therefore less RSCE. The RSCE of the p^+ poly-gate P-MOSFET's is explained by the SUPREM-4 simulator in which the model of fluorine enhanced boron penetration is incorporated.

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