Performance Improvement in RF LDMOS Transistors Using Wider Drain Contact

Kun-Ming Chen, *Member, IEEE*, Bo-Yuan Chen, Chia-Sung Chiu, Guo-Wei Huang, *Member, IEEE*, Chun-Hao Chen, Horng-Chih Lin, *Senior Member, IEEE*, Tiao-Yuan Huang, *Fellow, IEEE*, Ming-Yi Chen, Yu-Chi Yang, Brenda Jaw, and Kai-Li Wang

***Abstract*— In this letter, we proposed a new layout structure for RF laterally diffused metal-oxide-semiconductor (LDMOS) transistors. In a multifinger layout, the drain contact region was designed to be wider than the channel region. The wider drain increases the equivalent drift region width to reduce the drift resistance and suppress the quasi-saturation effect. We found that the wide-drain multifinger LDMOS devices have lower on-resistance, higher cutoff frequency, higher maximum oscillation frequency, and better power performances than the standard multifinger ones.**

***Index Terms*— Drain contact, laterally diffused metal-oxide-semiconductor (LDMOS), multifinger layout, resistance, RF transistor.**

I. Introduction

LATERALLY diffused metal-oxide-semiconductor (LDMOS) transistors have been widely used in RF power amplifier modules for a high-frequency range up to 3.8 GHz [1]–[4]. The tradeoff between the on-resistance (R_{ON}) and the breakdown voltage (V_{BD}) is one of the important design issues for LDMOS fabrication. Various drift region designs have been investigated to solve this tradeoff [5]–[7]. In these researches, the reduction of R_{ON} was achieved by decreasing the resistance in drift region through optimizing the doping profile. Lower drift resistance can also improve the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) and thus the RF power performance.

Aside from changing the device process flow, the drift resistance can also be reduced by optimizing the layout structure. In [8] and [9], device layouts with a ring style have been demonstrated to reduce the on-resistance and increase f_T and f_{max}. When the channel width in a unit cell is scaled down, the curvature radius in drift region will be, however, increased leading to the increase of electric field crowding and the reduction of breakdown voltage. In this letter, we proposed and demonstrated a new LDMOS structure using conventional multifinger layout but the drain contact region is wider than the channel region to improve the RF performances without deteriorating the breakdown voltage apparently.

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K.-M. Chen, B.-Y. Chen, and C.-S. Chiu are with the National Nano Device Laboratories, Hsinchu 30078, Taiwan (e-mail: kmchen@narlabs.org.tw).

G.-W. Huang and H.-C. Lin are with the National Nano Device Laboratories, Hsinchu 30078, Taiwan, and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan.

C.-H. Chen and T.-Y. Huang are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan.

M.-Y. Chen, Y.-C Yang, B. Jaw, and K.-L. Wang are with the United Microelectronics Corporation, Hsinchu 30076, Taiwan.

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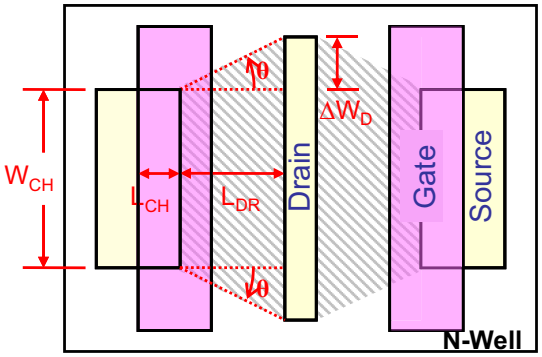

Fig. 1. Layout structure of wide-drain multifinger LDMOS in a unit cell. The drain contact width is larger than the channel width, so the equivalent drift region width is larger than that in conventional devices.

II. Device Structure

The n-channel LDMOS transistors were fabricated by a 0.5 μm CMOS-DMOS process with a gate oxide thickness of 135 Å. The n-well drift region underneath the field oxide was adopted for sustaining the high drain voltage. Effective channel length (L_{CH}) and drift length (L_{DR}) are 1.1 and 1.9 μm, respectively. Detailed description of the device structure can be found in [8]. For RF applications, the transistors are usually implemented in a multifinger layout to reduce the gate resistance. In this letter, we proposed a new layout design method based on the multifinger structure. As shown in Fig. 1, the drain contact width is larger than the channel width in our devices. Assuming the current flow in the effective drift region (shadow area in Fig. 1) is uniform, the equivalent drift width can be derived as

$$W_{DR,eq} = \frac{2L_{DR}\tan\theta}{\ln\left(1+2L_{DR}\tan\theta/W_{CH}\right)} \quad (1)$$

where W_{CH} is the channel width of one finger and θ is the angle indicating the ratio of increased drain contact width (ΔW_D) and drift length as shown in Fig. 1. For conventional multifinger device, θ is zero. The width estimated from (1) approaches to the one at the middle point of the drift region.

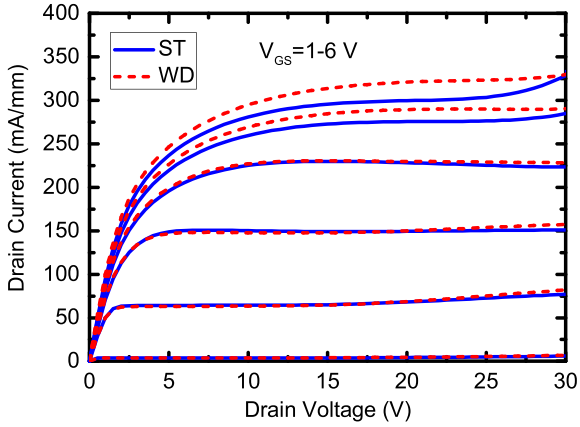

Fig. 2. Output characteristics of LDMOS transistors with wide-drain and standard multifinger structures. The channel width of one finger is 5 μm.

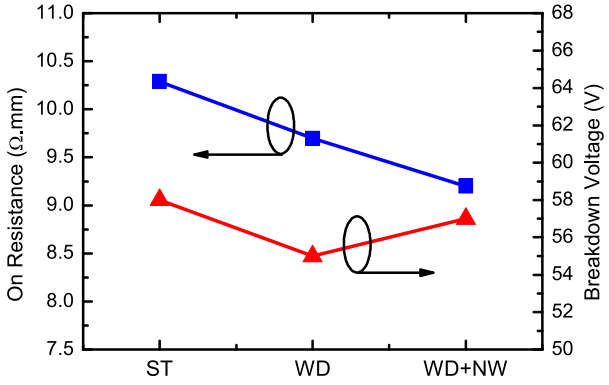

Fig. 3. On-resistances and breakdown voltages of LDMOS transistors with different drain contact and channel widths. ST and WD are the ST and WD devices with W_{CH} = 5 μm. WD + NW is the WD device with W_{CH} = 2.5 μm.

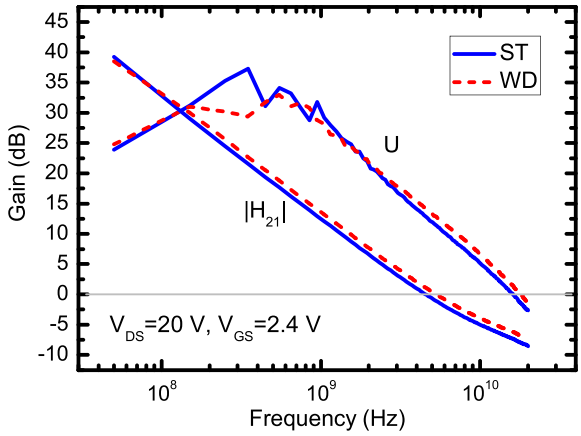

Fig. 4. Short-circuit current gain (H_{21}) and unilateral power gain (U) of LDMOS transistors with WD and ST multifinger structures. The channel width of one finger is 5 μm.

Therefore, the effective drift width in the wide-drain (WD) device could be larger than that in the conventional device with the same channel width, and it is increased by increasing θ.

III. Results and Discussion

The output characteristics of LDMOS transistors with WD and standard (ST) multifinger structures are shown in Fig. 2, where W_{CH} and θ are 5 μm and 22.5°, respectively. At high gate voltages, the increase of drain current becomes insensitive to the increase of the gate voltage. This phenomenon is called the quasi-saturation effect, which is due to the velocity saturation in the drift region. The critical current for the onset of quasi-saturation effect depends on the drift resistance [10]. Because the equivalent drift width in the WD device is larger than that in ST counterpart, WD device exhibits a lower drift resistance and thus a higher critical current for the onset of quasi-saturation effect. As shown in Fig. 2, the drain currents in the WD device are higher than that in ST device at high gate voltages, owing to the suppression of quasi-saturation effect. In addition, we also observed that the drain currents in ST device increase rapidly for high gate voltages and high drain voltages (V_{DS} > 25 V), which is caused by the impact ionization in the drift region [11]. For WD device, the lower drift resistance will result in a lower electric field in the drift region, so the impact ionization will be reduced and thus the rapid increase of current is suppressed.

From the linear region of Fig. 2, we extracted the on-resistance at gate voltage V_{GS} = 5 V, and the results are shown in Fig. 3, where θ is kept to 22.5°. The off-state breakdown voltages for different layouts are also shown in this figure. It can be seen that the WD and ST devices have similar breakdown voltages. On the other hand, the on-resistance (R_{ON}) is reduced by increasing the drain contact width. Therefore, the tradeoff between the on-resistance and breakdown voltage can be solved by increasing the drain contact width, which will not increase the complexity of device fabrication.

The R_{ON} reduction in WD device is more apparent when the channel width of one finger is changed from 5 μm to 2.5 μm. This is because the equivalent drift width can be increased more efficiently by narrowing the channel width according to (1). From these results, we concluded that the WD layout might have a significant improvement in device performance when it applies to the nanowire power transistors. We extracted the drain resistances (R_d) at V_{DS} = 0.5 V and they are 7.6 and 7.0 Ω·mm for ST and WD devices, respectively. The R_d improvement corresponds to the prediction of (1). It suggests that the lower R_{ON} in WD device is attributed to the lower R_d because of the larger equivalent drift width.

To examine the RF performances of LDMOS transistors, S-parameters were measured on chip using an Agilent 8510 network analyzer from 0.1 to 20 GHz. The devices under test have a multifinger gate configuration featuring 32 fingers with a total width (W) of 160 μm. After de-embedding the parasitic pad effects from measured S-parameters, short-circuit current gain (H_{21}) and unilateral power gain (U) were calculated to extract f_T and f_{max}, respectively. As shown in Fig. 4, the extracted f_T and f_{max} of WD device are 5.3 and 18 GHz, respectively, higher than those of ST counterpart (4.6 and 16 GHz). These results suggest that better RF performances could be achieved in LDMOS with a larger drain contact width. In [12], it was reported that the drain resistance has a large influence

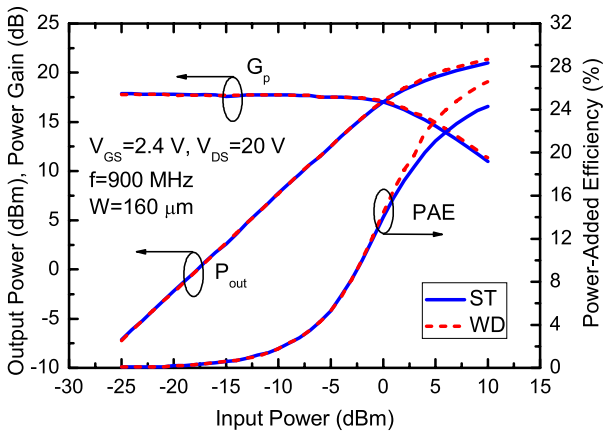

Fig. 5. RF power characteristics of LDMOS transistors with WD and ST multifinger structures. The channel width of one finger is 5 μm.

on f_T and f_{max}. The values of f_T and f_{max} will be degraded with the increase of drain resistance. Therefore, higher f_T and f_{max} in WD devices might be contributed to the lower drain resistance compared with the ST ones. In addition, though the WD device exhibits a wider drain contact, its gate–drain capacitance might be similar to that of ST one because of the same gate–drain overlap area. We extracted the gate–drain capacitances roughly from the two-port admittance parameters at low frequencies [13], and they are $\sim$ 71 fF for both devices.

If we increase the device width of ST devices making it equal to the drain contact width of WD devices, the high-frequency performances of ST devices might be still worse than those of WD devices in theory. When considering the drain resistance, the cutoff frequency can be written as [12]

$$f_T = \frac{g_{m'}}{2\pi\left[C_{gs'} + C_{gd'}\left(1 + g_{m'}R_{d'}\frac{W_{CH}}{W_{DR,eq}}\right)\right]} \quad (2)$$

where $g_{m'}$, $C_{gs'}$, $C_{gd'}$, and $R_{d'}$ are the transconductance, gate–source capacitance, gate–drain capacitance, and drain resistance per unit width, respectively. For ST devices, when W_{CH} increases, $W_{DR,eq}$ also increases equally. Therefore, the cutoff frequency cannot be improved by increasing the channel width of conventional multifinger structure. For WD device, $W_{CH} < W_{DR,eq}$, so its f_T must be always higher than that of ST counterpart. A similar conclusion can also be derived for maximum oscillation frequency.

Fig. 5 shows the RF power characteristics of LDMOS transistors. Because the f_{max} enhancement is only 10% by increasing the drain contact width for devices with $W_{CH} = 5$ μm, the improvement of power gain at low input powers is not observed clearly for WD devices. Since the drift resistance and thus drain resistance can be reduced more efficiently for device with narrower W_{CH} when using WD structure, we expect that the linear power gain could be enhanced apparently in nanowire WD devices. At high input powers, the gain compression is improved for WD device because of lower drain resistance. Therefore, the WD device has a better power handle capacity and power-added efficiency (PAE) compared with ST counterpart.

IV. Conclusion

A multifinger LDMOS layout with a wider drain contact was demonstrated for RF applications. With the wider drain contact, the equivalent drift region width can be increased to reduce the on-resistance and suppress the quasi-saturation effect. In addition, owing to the reduction of drain resistance, the cutoff frequency, maximum oscillation frequency, output power at 1-dB compression point, and PAE were improved for devices with WD structure.

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