Fabrication of High-Performance ZnO Thin-Film Transistors With Submicrometer Channel Length

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***Abstract*—A method was developed to fabricate ZnO thin-film transistors (TFTs) with submicrometer channel length. In this scheme, mature process techniques are used to form a suspending hardmask bridge on the wafer surface, which enables the subsequent construction of a TFT by the sequential deposition of gate oxide, ZnO channel layer, and Al source/drain contacts. Excellent electrical characteristics were demonstrated by the fabricated ZnO TFTs that show high ON/OFF current ratio (>10^9), low subthreshold swing (89 mV/decade), and high field-effect mobility (41 cm^2/V s). Very small variation in the device characteristics is also demonstrated.**

***Index Terms*—Metal oxide, shadow mask, submicrometer, thin-film transistors, ZnO.**

I. Introduction

RECENTLY, metal oxide has been adopted as the channel material of thin-film transistors (TFTs) in various applications, such as active matrix liquid crystal displays [1], [2], high-frequency microwave devices [3], back-end-of-line power transistors [4], [5], and flexible displays [6]. In particular, ZnO and its variants, IGZO, HIZO, and so on have great potential to replace the conventional a-Si:H and ploy-Si materials due to their high mobility, high transparency, and low process temperature.

Several device structures of TFTs have been proposed and developed [7]. In 2010, Lu *et al.* [8] developed a simple and ingenious approach to fabricate coplanar ITO TFT using only one metal shadow mask. In this approach, the shadow mask was employed to define the source/drain (S/D) regions. After the sputtering deposition of an ITO film, thick S/D regions accompanied with a thin self-assembled channel are formed. The mechanism responsible for the above result is attributed to the scattering of the deposition species in the ambient.

Although the above scheme is simple and novel, there still exist a few issues.

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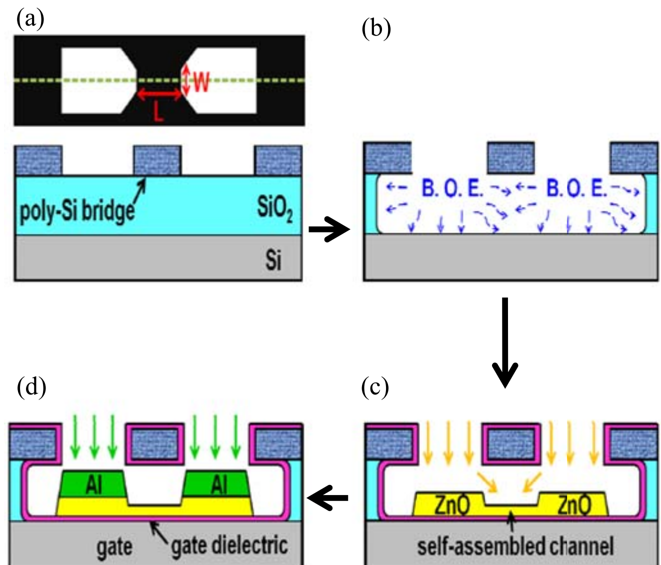

Fig. 1. Fabrication sequence of the ZnO TFT. Top view of the structure is shown at the top of (a). For simplicity, the deposited ZnO and Al on the poly-Si hardmask are not shown in (c) and (d).

1) Distance between the shadow mask and substrate is hard to control due to warps in both the shadow mask and substrate. This would result in a variation in the deposited profile and thus the device characteristics.
2) Dimensions of the patterns on the shadow mask are usually large (e.g., $\geqq$ 50 μm). Devices with submicrometer dimensions and beyond are difficult to achieve.
3) In the previous research [8] only one ITO film is deposited. This makes it hard to optimize the structure for a good TFT that contains insulating gate oxide, semiconducting channel, and metallic S/D contacts.

In this letter, a novel approach is proposed to address the above issues. The new scheme adopts mature lithographic and etching techniques so that submicrometer devices with small variations in characteristics can be readily achieved. Besides, we also show that the profile of the deposited films can be cleverly tailored. This feature favors the construction of refined device structures with improved characteristics.

II. Experimental Details

The proposed scheme is demonstrated with a one-mask process. The fabrication sequence of the ZnO TFT is shown in Fig. 1. For simplicity, Si substrate is used as the bottom

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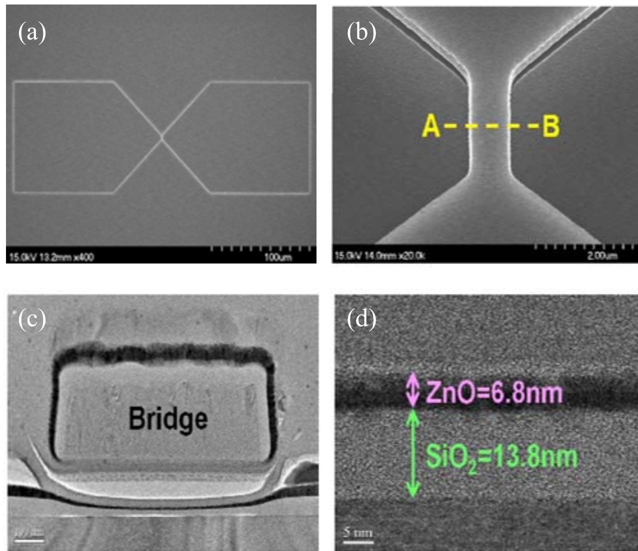

Fig. 2. (a) SEM top view image of a fabricated ZnO TFT. (b) Suspending bridge formed on the wafer surface. (c) TEM image showing the cross-section along the line AB in (b). In this figure a nitride capping layer was deposited to passivate and strengthen the device. (d) TEM image showing the thinnest part at the center of channel.

gate. First, a 400-nm-thick SiO_2 and 200-nm-thick undoped ploy-Si were deposited sequentially on an n-type Si wafer by low-pressure chemical vapor deposition to serve as the sacrificial and hardmask layers, respectively. After an I-line-based photolithographic step to generate the photoresist pattern of S/D regions [top of Fig. 1(a)], the surface poly-Si was etched as shown in Fig. 1(a). Wet etching using buffer oxide etch solution was subsequently carried out to remove the underlying SiO_2 [Fig. 1(b)]. After this step the central poly-Si stripe became a suspended bridge. A 50-nm-thick tetraethylorthosilicate (TEOS)-based SiO_2 was then deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C under a pressure of 500 mtorr to serve as the gate dielectric, followed by the deposition of 50-nm-thick ZnO channel layer using a radio-frequency magnetron sputter at room temperature under a pressure of 5 mtorr [Fig. 1(c)]. The deposited ZnO film is polycrystalline as verified by the X-ray diffraction analysis. If the channel length (defined by the width of the poly-Si strip) is sufficiently short (e.g., <0.8 μm in the present case), a self-assembled channel is formed [8] that is much thinner than that at the S/D regions. Finally, 100-nm Al was deposited by a thermal coater at a pressure of $\sim 8 \times 10^{-6}$ torr to form the S/D contacts. Owing to the ultralow deposition pressure, the Al contacts are disconnected between the source and drain. Electrical characteristics of the ZnO TFTs were measured by an HP4156 parameter analyzer and the device structure was traced by scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

III. Results and Discussion

Fig. 2(a) and (b) shows the SEM top view images of a fabricated ZnO TFT. The suspending bridge is observed and its width is $\sim$0.8 μm that is longer than the designed dimension (0.6 μm). This is due to the follow-up deposition of gate

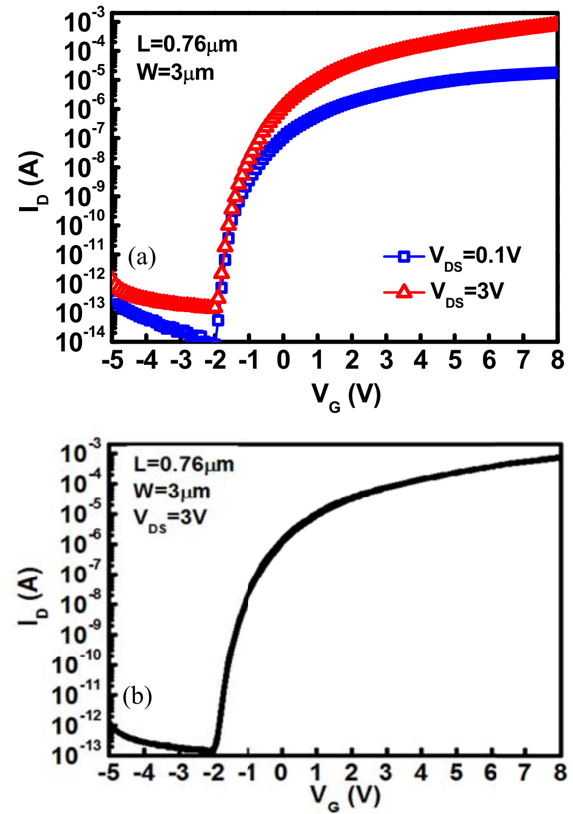

Fig. 3. (a) Transfer curves of a ZnO TFT at $V_{DS} = 0.1$ and 3 V. (b) Transfer curves of five devices located at different dies at $V_{DS} = 3$ V.

oxide, channel, and metal materials after the formation of suspending bridge. TEM image of the cross-section along the line AB in Fig. 2(b) is shown in Fig. 2(c). Continuous ZnO channel under the suspending bridge can be observed and its thickness is gradually thinned down along the direction toward the center of the channel. Similar condition can also be seen on the gate dielectric although to a lesser extent. In contrast, Al metal pads are isolated from each other and form the S/D regions. The cross-sectional image of a fabricated device is shown in Fig. 2(c). Obviously the profiles of the deposited films (gate oxide, ZnO channel, and Al S/D contact pads) are quite different and the differences are mainly related to the deposition pressure. As the scattering probability is greatly increased with increasing pressure, the film thickness is expected to be thicker at the channel center as the deposition pressure is higher. Fig. 2(d) shows the thinnest part of ZnO and oxide films at the center of the channel with the thickness of 6.5 and 13.8 nm, respectively, which are much thinner than the set thickness (50/50 nm). As the deposition pressure of the PECVD process is two orders in magnitude higher than that of the sputtering process, the oxide is much thicker than the ZnO at the channel center. The deposition of Al film is prohibited in the central channel region underneath the suspended bridge owing to the fact that the process pressure is $<10^{-5}$ torr. Under such condition the scattering of the evaporated Al species in the chamber space is negligible.

Transfer curves of a typical ZnO TFT at $V_{DS} = 0.1$ and 3 V are shown in Fig. 3(a). The channel length of ZnO TFT is defined to be the distance between the two Al pads

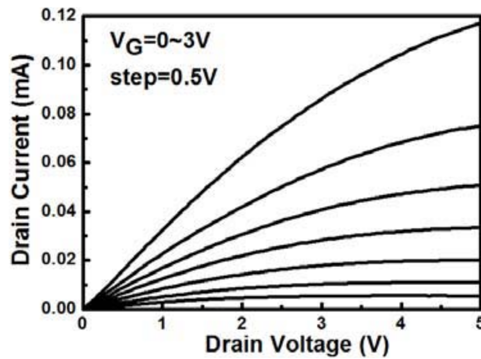

Fig. 4. Output characteristics of a ZnO TFT.

and is measured to be 0.76 μm that is comparable with the planar dimension of the suspending poly-Si bridge. Excellent electrical characteristics are obtained in terms of high ON/OFF current ratio $>10^9$, good mobility value of 41 cm^2/V s, and steep subthreshlod property with swing of 89 mV/decade. The threshold voltage is 0.87 V.

The variation of the device characteristics is also checked by measuring a number of devices on a wafer. Fig. 3(b) shows the transfer curves of five ZnO TFTs located on different dies of the wafer. Negligible differences are found among those characteristics, demonstrating good uniformity is achievable with the present fabrication approach. Fig. 4 shows the well-behaved output characteristics of the device.

IV. Conclusion

A new method employing mature semiconductor process techniques are developed in this letter to fabricate ZnO TFTs featuring submicrometer channel length, self-assembled channel layer, and self-aligned Al S/D contacts. Excellent transfer characteristics were achieved for the fabricated ZnO TFTs with very high ON/OFF current ratio ($>10^9$), low subthreshold swing (89 mV/decade), and high field-effect mobility (41 cm^2/V s). Electrical properties of the manufactured devices are randomly selected from different dies on the wafer evidence, very small variation.

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