



## Investigation of Lateral Trap Position by Random Telegraph Signal Analysis in Moderate Inversion in n-Channel MOSFETs

Ching-En Chen,<sup>a</sup> Ting-Chang Chang,<sup>a,b,c,z</sup> Bo You,<sup>d</sup> Wen-Hung Lo,<sup>b</sup> Szu-Han Ho,<sup>a</sup> Chih-Hao Dai,<sup>d</sup> Jyun-Yu Tsai,<sup>b</sup> Hua-Mao Chen,<sup>e</sup> Guan-Ru Liu,<sup>b</sup> Ya-Hsiang Tai,<sup>e</sup> and Tseung-Yuen Tseng<sup>a</sup>

<sup>a</sup>Department of Electronics Engineering, National Chiao Tung University, Hsin-Chu 300, Taiwan

<sup>b</sup>Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan

<sup>c</sup>Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan 701, Taiwan

<sup>d</sup>Department of Photonics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan

<sup>e</sup>Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsin-Chu 300, Taiwan

This paper investigates the trap position by random telegraph signal (RTS) analysis in moderate inversion in partially depleted silicon-on-insulator n-channel metal-oxide-semiconductor field-effect transistors. In the diffusion current-dominated region, the electron concentration distribution is more non-uniform along the channel than the one in the drift current-dominated region. In the diffusion region, the application of drain (source) voltage can influence the potential at the drain (source) side only. Accordingly, the position of oxide trap can be further clarified using RTS measurements to compare both the capture times as well as the relative channel current amplitudes of devices with and without interchanged source/drain.

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Recently, popular applications of mobile electronic products have included combined display designs,<sup>1-3</sup> memory circuits<sup>4-6</sup> and IC circuits. To accomplish low power consumption and high operation speed, silicon-on-insulator (SOI) technology has been developed in the manufacturing process. However, there are some inherent disadvantages in SOI structure, such as floating body effect (FBE), and self-heating effect.<sup>7-10</sup> With the scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs), random telegraph signal (RTS) have become a major issue that has influenced performance of MOSFETs.<sup>11-17</sup> The RTS phenomenon is commonly related to the behaviors of a carrier that has been captured and emitted by the oxide trap. Additionally, the operating region of MOSFETs is often chosen in the moderate inversion region due to the need for low power consumption in analog circuits. However, RTS in this region also brings in inaccurate output current in analog circuits. Therefore, investigations on RTS in the moderate inversion region have been considerable. The methods for extracting the lateral trap position have been proposed before by several groups.<sup>14,18-20</sup> The operating region for extracting the lateral position of an oxide trap is in linear region where the drift current dominates. However, these methods for determining the lateral trap position are not accurate in the moderate inversion because both the diffusion current and the drift current contribute to the drain current in the moderate inversion. Moreover, a few RTS analysis for trap lateral position in moderate inversion have been reported. Therefore, in this work, the position of the oxide trap is analyzed by channel current RTS without and with interchanged source/drain (forward and reverse operation), indicated as  $I_D$ -RTS and  $I_S$ -RTS, respectively. Then, according to the Shockley-Read-Hall (SRH) model, the position of the oxide trap is clarified. Furthermore, this result can be demonstrated by analysis of the relative amplitude of channel current. Although the relative amplitude of channel current can be influenced by the random dopant fluctuation,<sup>16,21,22</sup> which is the major source of threshold voltage fluctuation as MOSFETs scaled down, the following analysis is valid for devices with the same threshold voltage under forward and reverse operation.

### Experimental

The PD SOI nMOSFETs used in this study were fabricated by 0.13  $\mu\text{m}$  SOI technology. The thickness of silicon film and buried oxide are 0.15  $\mu\text{m}$  and 1  $\mu\text{m}$ , respectively. The gate oxide with thickness of 100  $\text{\AA}$  was grown on silicon film with channel doping concentration

of about  $1.3 \times 10^{18} \text{ cm}^{-3}$ . In this paper, the device has dimensions of width/length = 1  $\mu\text{m}/0.35 \mu\text{m}$ . The IV characteristics and RTS measurements were performed by an Agilent B1500A semiconductor device analyzer, an Agilent B1530A Waveform-Generator/Fast-Measurement-Unit (WGFMU) and a Cascade Microtech M150 measurement platform.

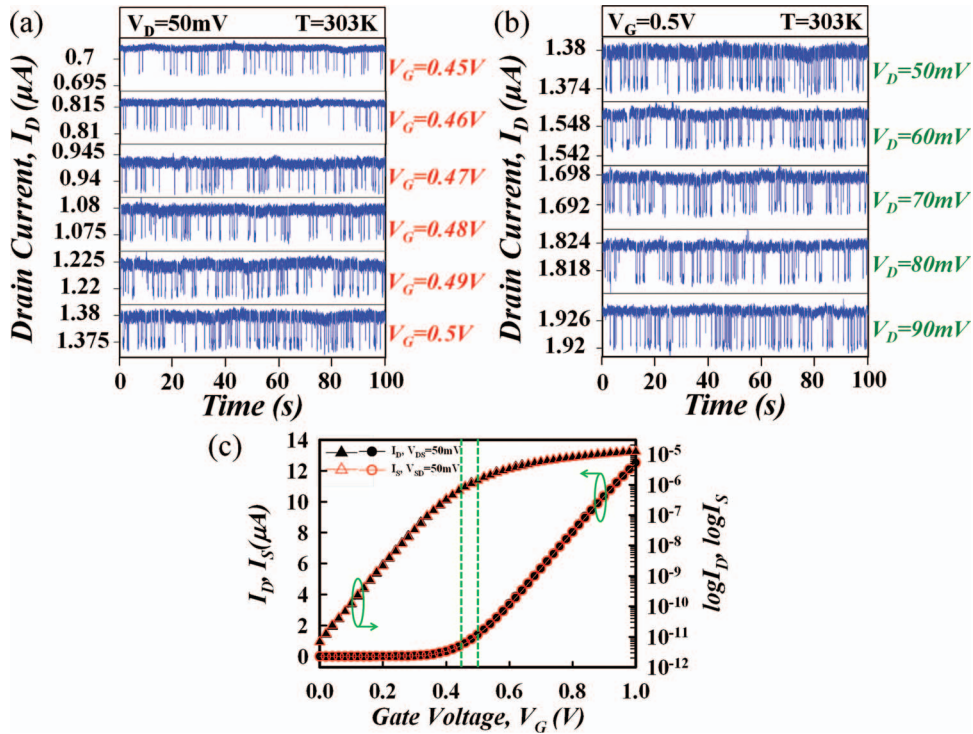
### Results and Discussion

Figure 1a shows the  $V_G$  dependence on  $I_D$ -RTS with  $V_D = 50$  mV for a period of 100 sec. The average time at high current state ( $\langle\tau_1\rangle$ ) decreases as  $V_G$  increases. On the contrary, the average time at low current state increases as  $V_G$  increases. This low current state has been previously shown to be due to both electron trapping and carrier mobility fluctuation.<sup>12-14</sup> In addition, previous research has identified two conditions causing mobility fluctuation through Coulombic scattering, either by a single positively or negatively charged trap.<sup>17</sup> In the presence of either a positive charge only without electron trapping (donor type trap) or a negative charge only due to electron trapping (acceptor type trap), Coulombic scattering will occur. Because a low current state is observed here, this suggests the latter cause. Moreover, because the trap occupancy is observed to increase with  $V_G$  due to an increase in the electron concentration in the channel, this confirms an increase in electron trapping. The low current state and the electron trapping in tandem indicate that the trap is acceptor type.

According to the SRH model,  $\langle\tau_1\rangle$  can be considered as the capture time of oxide traps, and  $\langle\tau_1\rangle$  is inversely proportional to the electron concentration in the channel below the trap, indicated as  $n_c(y_T)$ .  $y_T$  is the distance of the trap from source edge. Fig. 1b shows  $I_D$ -RTS with  $V_G = 0.45$  V for different  $V_D$ . The  $I_D$ -RTS does not obviously vary with  $V_D$ .

Further extraction of  $\langle\tau_1\rangle$  at different  $V_G$  and  $V_D$  is shown in Fig. 2a. Here,  $\langle\tau_1\rangle_f$  represents  $\langle\tau_1\rangle$  under forward operation. Obviously,  $\langle\tau_1\rangle_f$  decreases as  $V_G$  increases due to  $n_c(y_T)$  increasing. As shown in Fig. 1c, the threshold voltage under forward operation ( $V_{th,f}$ ) is identical to the value under reverse operation ( $V_{th,r}$ ), and the region between two vertical dashed lines indicates the  $I_D$ -RTS and  $I_S$ -RTS observation region. In this region between weak and strong inversion, diffusion current dominates ( $I_D$ - $V_G$  curves at different temperatures can demonstrate this, but are not shown here). Figure 2b shows  $\langle\tau_1\rangle$  under reverse operation, indicated as  $\langle\tau_1\rangle_r$ , for different  $V_G$  and  $V_S$ . Similar to  $\langle\tau_1\rangle_f$ ,  $\langle\tau_1\rangle_r$  decreases as  $V_G$  increases. However,  $\langle\tau_1\rangle_r$  is larger than  $\langle\tau_1\rangle_f$  at the same  $V_G$ . This behavior may result from different  $n_c(y_T)$  under forward and reverse operations. For

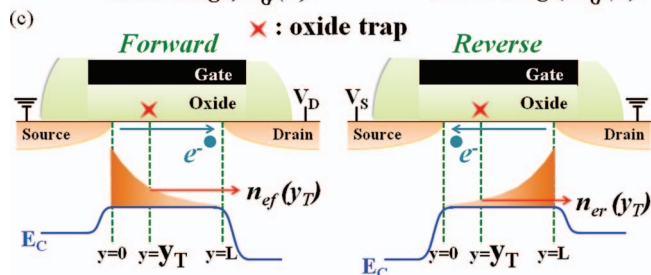
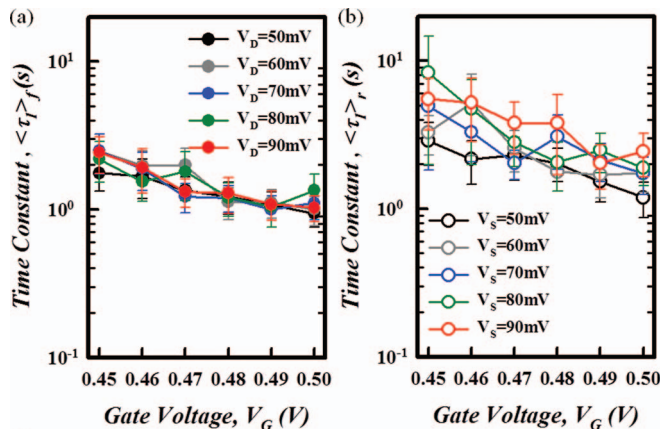
<sup>z</sup>E-mail: tcchang@mail.phys.nsysu.edu.tw



**Figure 1.** Time domain  $I_D$ -RTS evolution for (a)  $V_D = 50$  mV and different  $V_G$  from 0.45 V to 0.5 V and (b)  $V_G = 0.5$  V and different  $V_D$  from 50 mV to 90 mV. (c)  $I_D$ - $V_G$  ( $I_S$ - $V_G$ ) curves for  $V_{DS} = 50$  mV ( $V_{SD} = 50$  mV), with the two vertical dashed lines corresponding to  $V_G = 0.45$  V and  $V_G = 0.5$  V.

further analysis, the electron concentration distributions and energy band diagrams under forward and reverse operation are shown in Fig. 2c. The parameters  $n_{ef}(y_T)$  ( $n_{er}(y_T)$ ) are the electron concentration in channel below the trap under forward (reverse) operation.

In the example given in this figure, because it is assumed that the trap is near source side,  $n_{ef}(y_T)$  will be larger than  $n_{er}(y_T)$ . Because  $\langle\tau_1\rangle$  is inversely proportional to  $n_e(y_T)$ ,  $\langle\tau_1\rangle_f$  is therefore smaller than  $\langle\tau_1\rangle_r$ . This phenomenon is similar to the experiment results in Fig. 2a and 2b. Therefore, these results suggest that the trap is near the source side.



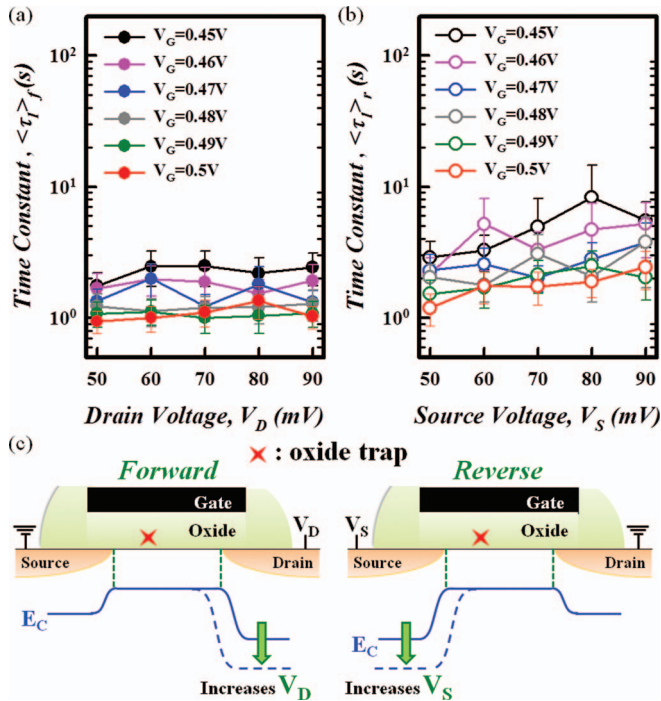
**Figure 2.** (a)(b) The value of  $\langle\tau_1\rangle_f$  ( $\langle\tau_1\rangle_r$ ) versus  $V_G$  in the range of  $V_D$  ( $V_S$ ) from 50 mV to 90 mV. (c) Schematic of electron concentration distribution and energy band diagram under forward (reverse) operation in moderate inversion, assuming that oxide trap is near source side.

In Fig. 3a,  $\langle\tau_1\rangle_f$  does not obviously vary with  $V_D$ . However,  $\langle\tau_1\rangle_r$  increases as  $V_S$  increases for different  $V_G$ , shown in Fig. 3b. Since channel current RTS is very sensitive to a local channel potential change near the trap as well as  $n_e(y_T)$ ,  $\langle\tau_1\rangle_r$  changing with  $V_S$  can be attributed to the fact that the position of the trap is near the source side. As shown in Fig. 3c, the depletion region near the drain side extends toward the channel as  $V_D$  increases, but the local channel potential is unaffected at the position of the trap. However, as  $V_S$  increases, the depletion extension is near the source side and thereby affects the local potential near the trap, as well as affecting  $n_e(y_T)$ . Since  $\langle\tau_1\rangle_r$  increases as a result of  $n_e(y_T)$  decreasing when  $V_S$  increases, the position of the trap can be verified to be near the source side, as has been demonstrated by channel current RTS measurements in moderate inversion under forward and reverse operation.

An analysis of relative amplitude of channel current is helpful to further demonstrate the trap position. The relative amplitude of  $I_D$  is given by<sup>12</sup>

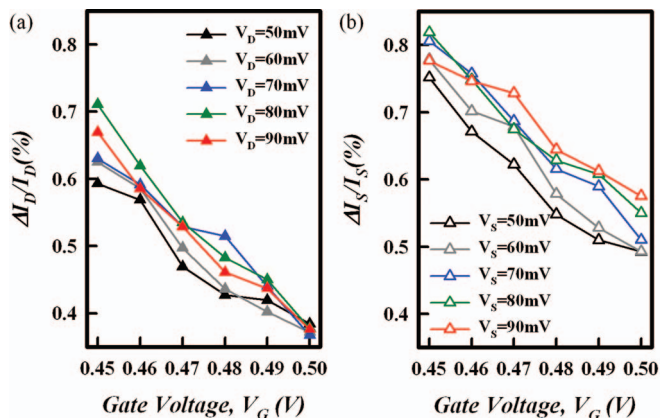
$$\frac{\Delta I_D}{I_D} = \frac{1}{W L} \left( \frac{1}{N_S} \pm \alpha_{SC} \mu \right) \quad [1]$$

where  $N_S$  is the density of channel carriers per unit area,  $\alpha_{SC}$  is the scattering coefficient,  $\mu$  is the carrier mobility, and  $W$  and  $L$  are the device channel width and length.  $\alpha_{SC}$  is a function of carrier density. The first term in Eq. 1 is the number fluctuation and the second term is the mobility fluctuation. Although Eq. 1 diverges in weak inversion where  $N_S$  goes to zero,  $N_S$  increases as  $V_G$  increases from weak inversion to moderate inversion. Moreover, there is one thing of note. For the quantitative analysis, Eq. 1 is an over-simplification of the relative amplitude of channel current. Here, a qualitative comparison of the relative amplitude values between forward and reverse operation are



**Figure 3.** (a)(b)The value of  $\langle \tau_1 \rangle_f$  ( $\langle \tau_1 \rangle_r$ ) versus  $V_D$  ( $V_S$ ) in the range of  $V_G$  from 0.45 V to 0.5 V. (c) Schematic of energy band diagram under forward (reverse) operation for increasing  $V_D$  ( $V_S$ ) in moderate inversion. It is assumed that oxide trap is near source side.

presented. The  $\pm$  sign in Eq. 1 depends on the type of scattering center. The + sign applies for a charged trap when filled (i.e., acceptor in nMOSFETs). The - sign applies for a neutral trap when filled (i.e., donor in nMOSFETs). Since the trap is an acceptor type in nMOSFETs, the + sign applies in Eq. 1. For further analysis, the relative amplitude of drain (source) current is investigated with different  $V_G$  and  $V_D$  ( $V_S$ ) under forward (reverse) operation, indicated as  $\Delta I_D/I_D$  ( $\Delta I_S/I_S$ ). As shown in Fig. 4a and 4b, both  $\Delta I_D/I_D$  and  $\Delta I_S/I_S$  decrease as  $V_G$  increases. This behavior is because carrier density increases as  $V_G$  increases, and then both  $1/N_S$  and  $\alpha_{SC}$  decrease as carrier density increases. However,  $\Delta I_S/I_S$  is larger than  $\Delta I_D/I_D$  for the same  $V_G$ . This



**Figure 4.** (a)(b)The value of  $\Delta I_D/I_D$  ( $\Delta I_S/I_S$ ) versus  $V_G$  under forward (reverse) operation. The value of  $\Delta I_S/I_S$  is larger than  $\Delta I_D/I_D$  at the same  $V_G$ . According to the SRH model, this behavior can be attributed to the position of oxide trap being near the source side.

can be attributed to the trap being near the source side, and therefore  $n_{er}(y_T)$  being larger than  $n_{er}(y_r)$ , as shown in Fig. 2c. If  $n_{er}(y_T)$  is in fact larger than  $n_{er}(y_r)$ , both  $1/N_S$  and  $\alpha_{SC}$  under reverse operation will be larger than under forward operation, and cause  $\Delta I_S/I_S$  to be larger than  $\Delta I_D/I_D$ . This comparison of  $\Delta I_D/I_D$  and  $\Delta I_S/I_S$  at the same  $V_G$  further confirms that the trap is located at the source side.

## Conclusions

This paper studies channel current RTS in moderate inversion in PDSOI nMOSFETs. It shows that  $\langle \tau_1 \rangle_r$  is larger than  $\langle \tau_1 \rangle_f$ . According to the SRH model, this result suggests that the position of the oxide trap is near the source side. Further,  $\langle \tau_1 \rangle_f$  is almost constant as  $V_D$  increases because  $n_{er}(y_T)$  is unchanged. However, with increased  $V_S$ ,  $\langle \tau_1 \rangle_r$  increases due to decrease in  $n_{er}(y_T)$ . This phenomenon can be attributed to the position of the trap near source side. In addition, by comparing  $\Delta I_D/I_D$  and  $\Delta I_S/I_S$  at different  $V_G$ , the position of the trap is further confirmed to be near the source side. Consequently, for the RTS in moderate inversion, the trap position near either source or drain sides can be demonstrated through comparisons of  $\langle \tau_1 \rangle$  and relative amplitude of channel current between forward and reverse operation with different  $V_G$  and lateral biases.

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## References

1. K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Nature*, **432**, 488 (2004).
2. C. T. Tsai, T. C. Chang, S. C. Chen, I. Lo, S. W. Tsao, M. C. Hung, J. J. Chang, C. Y. Wu, and C. Y. Huang, *Appl. Phys. Lett.*, **96**, 242105 (2010).
3. T. C. Chen, T. C. Chang, C. T. Tsai, T. Y. Hsieh, S. C. Chen, C. S. Lin, M. C. Hung, C. H. Tu, J. J. Chang, and P. L. Chen, *Appl. Phys. Lett.*, **97**, 112104 (2010).
4. T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, *Mater. Today*, **14**, 608 (2011).
5. M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, *Appl. Phys. Lett.*, **96**, 262110 (2010).
6. Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, *IEEE Electron Device Lett.*, **32**, 545 (2011).
7. J. P. Colinge, *IEEE Electron Device Lett.*, **9**, 97 (1988).
8. L. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, *IEEE Trans. Electron Devices*, **41**, 69 (1994).
9. C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. C. Tsai, S. H. Ho, W. H. Lo, G. Xia, O. Cheng, and C. T. Huang, *IEEE Electron Device Lett.*, **31**, 540 (2010).
10. W. H. Lo, T. C. Chang, C. H. Dai, W. L. Chung, C. E. Chen, S. H. Ho, O. Cheng, and C. T. Huang, *IEEE Electron Device Lett.*, **33**, 303 (2012).
11. M. J. Kirton and M. J. Uren, *Adv. Phys.*, **38**, 367 (1989).
12. K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, *IEEE Trans. Electron Devices*, **37**, 654 (1990).
13. C. E. Chen, T. C. Chang, H. P. Lo, S. H. Ho, W. H. Lo, T. Y. Tseng, O. Cheng, and C. T. Huang, *ECS Trans.*, **45**, 261 (2012).
14. H. C. Ma, Y. L. Chou, J. P. Chiu, Y. T. Chung, T. Y. Lin, T. Wang, Y. P. Chao, K. C. Chen, and C. Y. Lu, *IEEE Trans. Electron Devices*, **58**, 623 (2011).
15. B. Oh, H. J. Cho, H. Kim, Y. Son, T. Kang, S. Park, S. Jang, J. H. Lee, and H. Shin, *IEEE Trans. Electron Devices*, **58**, 1741 (2011).
16. A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, *IEEE Trans. Electron Devices*, **50**, 839 (2003).
17. Z. Shi, J. P. Mieveille, and M. Dutoit, *IEEE Trans. Electron Devices*, **41**, 1161 (1994).
18. P. Restle and A. Gnudi, *IBM J. Res. Develop.*, **34**, 227 (1990).
19. Z. Çelik-Butler, P. Vasina, and N. V. Amarasinghe, *IEEE Trans. Electron Devices*, **47**, 646 (2000).
20. D. Kang, J. Kim, D. Lee, B. G. Park, J. D. Lee, and H. Shin, *Jpn. J. Appl. Phys.*, **48**, 04C034 (2009).
21. K. Sonoda, K. Ishikawa, T. Eimori, and O. Tsuchiya, *IEEE Electron Device Lett.*, **54**, 1918 (2007).
22. K. Sonoda, M. Tanizawa, K. Ishikawa, and Y. Inoue, *Int. Conf. Simulation of Semiconductor Processes and Devices (SISPAD)*, 19 (2011).