The TEOS CVD Oxide Deposited on Phosphorus *In Situ* Doped Polysilicon with Rapid Thermal Annealing

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***Abstract*— A TEOS oxide deposited on the phosphorus *in situ* doped polysilicon annealed with RTA is shown to have good electrical characteristics such as a high breakdown field (>12 MV/cm), especially for the positive bias, and a large Qbd (26 Coul/cm^2). The improvement is believed to be due to the relatively smooth surface of the *in situ* doped polysilicon and the reduction of the trapping density by RTA.**

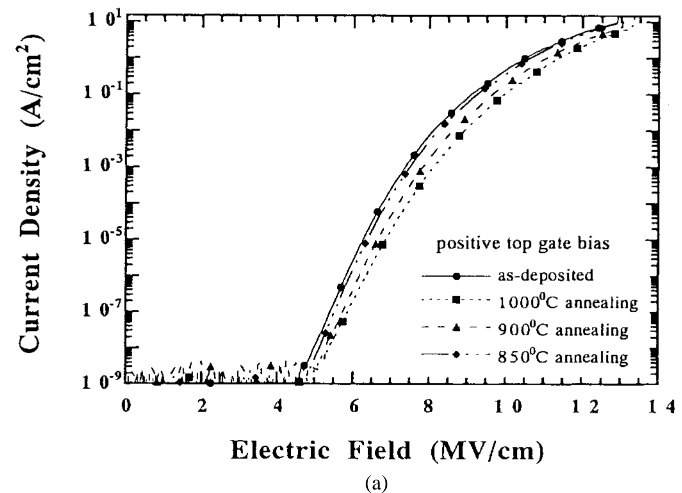
I. Introduction

For nonvolatile memories such as EPROM, EEPROM, and Flash, thermal oxides grown on n^+ polysilicon (polyoxides) have been used as the interdielectrics. However, polyoxides have drawbacks of a lower dielectric strength and a higher leakage current than oxides grown on single crystal silicon due to asperities (surface roughness) caused by the enhanced oxidation at grain boundaries. Also, the characteristics of polyoxides are heavily dependent on the structure and morphology of the predeposited-polysilicon film, which in turn are affected by the process parameters [1], [2]. ONO polyoxides are thus used for the inter-polyoxides and show good charactristics [3], [4]. However, due to the intrinsic multiple layer structure, they face a rather difficult scaling down problem [4].

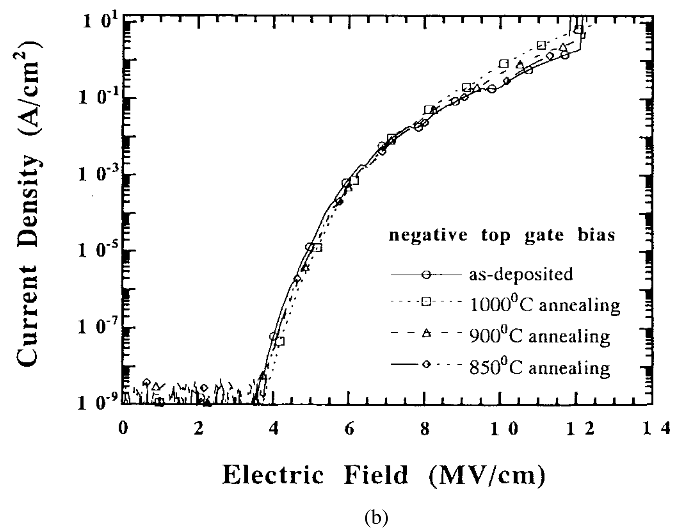
In this letter, we report a TEOS CVD oxide to be a possible candidate for the inter-polyoxide. The oxide is deposited on the phosphorus *in situ* doped polysilicon which has a relatively flat and smooth surface [5], [6], and the CVD deposition makes the grain boundaries of the bottom polysilicon not propagate into the deposited polyoxide film as that which occurs in the thermal polyoxides [6]. The prepared TEOS CVD polyoxide has desirable characteristics such as an asymmetric J-E characteristic and a large charge-to-breakdown (Qbd ~26 Coul/cm^2).

II. Experiments

P-type wafers were first thermally oxidized to have an oxide of a thickness of 100 nm, then, a 300 nm phosphorus *in situ* doped polysilicon film (poly1) was deposited at 580 °C with the sheet resistance to be 44 Ω/cm. A LPCVD TEOS oxide of 13 nm was then deposited at 700 °C and rapidly annealed in N_2 ambient at temperatures of 850, 900, and 1000 °C for 30 s. A second polysilicon film (poly2) of 300 nm, also *in situ* doped with phosphorus, was deposited at 580 °C. After poly2 was patterned, another oxide of 100 nm was grown and contact holes were opened and metallized to form the capacitor



(a)



(b)

Fig. 1. The J-E characteristics of the deposited TEOS oxides annealed at different temperatures (850, 900, and 1000 °C) for the top gate (a) positive bias and (b) negative bias.

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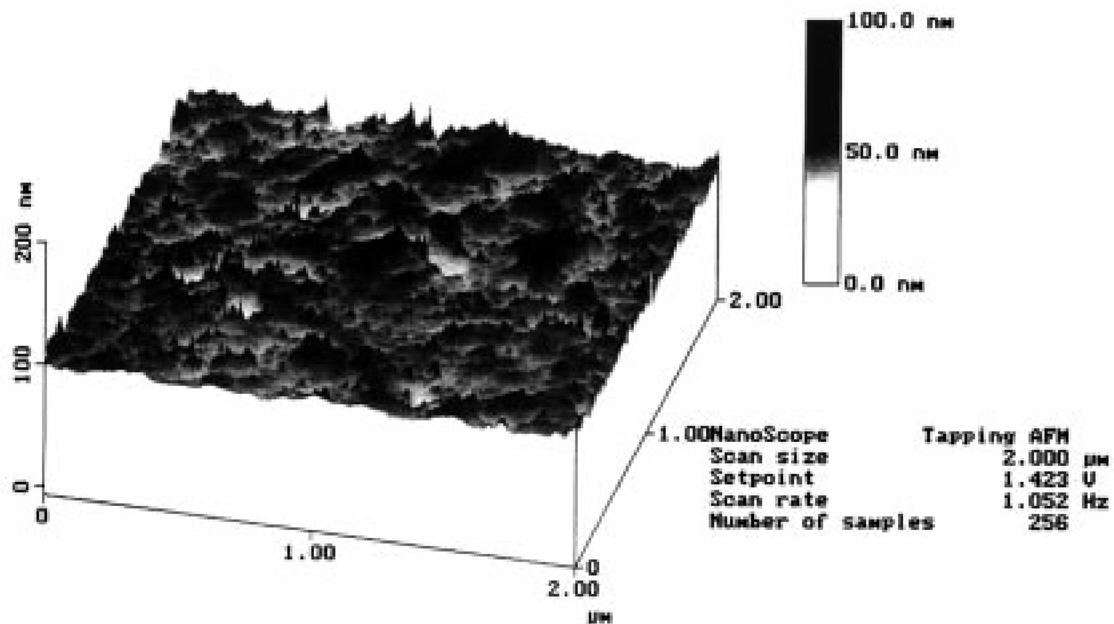
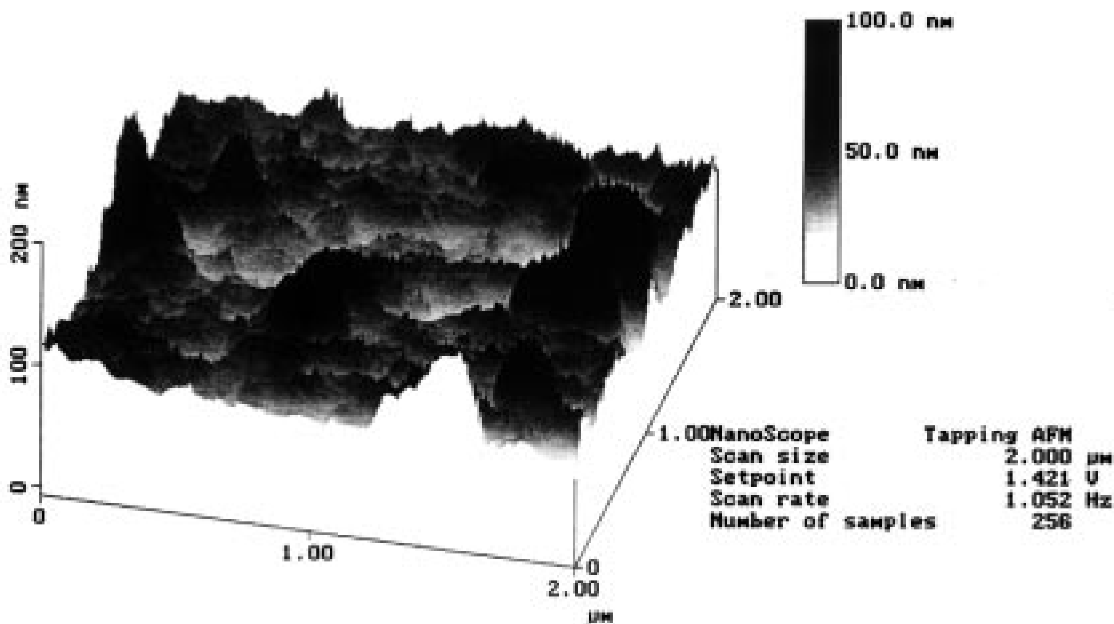


(a)



(b)

Fig. 2. The AFM (atomic force microscope) images of the surface of the polysilicon films doped with (a) phosphorus *in situ* (580 °C) and (b) POCl3 (950 °C).

structure. Finally, all devices were sintered at 350 °C for 40 min in the N_2 gas.

III. Results and Discussion

Fig. 1(a) and (b) shows the positive (gate positive) and the negative J-E characteristics of oxides annealed at temperatures of 850, 900, and 1000 °C, respectively. It can be seen that both J-E characteristics had breakdown fields over 12 MV/cm and the positive J-E characteristics had lower currents and even higher breakdown fields. These high breakdown fields are due to smooth polysilicon1/polyoxide and polyoxide/polysilicon2 interfaces [7], [8]. This can be seen from Fig. 2(a) which shows the AFM (atomic force microscope) image of the surface of the phosphorus *in situ* doped polysilicon, which can be compared with that of the same polysilicon but doped with POCl3 as shown in Fig. 2(b). We can see that Fig. 2(a) has a much smoother surface. In Fig. 1(a), it is also seen that as the annealing temperature was increased, the current and the breakdown field were improved for the positive J-E characteristics.

Fig. 3 shows the gate voltage change for samples under a 10 μA/cm^2 constant current stress. The electron trapping

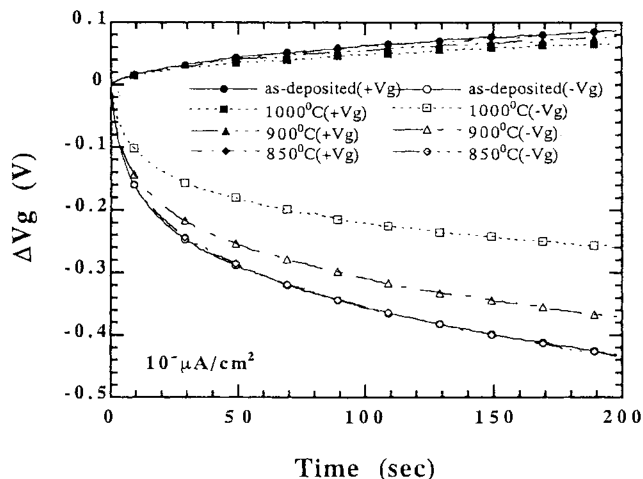


Fig. 3. The incremental voltage shifts of deposited TEOS oxides annealed at different temperatures under positive and negative constant current stress of 10 μA/cm^2. The gate area was 5×10^{-4} cm^2.

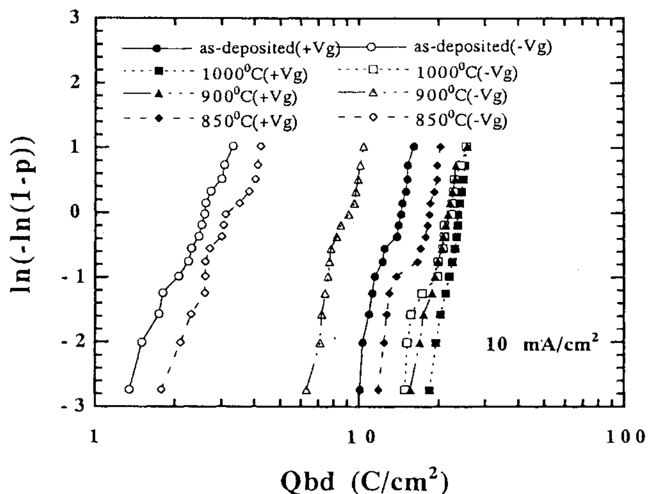


Fig. 4. The Weibull charge-to-breakdown plots for TEOS oxides annealed at different temperatures under positive and negative stress, respectively. The stress condition was 10 mA/cm^2 and the gate area was 5×10^{-4} cm^2.

rate under the $-Vg$ bias was larger than that under the $+Vg$ bias. The annealing temperature had a remarkable effect on improving the trapping rate for the $-Vg$ bias. Fig. 4 shows the Weibull charge-to-breakdown (Qbd) plots for the above samples under the 10 mA/cm^2 stress. All the $+Vg$ stressed samples had higher Qbd's than the corresponding $-Vg$ stressed samples, and the higher annealing temperature, the higher Qbd. The improvement was believed to be due to reducing electron trapping sites by RTA's. In addition, the plots also show that as the annealing temperature increased, the polarity asymmetry became smaller. The 1000 °C annealed sample had the largest Qbd ($+Vg$: 26 Coul/cm^2; $-Vg$: 23 Coul/cm^2) while the smallest polarity asymmetry.

IV. Conclusion

We conclude that the TEOS CVD oxide deposited on the phosphorus *in situ* doped polysilicon annealed with RTA is a very attractive inter-dielectric, which has a high breakdown field, low leakage current for the positive bias, and very large Qbd (26 Coul/cm^2) than conventional thermally grown or CVD deposited dielectrics.

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