PAPER
Well-Structured Modified Booth Multiplier and Its Application to Reconfigurable MAC Design

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SUMMARY This paper presents a well-structured modified Booth encoding (MBE) multiplier which is applied in the design of a reconfigurable multiply-accumulator (MAC) core. The multiplier adopts an improved Booth encoder and selector to achieve an extra-row-removal and uses a hybrid approach in the two's complementation circuit to reduce the area and improve the speed. The multiplier is used to form a 32-bit reconfigurable MAC core which can be flexibly configured to execute one 32×32, two 16×16 or four 8×8 signed multiply-accumulation. Experimentally, when implemented with a 130 nm CMOS single-V_t standard cell library, the multiplier achieved a 15.8% area saving and 11.7% power saving over the classical design, and the reconfigurable MAC achieved a 4.2% area and a 7.4% power saving over the MAC design published so far if implemented with a mixed-V_t standard cell library.

key words: *multiplier, multiply-accumulator, modified Booth encoding, reconfigurable, mixed-V_t, standard cell library*

1. Introduction

Multiplication and multiplication-accumulation are the very common mathematical operations in many Digital Signal Processing (DSP) applications. Hardware implementations of high-speed and low-power multipliers have attracted much research attention [1]–[9]. Parallelism in partial products is the most common approach used in those architectures to achieve the high speed and low power. There are two common techniques to exploit parallelism in enhancing the multiplication performance: The first is to reduce the number of partial product (PP) rows: for examples, [1]–[6] use the MBE [10] scheme to half the number of PP rows. The second is to adopt the carry-save-tree technique to reduce the multiple PP rows into two "carry-save" redundant forms [1]–[3], [5]–[7], [9], [11], [12]. The examples of this approach are: [1] and [9] find an optimal partial products reduction or a compressors tree by carefully modeling the delay paths of a counter; [2] saves one stage of carry save adders (CSA) by removing extra signed row with a tree type two's complementation logic; [5], [11] compress the sign-extension bits by merging the signs of the partial products with the multiplicand, removing the sign-extension bits from the critical path of partial product reduction tree (PPRT); and [12] rearranges the positions of signed carries to reduce the hardware of carry-save additions.

Many DSP applications involve large amounts of data-level parallelism operated on the low-precision operands. For those applications, reconfigurable multiplier/MAC architectures were proposed to facilitate more flexible multiplication for complex single instruction multiple data (SIMD) processing [13], [14]. For example, in [13], a sub-word parallel method was presented based on the Baugh-Wooly algorithm for generating of PPs using signed operands without using blocking carries to cross sub-word boundaries. This method has a disadvantage, i.e., the multiplication is realized by array multipliers and the number of PP rows equals the input-width of the multiplier, leading to a large number of adding stages. In [14], a vectorized MAC architecture was proposed based on the MBE scheme to use a "shared-segmentation" method to support multiple mode selection. However, this multiplier has one extra PP row due to the negative increment, leading to the requirement of one extra carry-save-adding stage in the final summation step.

This paper presents an improved MBE multiplier design which rearranges and reduces partial products by an improved modified Booth encoder and selector. This reduces the gate count and improves performance of the multiplier. The design also uses a spare-tree structure in extra-row removing to further reduce the area of two's complementation circuit. In addition, the design adopts a hybrid-structured two's complementation logic, taking the advantage of the uneven arrival time of inputs, to reduce furthermore the area and power consumption of the multiplier. The multiplier is then applied to design a reconfigurable MAC, which can serve as an embedded core in a chip. The MAC can be configured to compute for one 32×32, two 16×16 or four 8×8 signed multiplication-accumulation operation. Since for this reconfigurable MAC, fewer PP rows are used and many common functions are shared, it is smaller in the size, faster in the speed and consumes less power as compared to the conventional MAC [14].

The rest of this paper is structured as follows: Sect. 2 describes the conventional MBE multipliers, with emphasis on the improvements provided by the proposed well-structured MBE multiplier. Section 3 describes the architectural design of the proposed well-structured MBE multiplier. Section 4 describes the application of this design to the reconfigurable MAC and Sect. 5 addresses the implementation results and evaluates the effect of the well-structured MBE multiplier on the reconfigurable MAC performance. Finally, Sect. 6 gives a conclusion.

2. Review of Modified Booth Multiplier

In order to describe the proposed modified Booth multiplier, the modified Booth multiplier is firstly reviewed. Figure 1 is the block diagram of an n-bits parallel modified (radix-4) Booth MAC design that computes $R = X \times Y + Z$, where $X = (x_{n-1}, \ldots, x_1, x_0)$ is the multiplicand, $Y = (y_{n-1}, \ldots, y_1 y_0)$ is the multiplier and $Z = (z_{2n-1}, \ldots, z_1, z_0)$ is the accumulated datum. The multiplier consists of an MBE partial product generator (PPG), a PPRT and a final carry-propagate adder (CPA). In the MBE mechanism, Y is segmented into groups of three bits $(y_{2i+1}, y_{2i}, y_{2i-1})$ which encoded to be one of $\{-2, -1, 0, 1, 2\}$ values. Based on the encoded value, the Booth selector chooses the multiples of multiplicand to generate PPs. In Fig. 1, PP terms (a.k.a. PP bits) are summed by CSA -based PPRT without carry propagation. In a MAC design, the accumulated datum Z is fed into the PPRT, increasing the carry-save-adding delay by no more than one extra stage. Finally, the summed results are added by a CPA.

For a given partial product, if a negative two (-2) or a negative one (-1) for the multiplicand is asserted, the multiplicand must be two's complemented, for which it inverts the multiplicand and generates a signed-carry output called "hot-one" $(h1)$. Therefore, one $h1_i$ for the i-th PP row will be appended to the least significant bit (LSB) of the $(i+1)$-th row, as shown in Fig. 2(a), where an 8×8 signed multiplication is taken as an example. In the array of Fig. 2(a), as well as that of Fig. 2(b), a_j, b_j, c_j and d_j represent the j-th partial product bit of each row respectively. However, fully sign-extending the sign bit to the $(2n-1)$-th position of each row makes PP rows unequal in length and the addition of extended signs is very costly. In a sign-encoding technique [11], the negatively weighted most significant bits (MSB) are replaced by $\{\overline{s_i}, s_i, s_i\}$ for the first row, $\{1, \overline{s_i}\}$'s for the remaining rows and $\{\overline{s_i}\}$ for the last row, where s_i is the MSB of the i-th partial product row.

An approach in [1] produces a more regular partial product array by integrating the logic functions of $h1_i$ and the LSB of the i-th PP row and by rearranging the bits to specified positions. Therefore, the original LSB and $h1_i$ are replaced by a newly formed LSB (κ_i) and a hot-two $(h2_i)$ signal for each row as shown in the right-hand of Fig. 2(b). In this way, although the number of bits is not reduced, the number of additions is reduced. Furthermore, a technique reported in [12] utilizes a reduced PP array which has fewer sign-extension bits for each row as shown at the left-hand side of Fig. 2(b), reducing the number of additions. However, for this scheme, the last extra signed carry requires one extra carry-save-addition before the final summation. Hence, in [2], a method was proposed to produce the two's complement of the multiplicand and the other PPs concurrently to remove this extra hot carry. The $(n+1)$-bits PP terms of the last row is replaced with the $(n+2)$-bits two's complemented PP terms without the last signed carry generation. The MSB of the last row is inverted $(\overline{p_9})$ and added by "1" directly to the position left to the MSB of the row above the last row to restore the correct value. This is also shown in Fig. 2(b).

Based on the above three methods, we present a well-structured multiplier as shown in Fig. 2(b). The detail logic design will be addressed in the following section. In addition to the speed-up due to the elimination of addition steps, the well-structured multiplier has another benefit, i.e., if it has a size of power of 2, it can achieve an even better speed performance and modularity by using the 4-2 compressors (4-2-Cs) configuration.
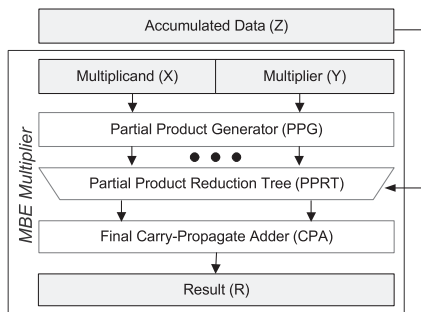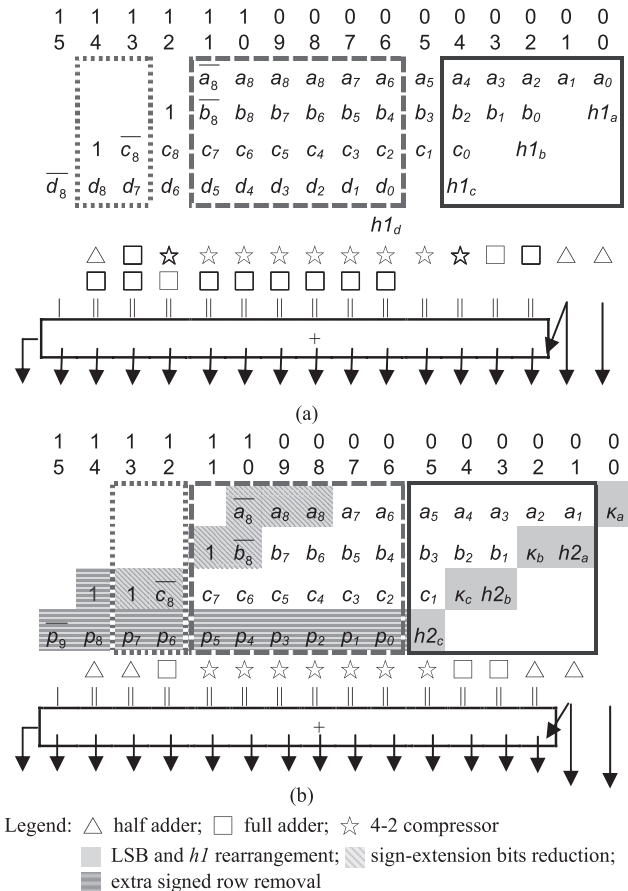

Fig. 1 Block diagram of a modified Booth MAC core.

Fig. 2 Partial product reduction tree for 8×8 signed multiplication with MBE scheme (a) traditional sign-encoding method, and (b) the proposed method.

3. The Proposed Well-Structured Multiplier

This section describes the architecture and circuit design of the proposed well-structured MBE multiplier. A sign-select Booth encoder and selector are used to make the array more regular and a two's complementation circuit is invented to remove the extra row of Fig. 2(a), so that both area and speed of the multiplier are improved.

3.1 Partial Product Generation Unit

Figure 3 illustrates the conventional modified Booth PPG unit [2]. The conventional modified Booth selector computes the j-th partial product bit in the i-th row ($PP_{i,j}$) according to the equation:

$$PP_{i,j} = \left(x_j \cdot M1_i + x_{j-1} \cdot M2_i\right) \oplus NEG_i \tag{1}$$

where x_j and x_{j-1} are the multiplicand inputs of weight 2^j and 2^{j-1} bits respectively. $M1$ and $M2$ determine whether the multiplicand should be doubled, and NEG is a digit that determines whether the multiplicand should be inverted. Also, the logic function to generate $h1$, i.e., NEG, are given in (2)

$$h1_i = NEG_i = \overline{(y_{2i-1} \cdot y_{2i}) + \overline{y_{2i+1}}} \tag{2}$$

In the proposed (sign-select) modified Booth selector, we adopt an extra positive sign signal, POS, to simplify the equation,

$$PP_{i,j} = (x_j \cdot POS_i + \overline{x}_j \cdot NEG_i) \cdot M1_i$$
$$+ (x_{j-1} \cdot POS_i + \overline{x_{j-1}} \cdot NEG_i) \cdot M2_i \tag{3}$$

where

$$POS_i = \overline{\overline{(y_{2i-1} + y_{2i})} + y_{2i+1}} \tag{4}$$

In this way, XOR gates in the Booth selector are removed and the depth of the logic path is reduced. Furthermore, the logic equations of κ_i and $h2_i$ in Fig. 2(b) can be derived as:

$$\kappa_i = x_0 \cdot M1_i = \overline{\overline{x_0} + M2_i} \tag{5}$$
$$h2_i = x_0 \cdot N2_i + \overline{x_0} \cdot NEG_i \tag{6}$$

The schematic of the proposed encoder and selector are shown in Fig. 4 respectively. For this structure, to generate κ and $h2$ for each row requires one NOR gate, one
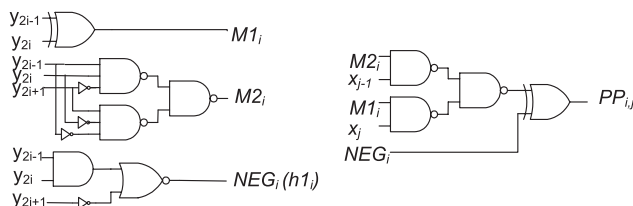
AOI gate and one INV gate, rather than a single Booth selector to generate $h1_i$ in the conventional design [2], which is also drawn in Fig. 4. Furthermore, according to Gajski's model [15], which is the delay model often used such as in [2], our sign-select modified Booth selector is smaller and faster than the conventional modified Booth encoder [2] or the MBE scheme proposed in [1].

In Fig. 4, the 3-4 encoder and the 5-1 selector, which is the last row selection unit, produce the $(n+2)$-bit two's complementation PP row (i.e. the signals $p_0 \sim p_9$ of Fig. 2(b)). For the 5-1 selector, the selector chooses the value from possible inputs which come either from the multiplicand itself (i.e., $P1$ or $P2$, when they are asserted) or two's complement logic (i.e., $N1$ or $N2$, when they are asserted), depending on the result of the 3-4 encoder. In the figure, w_j and w_{j-1} are from the outputs of two's complementation logic of weight 2^j and 2^{j-1} bits respectively, which is shown in Fig. 4. If none of $P1$, $P2$, $N1$, $N2$ is asserted, the 5-1 selector produces a "0" for bit p_j. The two's complementation operation is executed in parallel with the sign-select modified Booth encoder and the 3-4 encoder.

3.2 Hybrid Two's Complementation Logic

A hybrid two's complementation circuit is used to remove the extra signed row of Fig. 2(a) to save the area. Although the idea is similar to that of [2], the circuit is improved to have faster speed. It is explained as follows:

At first, the Sklansky parallel prefix tree [2] of the two's complementation logic is shown in Fig. 5(a). This network can finish two's complementation of a binary number in a logarithmic time $O(\log_2 n)$ [2]. However, one drawback of the this network is that the fan-out of each intermediate prefix-computing gate doubles at each level, making it require a large numbers of OR gates and wires for wide two's complement computation. To overcome this drawback, we
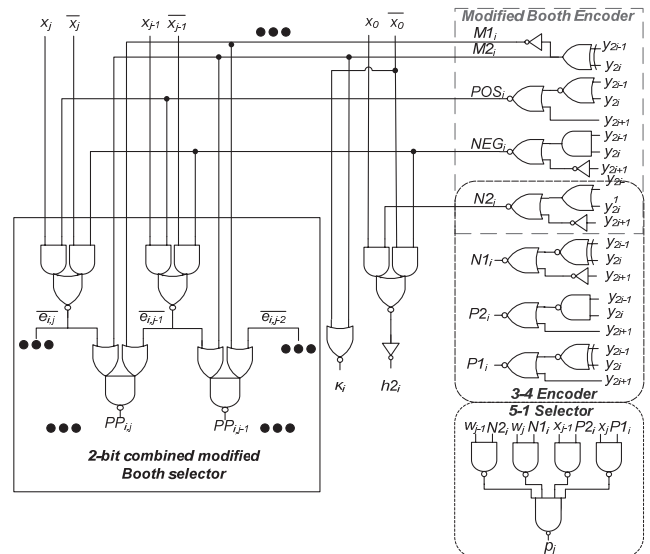

Fig. 3 Conventional modified Booth partial product generation unit.

Fig. 4 Proposed modified Booth partial product generation unit.

adopt a "hybrid" approach that is based on the signal arrival delay analysis of the final CPA. Figure 6 shows the output arrival-profile of the PPRT of the 16-bit MBE multiplier. The PPRT is built up with only FAs and 4-2-Cs compressor elements and the delay of the 4-2-C compressor element is counted to be 1.5 delay count [9]. The profile is the com-

(a)

(b)

Legend: ● OR gate and ⊙ XOR gate

Fig. 5 General models of a 16-bit two's complementation logic, (a) Sklansky network, and (b) the proposed hybrid network of an 8-bit VINC network cascaded with an 8-bit Sklansky network.

Fig. 6 Partial product reduction tree delay profiles of 16-bit MBE multipliers network.

pressors delay (i.e. FAs delay) difference between the earliest and the latest arriving at the network outputs which are the CPA inputs. Figure 6 indicates the critical paths of this network lie on the paths of bits 12-19. The signals arriving at the paths of bits other than these bits take less time to propagate to the network outputs. Hence, we design the 16-bit two's complementation logic to be made up of two segments, i.e., segment ($w_8 - w_{15}$) that we call VINC (variable group-length increment) network, has one extra level of OR gates but on the non-critical path, and another segment ($w_0 - w_7$) which is a network same as the original Sklansky network (Fig. 5(b)) and is on the critical path. However, for the latter segment network, the number of fan-out of G_7 gate that dominates the most critical path is reduced dramatically. This structure decreases the loading of G_7 gate and shortens the delay of the network significantly. Hence, partial products on the critical path are computed rapidly. Moreover, this improved hybrid structure needs fewer number of OR gates than does the original Sklansky structure.
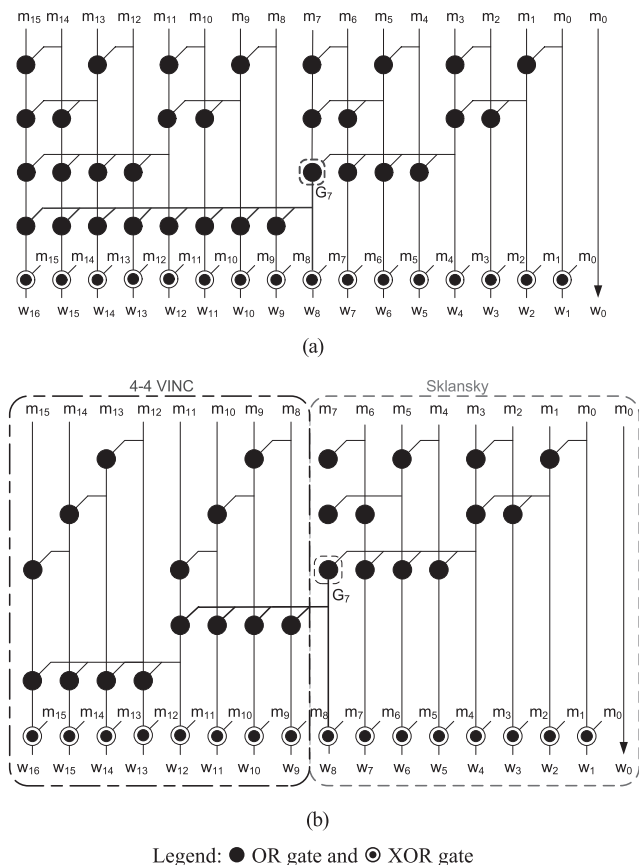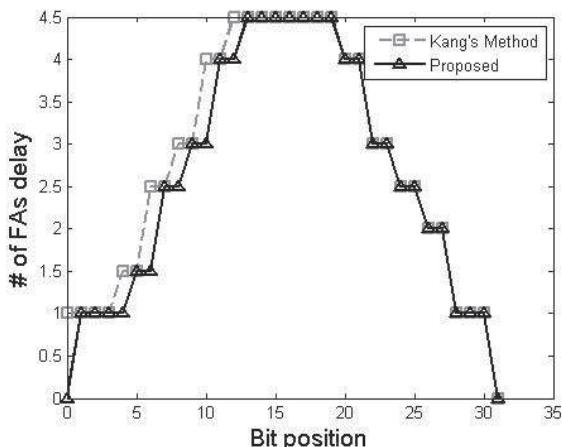
3.3 Hardware Reduction and Performance Improvement

The adoption of the sign-select PPG and hybrid two's complementation logic together with the well- structured partial product array reduces the hardware and improves the performance. A more detailed discussion can be explained with the aid of Table 1, for which PP rows and PP terms for the conventional schemes and the proposed scheme are shown. For the conventional designs, the number of the PP rows is ($\lceil n/2 \rceil + 1$) but for our proposed design it is $\lceil n/2 \rceil$ where n is the word length. The number of PP terms for our proposed scheme is ($\lceil n/2 \rceil (n + 3) + 1$) and is small than conventional schemes. For example, for the design of [5], the number of PP terms is ($\lceil n/2 \rceil - 1$) larger than our proposed design. Furthermore, reducing the number of carry-save addition bits of a column can speed-up the operation of PPRT. Although the number of PP terms is equal to the design of [2], our proposed design has a more regular PPRT. For example, in the array of [2] as shown in Fig. 2(a), the first column with three PP terms occurred at the 2-nd column and requires an FA to do ADD operation. This FA also produces a carry to the next CSA. However, in the proposed method as shown in Fig. 2(b), this ADD operation occurs at the 3-rd column which has three PP terms: a_3, b_1, and $h2_b$. This means that the first ADD operation executed by the FA has moved one bit toward the MSB direction in our design. This behavior improves the speed a little bit and saves the hardware due to its more regular structure.

Thus, we find that, as shown in Fig. 2(a), the conven-

Table 1 Numbers of PP rows and PP terms of the conventional schemes and the proposed scheme.

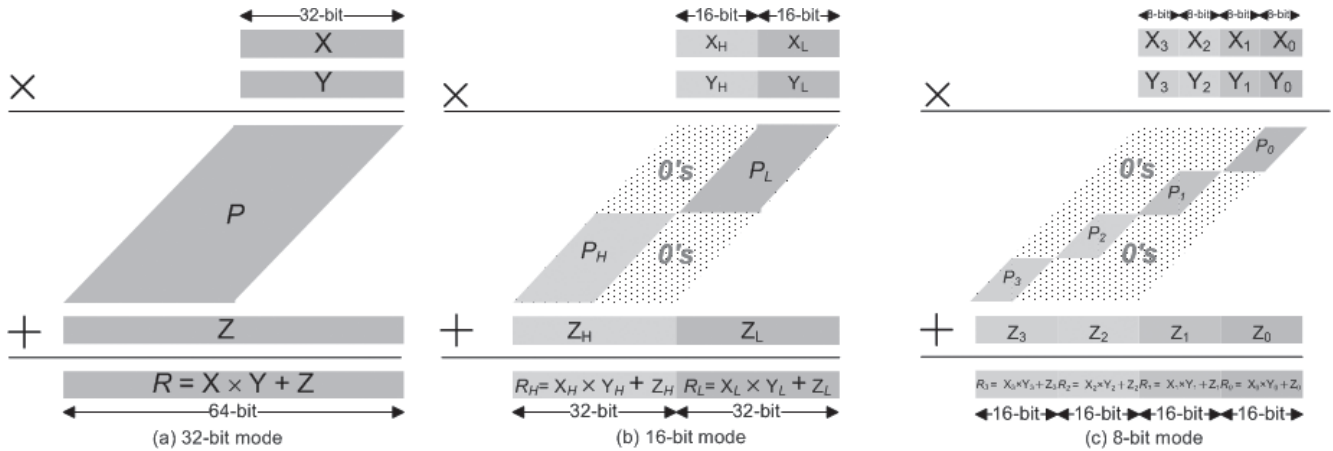| Method	Full sign-extended	[1], [5]	[12]	[2], proposed
PP rows	$\lceil n/2 \rceil + 1$	$\lceil n/2 \rceil + 1$	$\lceil n/2 \rceil + 1$	$\lceil n/2 \rceil$
PP terms	$\lceil n/2 \rceil (n + \lceil n/2 \rceil + 2)$	$\lceil n/2 \rceil (n + 4)$	$\lceil n/2 \rceil (n + 3) + 1$	$\lceil n/2 \rceil (n + 3) + 1$

Fig. 7 Segmented partial products and addendums for a 32-bit MAC core operate in (a) 32-bit scalar mode, (b)16-bit vector mode and (c) 8-bit vector mode.

tional scheme requires two additional 4-2-Cs, located at the 4-th and the 12-th columns, and one extra row of FAs, but the proposed scheme requires only one additional HA which is for negative compensation. The proposed scheme, in addition to being more regular, saves nine FAs and two 4-2-Cs at the expense of only one more HA. If we count the gate count of an HA as an FA and a 4-2-C as two FAs, the hardware saving of the proposed scheme is about $((\lceil n/4 \rceil - 1) \times 4 + n - 1) \times A_{FA}$, where A_{FA} is the area of an FA. This is mainly because for the conventional partial product array [5], [6] it requires two more 4-2-Cs which are located at the $(n - 4)$-th column and the $(n+4)$-th column respectively and one extra carry-save-adding row.

Another advantage of the proposed structure is that when the multiplier performs a wide-bit multiplication, the hybrid approach of two's complementation logic of the proposed scheme reduces the penalty of the last row selection mechanism and makes the partial product bits on the critical path arrive at the PPRT earlier. As stated previously, since the hybrid structure reduces both gate count on the non-critical paths and the loading of the intermediate prefix computing node on the critical path, the computation time of wide two's complementation rather than the Booth selector delay dominates its performance. Therefore, as the bit width of multiplication gets wider, the proposed scheme has more merit on gaining the speed performance and area saving. Furthermore, our proposed sign-select PPG circuit has additional speed performance over that of the PPG circuit of [2]. The estimated delay of our proposed Booth selector is 7.8 normalized gate delay (Gajski's model [15]) but that of the conventionally used Booth selector [2] is 11.2 normalized gate delay.

4. Application to the Reconfigurable MAC Design

The above proposed well-structured multiplier is applied to design a reconfigurable MAC core which can perform computations for one 32×32, two 16×16 or four 8×8 signed multiplication-accumulation. The structure as shown

in Figs. 7(a)–(c), where (a) shows a 32-bit operation, (b) shows a two 16-bit vector operation, and (c) shows a four 8-bit vector operation. The core achieves "share segmentation" [14] by using mode-depended multiplexers when generating the partial products and by eliminating carries which cross boundaries of sub-words in the PPRT and the final CPA.

The partial products associated with each sub-word do not overlap with others. Figure 8 shows the partial product array for the $32 \times 32 + 64$ multiplication-accumulation operated in an 8-bit vector mode using the proposed method. There are four vectorized sub-words, each of which performs an 8×8 bit multiplication-accumulation in a way which is explained in Fig. 2(b). Also, in this array, only 16 rows of PP terms are needed in contrast to the conventional 17 rows. The removal of the extra row enables this array to be easily implemented in the 4-2-Cs fashion to achieve a higher speed.

The block diagram of the reconfigurable PPG is shown in Fig. 9. The mode control signals select different precision mode that the MAC core can perform The "Multiplicand Muxes" control "sub-multiplicand masking", "zero-insertion", and "sign extending" with proper sign-encoding for each sub-word. The "Multiplier Masks" are used to zero out the regions of the sub-multiplicand when they are not used in the lower precision computing like an 8×8 operation. "Hot-two generator" and the "Last row selection unit" are used for achieving the rearranging signed carries and removing extra low of partial product array of Fig. 2(b). The partial products generated from "Booth selector" together with signals generated from "Hot-two generator" are then fed into the "PP Muxes" to generate leading $(n - 1)$ partial product rows depending on the permutation of mode control bits, significance and row number.

The sharing of common functions with a few additional control signals can make the power consumption and circuit area overheads of this structure very small. This MAC can be fully pipelined and so is suitable for high-performance processors.
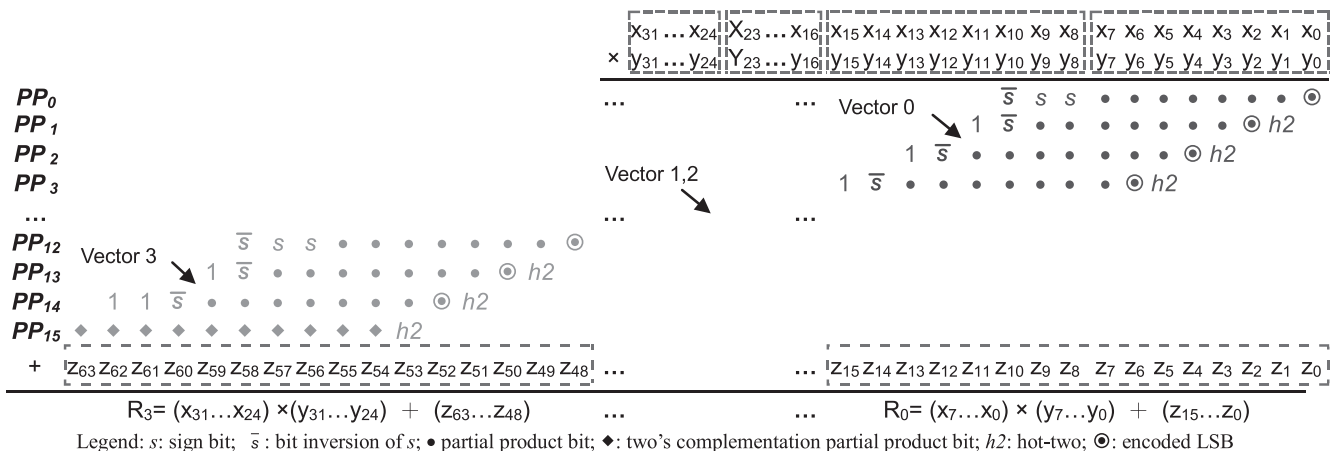
Legend: s: sign bit; $\bar{s}$: bit inversion of s; • partial product bit; ◆: two's complementation partial product bit; $h2$: hot-two; ◉: encoded LSB

Fig. 8   Partial product array for $32 \times 32 + 64$ multiplication-accumulation in an 8-bit mode using the proposed segmentation method.
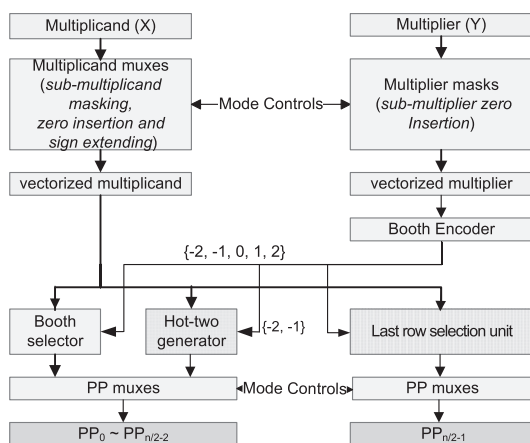

Fig. 9   Block diagram of reconfigurable PPG unit.

Table 2   Synthesis results of 32×32 MBE multipliers.

	Type I ([1])	Type II ([2])	Type III	Type IV
Area (μm^2)	102183	93092	87025	85983
Gate count	20557	18619	17405	17196
Power (mW@100MHz)	13.7	12.8	12.6	12.1

5.   Experiments —— Implementation and Results ——

5.1   Implementation of the Proposed Well-Structured Multiplier and its Performance

A proposed 32-bit well-structured multiplier was implemented with the Verilog hardware description language (HDL) and then synthesized with the Artisan standard cell library using the TSMC $0.13\,\mu m$ 1P8M CMOS process, under the "typical corner" operating condition. For comparison, multiplier structures of [1] and [2] were also implemented and synthesized. Dynamic simulations were performed to verify the function and to obtain the dynamic power consumption for each design. All the syntheses were done under the maximum-delay constraint, which was 3 ns. For these syntheses, in order to meet the same fixed delay constraint, the designs of slower speed will be assigned transistors of larger sizes by the synthesizing tool to meet the speed constraint. This will lead to a larger area and more gate count, consequently more power, for the designs of the slower speed performance. The results are shown in Ta-

ble 2. In the table, Type I and Type II are the multipliers of the structures of [1] and [2] respectively. A multiplier (Type III) which is of the proposed PPRT and PPG but with the two's complementation logic of Sklansky [2] was also synthesized for comparison. Type IV is our proposed well-structured design of the PPRT, the sign-select PPG and its two's complementation logic which has a 16-bits Sklansky and 5-6-5-bits VINC hybrid structure. From the table, it is seen that Type I has the largest area because of the extra row, as compared to the Type II design for which the extra row was removed. For the Type III design, the area and power were improved by about 6.5% and 1.6% respectively over those of the Type II design. For the Type IV design, further area (1.2%) and power (4%) reduction were obtained as compared to the Type III design due to the hybrid approach of two's complementation logic design used. Overall, as compared to the Type I design, the Type IV design has a 15.8% area and 11.7% power savings respectively.

5.2   Reconfigurable MAC with Mixed V_t Standard Cell Library

The proposed low-power MBE-based 32-bit reconfigurable MAC was implemented using a 130 nm 1.2 V CMOS process mixed-V_t (MVT) standard cell library. The MVT cell library was used to reduce power by applying low threshold voltage transistors in critical paths while standard threshold transistors in non-critical paths of logic gates [16]. The MVT standard cell library has lower power dissipation than single-V_t (SVT) standard cell library while it has the same speed of SVT cell library. The reconfigurable MAC core

Table 3 Comparisons of 32-Bit Reconfigurable MAC designed in scheme [14] and our proposed scheme.

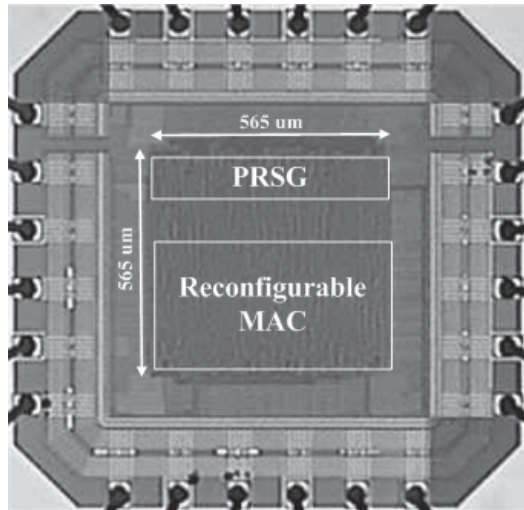|	[14]/MVT	Proposed/MVT
Area (um^2)	91407	87506
Gate count	18282	17502
Power(mW@100MHz)	12.1	11.2

Fig. 10   Chip microphotograph.

was synthesized using MVT cell library under the constraint of 4ns. For comparison, the reconfigurable design of [14] was also synthesized. Table 3 presents the results of the synthesis. The implementation shows that the area and power consumption of the proposed architecture are reduced about 4.2% and 7.4%, respectively, less than those of the aforementioned architecture [14].

The synthesized MVT design was also optimized to operate at 500 MHz and Fig. 10 shows the microphotograph of the die. A pseudo random signal generation (PRSG) circuit was included to generate test patterns to self-test the circuit. The post layout simulation of the chip shows that the chip can operate at 500 MHz at a power consumption of 86.25 mW under 1.2 V supply source. The chip was fabricated and tested. Due to the limitation of testing equipment, the core was tested at 125 MHz and the power consumption measured was 12.5 mW, excluding the I/O pins and PRSG circuit power consumption. This is close to the simulation result, which was simulated at 100 MHz, of Table 3. The measured higher power consumption is believed to be due to a higher operation frequency.

6.   Conclusion

This paper has presented a well-structured MBE multiplier design. Combining the design schemes such as the sign-extension bits reduction, the one extra partial product row removal and the hot signals position adjustment, the design saves both on area and power consumption, in addition to

its good feature of reconfigurability. Also, this design uses a hybrid structure to design the two's complementation circuit to further reduce the area and improve the speed. According to the synthesis results, the design can obtain 15.8% and 11.7% on the area and power savings respectively over the classical design and 7.5% and 5.5% area and power savings respectively over the design [2] which was reported to have the best performance. The well- structured multiplier had been applied to design a reconfigurable MAC core which can perform one 32×32, two 16×16, or four 8×8 signed multiplication-accumulation operations. The core was constructed by using a compact partial product array for two's complement based on the MBE algorithm. Experimental results show that the MAC exhibits about 4.2% and 7.4% savings respectively on the area and power consumption as compared to a previously reported architecture [14]. The proposed MAC core can be a good candidate for use in an SOC as a flexible data processing element.

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