Letters

MPPT and Voltage Balancing Control With Sensing Only Inductor Current for Photovoltaic-Fed, Three-Level, Boost-Type Converters

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***Abstract*—In the literature, both photovoltaic voltage and PV current need to be sensed to perform maximum power point tracking (MPPT) control. For three-level boost converter, both capacitor voltages need to be sensed and an additional voltage balancing control loop is required to balance the capacitor voltages. In this paper, the MPPT control and the voltage balancing control with sensing only inductor current is proposed. The provided simulation and experimental results demonstrate the proposed method.**

***Index Terms*—Maximum power point tracking (MPPT), voltage balancing control.**

I. Introduction

THE three-level boost-type converters have the advantages of the low voltage stress, the low inductor current ripple, and the low switching loss [1], [2]. Therefore, the three-level boost converters are widely used in the modern power electronics applications, such as ac/dc PFC application [1], [2], dc/dc PV applications [3]–[5], the fuel-cell applications [6], [7], and the wind energy application [8].

For the PV-fed converter, sensing both PV current and PV voltage is required to achieve the maximum power point tracking (MPPT) control. Additionally, for three-level boost-type converter, sensing additional capacitor voltages is also required to detect the voltage imbalance and force both capacitor voltages to be balanced [1], [2], [5], [7], [8].

By properly setting the sampling instants of the inductor current sensor, the average inductor current and the voltage imbalance can be detected by the proposed sampling strategy. It means that sensing only PV current (i.e., the inductor current) is able to achieve both MPPT function and the voltage balancing function. Then, both the MPPT and voltage balancing control will be achieved only by using the proposed sampling strategy of sampling the inductor current values. The simulation and experimental results are provided to verify the proposed methods.

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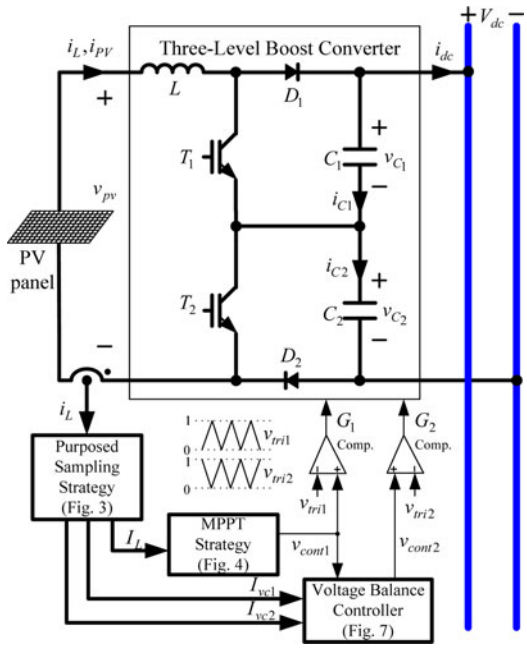

Fig. 1. PV-fed three-level boost-type converter with the proposed voltage balancing control.

II. Three-Level Boost-Type Converter

As shown in Fig. 1, the switching signals G_1 is obtained from the comparisons of the control signal $v_{\rm cont1}$ with the triangular signal $v_{\rm tri1}$. Since the three-level converter is connected to a well-regulated dc voltage $V_{\rm dc}$, the sum of two capacitor voltages is assumed to be fixed $v_{C_1} + v_{C_2} = V_{\rm dc}$.

In addition, the other switching signals G_2 is obtained by comparing the control signal $v_{\rm cont2}$ with the triangular signal $v_{\rm tri2}$ where there is a phase difference of 180° between two triangular signals.

Due to the input inductor L and two diodes D_1 and D_2 in the three-level boost-type converter, both switches can be turning on at the same time. Therefore, there are four possible switching states plotted in Fig. 2.

As shown in Fig. 2(a), both switches turn on when the control signal $v_{\rm cont1}$ is larger than the signal $v_{\rm cont1} \geq v_{\rm tri1}$ and the control signal $v_{\rm cont2}$ is larger than the signal $v_{\rm cont2} \geq v_{\rm tri2}$. Thus, the inductor voltage v_L is equal to the PV voltage $v_L = v_{\rm PV} \geq 0$. The current rising rate in the switching state 1 is always positive.

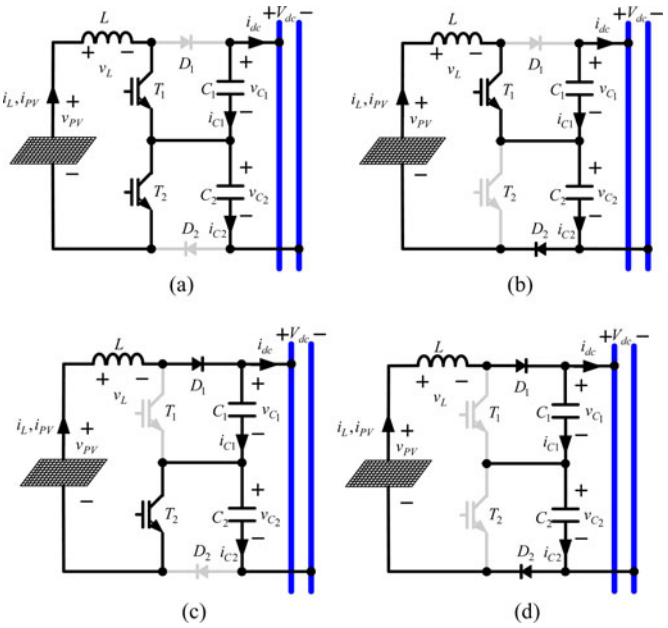

Fig. 2. Possible switching states in three-level boost-type converter: (a) state 1; (b) state 2; (c) state 3; and (d) state 4.

For the switching state 2 in Fig. 2(b), the upper switch T_1 turns on and the lower switch T_2 turns off. The inductor voltage v_L is equal to the difference between the PV voltage $v_{\rm PV}$ and the capacitor voltage $v_L = v_{\rm PV} - v_{C_2}$. The current rising rate may be either positive or negative. Additionally, the capacitor current i_{C_2} is equal to the inductor current $i_{C_2} = i_L \geq 0$. Thus, the capacitor C_2 is charging, and the other capacitor C_1 is discharging in the switching state 2.

Similarly, when the upper switch T_1 turns off and the lower switch T_2 turns on as plotted in Fig. 2(c), the inductor voltage v_L is equal to the voltage difference $v_L = v_{\rm PV} - v_{C_1}$ and the current rising rate may be either positive or negative. It is also noted that in switching state 3, the capacitor C_1 is charging, and the other capacitor C_2 is discharging.

When both switches turn off as shown in Fig. 2(d), the inductor voltage v_L is equal to the PV voltage minus the dc-bus voltage $v_L = v_{\rm PV} - V_{\rm dc} = v_{\rm PV} - v_{C_1} - v_{C_2}$. Since the output voltage is higher than the input voltage in the boost-type converter, the current rising rate is always negative in switching state 4.

The current rising rates in various conditions and in various switching states are listed in Table I. For the condition $v_{\rm cont1} + v_{\rm cont2} < 1$, two switching signals G_1 and G_2 may not be high at the same time due to the 180° phase-shift triangular signals. Thus, there are only switching state 2, state 3, and state 4 in the condition $v_{\rm cont1} + v_{\rm cont2} < 1$. Similarly, only switching state 1, state 2, and state 3 exist in the other condition $v_{\rm cont1} + v_{\rm cont2} > 1$.

The proposed sampling strategy is shown in Fig. 3 where the sampling instants are interleaved. When the triangular signal $v_{\rm tri1}$ is at its peaks and valleys, the inductor current i_L is sampled, and the obtained value is defined as the average inductor current value I_L.

When the ascending triangular signal $v_{\rm tri1}$ is equal to 0.5, the inductor current as previously explained is also sampled and defined as I_{vc1}. In addition, the other value $I_{\rm vc2}$ is obtained by sampling the inductor current i_L at the instants of the descending triangular signal $v_{\rm tri1}$ equal to 0.5.

From Fig. 1, the sampled value I_L is used for MPPT control, and the two values $I_{\rm vc1}$ and $I_{\rm vc2}$ are used for the proposed voltage balancing control.

III. Proposed MPPT Control

The PV power $P_{\rm PV}$ is the product of the PV current $i_{\rm PV}$ and the PV voltage $v_{\rm PV}$. By neglecting the power loss of the three-level boost converter, the PV power can also be expressed as the product of the dc-bus voltage $V_{\rm dc}$ and the average bus current $\langle i_{\rm dc}\rangle_{Ts}$ within the switching period T_s

$$P_{\rm PV} = v_{\rm PV} \times i_{\rm PV} = V_{\rm dc} \times \langle i_{\rm dc}\rangle_{Ts} \tag{1}$$

In the boost-type converter, the average bus current $\langle i_{\rm dc}\rangle_{Ts}$ is equal to the product of the duty ratio $(1 - v_{\rm cont1})$ and the average inductor current value $\langle i_{\rm dc}\rangle_{Ts} = (1 - v_{\rm cont1})\langle i_L\rangle_{Ts}$. Since the average inductor current value $\langle i_L\rangle_{Ts} = I_L$ is obtained by the proposed sampling strategy, the PV power $P_{\rm PV}$ can be rewritten as

$$P_{\rm PV} = V_{\rm dc}(1 - v_{\rm cont1})I_L. \tag{2}$$

Because the dc-bus voltage $V_{\rm dc}$ is well regulated, the PV power $P_{\rm PV}$ is directly proportional to the product of the average inductor current I_L and the duty ratio $(1-v_{\rm cont1})$. By using the simple perturbation and observation method, the proposed MPPT method with sensing only inductor current is shown in Fig. 4 where the duty ratio signal $v_{\rm cont1}$ may be changed with a constant step $\Delta v_{\rm cont1}$.

After sampling the inductor current and calculating the new product $P'_{\rm PV}[n] = (1 - {\rm v}_{\rm cont}[n]) \times I_L[n]$, two comparisons are made. The former comparison is between the latest product $P'_{\rm PV}[n]$ and the previous product $P'_{\rm PV}[n-1]$, and the latter comparison is between the duty ratio $v_{\rm cont1}[n]$ and the previous duty ratio $v_{\rm cont1}[n-1]$.

For the case of $P'_{\rm PV}[n] > P'_{\rm PV}[n-1]$ and $v_{\rm cont1}[n] > v_{\rm cont1}[n-1]$, the duty ratio should keep increasing to move to maximum power point and the new control signal is obtained by adding a constant $\Delta v_{\rm cont1}$ to the control signal $v_{\rm cont1}[n]$. Similarly, the duty ratio should also increase to move to maximum power point for the case of $P'_{\rm PV}[n] < P'_{\rm PV}[n-1]$ and $v_{\rm cont1}[n] < v_{\rm cont1}[n-1]$.

In both cases of $P'_{\rm PV}[n] > P'_{\rm PV}[n-1]$ and $v_{\rm cont1}[n] < v_{\rm cont1}[n-1]$ or the case $P'_{\rm PV}[n] < P'_{\rm PV}[n-1]$ and $v_{\rm cont1}[n] > v_{\rm cont1}[n-1]$, the control signal $v_{\rm cont1}[n]$ should keep decreasing to return to the maximum power point by subtracting a constant $\Delta v_{\rm cont1}$ from the duty ratio $v_{\rm cont1}[n]$.

IV. Proposed Voltage Balancing Control

In this section, the new voltage balancing control loop without sensing capacitor voltages is proposed. The following analysis is divided into two cases. One case is that the sum of two duty ratios

TABLE I
CURRENT RISING RATES IN VARIOUS STATES

Switching state		State 1	State 2	State 3	State 4
Current rising rate $\frac{di_L}{dt}$		$\frac{v_{PV}}{L}$	$\frac{(v_{PV}-v_{C2})}{L}$	$\frac{(v_{PV}-v_{C1})}{L}$	$\frac{(v_{PV}-V_{dc})}{L}$ $=\frac{(v_{PV}-v_{C1}-v_{C2})}{L}$
$v_{cont1}+v_{cont2}<1$ (Only State 2, 3, 4)	$v_{PV}>v_{C1}>v_{C2}$ (Fig. 5(a))		>0	>0	<0
	$v_{PV}>v_{C2}>v_{C1}$ (Fig. 5(b))		>0	>0	<0
	$v_{C1}>v_{PV}>v_{C2}$		>0	<0	<0
	$v_{C2}>v_{PV}>v_{C1}$		<0	>0	<0
$v_{cont1}+v_{cont2}>1$ (Only State 1, 2, 3)	$v_{C1}>v_{C2}>v_{PV}$	>0	<0	<0	
	$v_{C2}>v_{C1}>v_{PV}$	>0	<0	<0	
	$v_{C1}>v_{PV}>v_{C2}$ (Fig. 6(a))	>0	>0	<0	
	$v_{C2}>v_{PV}>v_{C1}$ (Fig. 6(b))	>0	<0	>0	

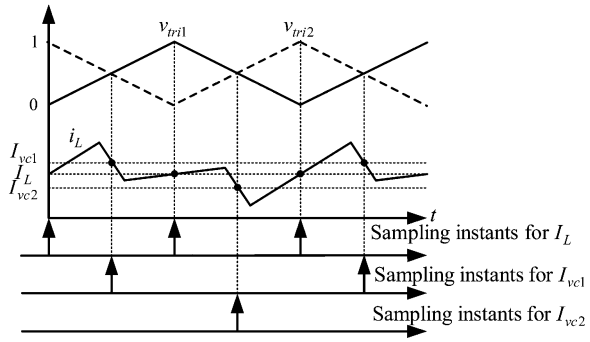

Fig. 3. Proposed sampling strategy.

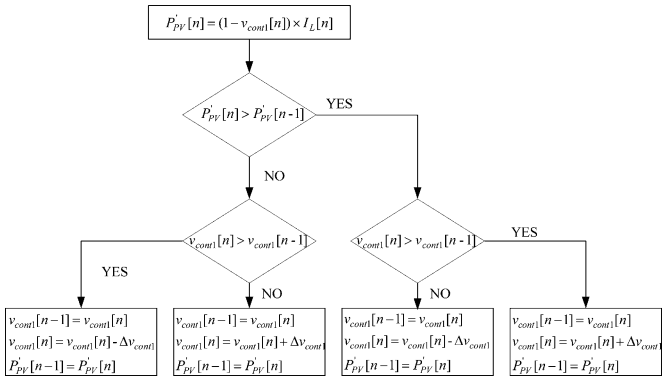

Fig. 4. Proposed MPPT algorithm with only sensing inductor current.

is smaller than one $v_{\rm cont1}+v_{\rm cont2}<1$, and in the other case, the sum of two duty ratios is larger than one $v_{\rm cont1}+v_{\rm cont2}>1$.

For the case $v_{\rm cont1}+v_{\rm cont2}<1$, both switching signals must not be "on" at the same time, and thus, only switching state 2, state 3, and state 4 can be found. By considering the current rising rates in Table I, there are four conditions and two of them are illustrated in Fig. 5.

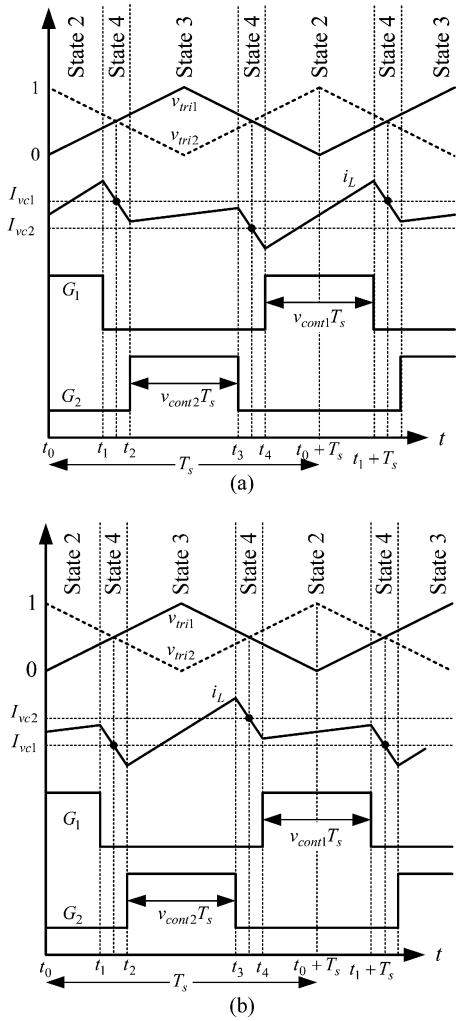

Fig. 5. Illustrated waveforms for the case of $v_{\rm cont1}+v_{\rm cont2}<1$: (a) when $v_{\rm PV}>v_{C_1}>v_{C_2}$; (b) when $v_{\rm PV}>v_{C_2}>v_{C_1}$.

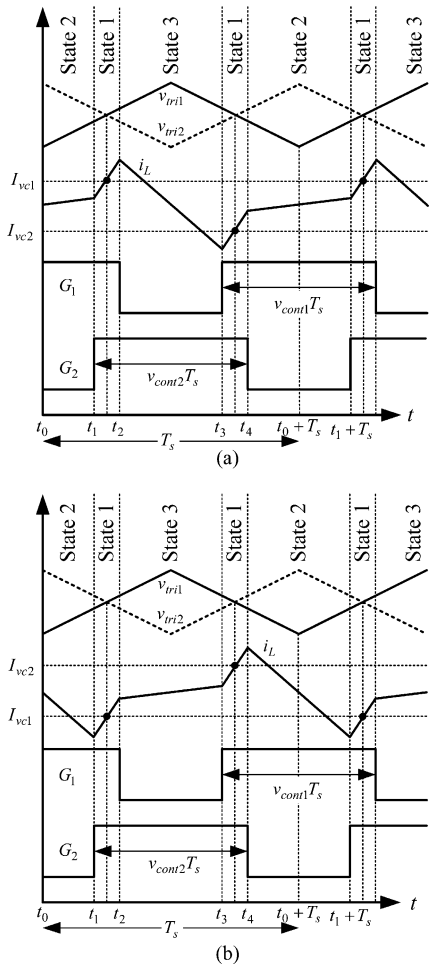

Fig. 6. The illustrated waveforms for the case of $v_{\rm cont1}+v_{\rm cont2}>1$: (a) when $v_{C1}>v_{\rm PV}>v_{C2}$; (b) when $v_{C2}>v_{\rm PV}>v_{C1}$.

For the case $v_{\rm cont1}+v_{\rm cont2}>1$, both switching signals must not be "off" at the same time, and thus, only switching state 1, state 2, and state 3 can be found. Two of the possible conditions are plotted in Fig. 6.

Case: $v_{\rm cont1}+v_{\rm cont2}<1$

The illustrated waveforms at the voltage imbalance conditions $v_{\rm PV}>v_{C_1}>v_{C_2}$ and $v_{\rm PV}>v_{C_2}>v_{C_1}$ are plotted in Fig. 5(a) and (b), respectively. According to Table I, the current rising rate in the switching state 2 of Fig. 5(a) is larger than the switching state 3 due to $v_{C_1}>v_{C_2}$. But in Fig. 5(b), the current rising rate of state 2 is smaller than that of the switching state 3 due to $v_{C_2}>v_{C_1}$.

From the proposed sampling strategy, the values $I_{\rm vc1}$ and $I_{\rm vc2}$ are sampled at the instants $t_1+(t_2-t_1)/2$ and $t_3+(t_4-t_3)/2$ as shown in Fig. 5, respectively. Due to the symmetry in the switching signals, the time difference (t_2-t_1) is equal to the time difference (t_4-t_3), and both are equal to $(t_2-t_1)=(t_4-t_3)=(1-v_{\rm cont1}-v_{\rm cont2})T_s/2$.

Thus, two sampled values $I_{\rm vc1}$ and $I_{\rm vc2}$ can be expressed as

$$I_{\rm vc1}=i_L\left(t_1+\frac{1-v_{\rm cont1}-v_{\rm cont2}}{4}T_s\right) \tag{3}$$

$$I_{\rm vc2}=i_L\left(t_3+\frac{1-v_{\rm cont1}-v_{\rm cont2}}{4}T_s\right). \tag{4}$$

Thus, the difference between two sampled values $I_{\rm vc2}$ and $I_{\rm vc1}$ can be expressed as

$$I_{\rm vc2}-I_{\rm vc1}=\frac{v_{\rm PV}-v_{C_1}-v_{C_2}}{L}\frac{1-v_{\rm cont1}-v_{\rm cont2}}{2}T_s+\frac{v_{\rm PV}-v_{C_1}}{L}v_{\rm cont2}T_s. \tag{5}$$

In steady-state condition, the inductor current is repetitive with period T_s, and thus, the difference between two sampled values $I_{\rm vc2}$ and $I_{\rm vc1}$ can also be expressed as

$$I_{\rm vc2}-I_{\rm vc1}=-\frac{v_{\rm PV}-v_{C_1}-v_{C_2}}{L}\frac{1-v_{\rm cont1}-v_{\rm cont2}}{2}T_s-\frac{v_{\rm PV}-v_{C_2}}{L}v_{\rm cont1}T_s. \tag{6}$$

Combining (5) and (6) yields the following equation:

$$v_{\rm PV}=(1-v_{\rm cont1})v_{C_1}+(1-v_{\rm cont2})v_{C_2} \tag{7}$$

By substituting (7) into (6), and thus, the difference $(I_{\rm vc2}-I_{\rm vc1})$ can be simplified to be

$$I_{\rm vc2}-I_{\rm vc1}\approx\frac{T_s}{2L}v_{\rm cont1}(v_{C_2}-v_{C_1}). \tag{8}$$

From (8), it is clear that the difference $(I_{\rm vc2}-I_{\rm vc1})$ is proportional to the voltage imbalance $(v_{C2}-v_{C1})$ in the case where $v_{\rm cont1}+v_{\rm cont2}<1$.

Case: $v_{\rm cont1}+v_{\rm cont2}>1$

The illustrated waveforms for the case where the voltage imbalance conditions $v_{C_1}>v_{\rm PV}>v_{C_2}$ and $v_{C_2}>v_{\rm PV}>v_{C_1}$ are plotted in Fig. 6(a) and (b), respectively. In Fig. 6, the difference $(I_{\rm vc2}-I_{\rm vc1})$ between two sampled values $I_{\rm vc2}$ and $I_{\rm vc1}$ can be expressed as

$$I_{\rm vc2}-I_{\rm vc1}=\frac{v_{\rm PV}}{L}\frac{1-v_{\rm cont1}-v_{\rm cont2}}{2}T_s+\frac{v_{\rm PV}-v_{C_1}}{L}v_{\rm cont2}T_s \tag{9}$$

Similarly, the difference $(I_{\rm vc2}-I_{\rm vc1})$ can also be expressed as

$$I_{\rm vc2}-I_{\rm vc1}=-\frac{v_{\rm PV}}{L}\frac{1-v_{\rm cont1}-v_{\rm cont2}}{2}T_s-\frac{v_{\rm PV}-v_{C_2}}{L}v_{\rm cont1}T_s. \tag{10}$$

Combining (9) and (10) may yield the following equation:

$$v_{\rm PV}=(1-v_{\rm cont2})v_{C_1}+(1-v_{\rm cont1})v_{C_2}. \tag{11}$$

By substituting (11) into (9), and thus, the difference $(I_{\rm vc2}-I_{\rm vc1})$ can also be simplified to be

$$I_{\rm vc2}-I_{\rm vc1}\approx\frac{T_s}{2L}(1-v_{\rm cont1})(v_{C_2}-v_{C_1}) \tag{12}$$

The aforementioned equation shows that the difference $(I_{\rm vc2}-I_{\rm vc1})$ is proportional to the voltage imbalance $(v_{C_2}-v_{C_1})$ in the case where $v_{\rm cont1}+v_{\rm cont2}>1$.

In Fig. 6(a), the current rising rate of the switching state 2 is positive, but the current rising rate in switching state 3 is negative due to $v_{C_2}>v_{C_1}$. The value $I_{\rm vc1}$ is larger than the other value $I_{\rm vc2}$ where the capacitor voltage v_{C_1} is larger than the other voltage v_{C_2}.

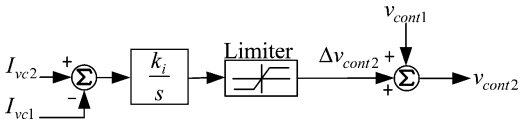

Fig. 7. Proposed voltage balancing control loop with only sensing the inductor current.

TABLE II
PARAMETERS OF PV PANELS

Maximum power	$480W$
Voltage at maximum power	$100V$
Current at maximum power	$4.8A$
Open-circuit voltage	$117.64V$
Short-circuit current	$5.33A$

TABLE III
PARAMETERS OF PV-FED THREE-LEVEL CONVERTER

DC voltage bus	$200V$
Inductor L	$1mH$
Capacitor C_1	$2420\mu F$
Capacitor C_2	$1980\mu F$
Switching period T_s	$12.5\mu s$
Deviation Δv_{cont1}	0.002
Controller parameter k_i	0.000025

In Fig. 6(b), the current rising rate of the switching state 2 is negative, and the current rising rate in switching state 3 is positive. The value $I_{\rm vc1}$ is smaller than the other value $I_{\rm vc2}$ where the capacitor voltage v_{C_1} is smaller than the other voltage v_{C_2}.

From (8) and (12), the voltage imbalance $(v_{C_2} - v_{C_1})$ can be detected from the difference $(I_{\rm vc2} - I_{\rm vc1})$ without sensing capacitor voltages. The proposed voltage balancing control loop is shown in Fig. 7 where a simple integrator controller and a limiter is used to generate the compensation signal $\Delta v_{\rm cont2}$. The control signal $v_{\rm cont2}$ is obtained by adding the signal $\Delta v_{\rm cont2}$ to the control signal $v_{\rm cont1}$ from the proposed MPPT control in Fig. 4

$$v_{\rm cont2} = v_{\rm cont1} + \Delta v_{\rm cont2}. \tag{13}$$

V. SIMULATION RESULTS

In this section, some simulation results are provided and the simulated parameters are listed in Tables II and III. Two capacitors $C_1 = 2420$ μF and $C_2 = 1980$ μF are connected in series in the circuit to yield the voltage imbalance. The dc voltage bus is 200 V and the switching period is 12.5 μs. The frequency of the MPPT loop is 100 Hz, and the frequency of the voltage balancing loop is 80 kHz.

The simulated waveforms are plotted in Fig. 8. Before the MPPT control is applied at the time t_0, both control signals $v_{\rm cont1}$ and $v_{\rm cont2}$ are fixed to 0.4. Due to the capacitance mismatch as indicated in Table III, the voltage imbalance 20 V exists between two capacitor voltages v_{C_1} and v_{C_2}. The sensed

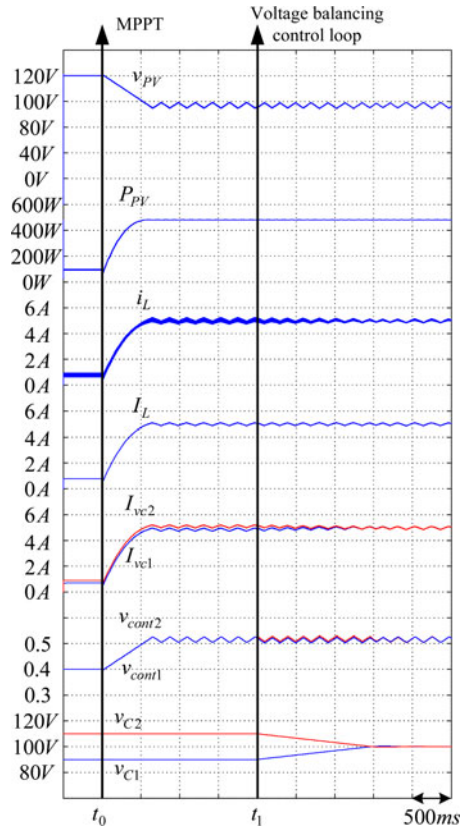

Fig. 8. Simulated results for the proposed MPPT and voltage balancing control methods.

value $I_{\rm vc2}$ is also larger than the other sensed value $I_{\rm vc1}$, which demonstrates the derived equation in (8).

After the MPPT control is applied at t_0, both control signals $v_{\rm cont1}$ and $v_{\rm cont2}$ change according to the proposed MPPT control strategy. The yielded waveforms $v_{\rm PV}$ and the PV power $P_{\rm PV}$ show that the maximum power point is achieved.

Before the voltage balancing control loop is applied at t_1, both control signals $v_{\rm cont1}$ and $v_{\rm cont2}$ are larger than 0.5 and thus, $v_{\rm cont1} + v_{\rm cont2} > 1$. The voltage imbalance across the capacitors still exists and fortunately, the voltage imbalance $(v_{C_2} - v_{C_1})$ can be detected from the difference $(I_{\rm vc2} - I_{\rm vc1})$.

After the proposed voltage balancing control loop is applied at the time t_1, the control signal $v_{\rm cont2}$ becomes larger than $v_{\rm cont1}$ and thus, the time of switching state 2 is larger than switching state 3. It follows that the capacitor C_1 has larger charging time than the other capacitor C_2. Therefore, due to the fixed dc-bus voltage 200 V, the capacitor voltage v_{C_1} starts rising, and the other voltage v_{C_2} falls until they come to half dc-bus voltage 100 V. Finally, both capacitor voltages are balanced and the sensed values $I_{\rm vc2}$ and $I_{\rm vc1}$ are equal to each other.

VI. EXPERIMENTAL RESULTS

The proposed control method has been implemented in a FPGA-based system with commercial FPGA XC3S200 chip. The nominal parameters are the same as those in Tables II and III, but the both capacitors in the experiment have the same

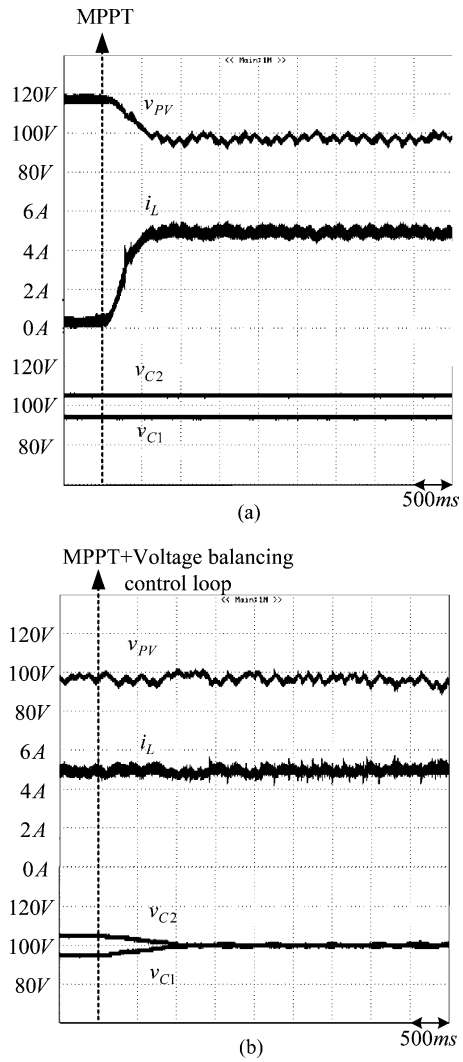

Fig. 9. Experimental results (a) with the proposed MPPT control and (b) with the proposed MPPT and voltage balancing control loop.

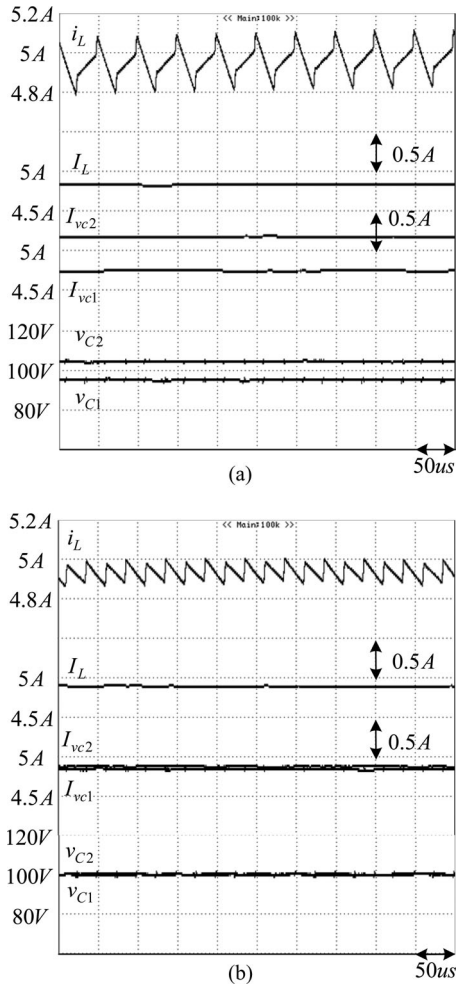

Fig. 10. Enlarged steady-state waveforms (a) before the voltage balancing control loop is applied and (b) after the voltage balancing control loop is applied.

nominal values 2200 μF. In practice, the mismatch of two real capacitances and two equivalent series resistors (ESRs) may contribute to the voltage imbalance.

The experimental results with the proposed MPPT control method and with the voltage balancing control loop are plotted in Fig. 9(a) and (b), respectively. In Fig. 9(a), the initial voltage imbalance is near 10 V.

After the proposed MPPT control is applied, the measured PV voltage $v_{\rm PV}$ and the inductor current i_L show that the PV panel is operating at the maximum power point. Therefore, the proposed MPPT method with sensing only inductor current is able to track the maximum power point.

In Fig. 9(b), the capacitor voltage v_{C_2} falls and the capacitor voltage v_{C_1} rises due to the applied voltage balancing control loop. The waveforms show that the proposed voltage balancing control loop is able to balance the capacitor voltages with sensing only the inductor current. In addition, the PV panel still operates at the maximum power point even the voltage balancing control loop is applied.

Before the proposed voltage balancing control loop is applied, the enlarged steady-state waveforms are plotted in Fig. 10(a). The waveforms shows the PV voltage $v_{\rm PV}$ is larger than the capacitor voltage v_{C_1}, but is smaller than the capacitor voltage v_{C_2} [i.e., the condition $v_{C_2} > v_{\rm PV} > v_{C_1}$ in Fig. 6(b)]. The waveform also shows that the inductor current ripple Δi_L is near 0.27 A. In addition, the difference $(I_{\rm vc2} - I_{\rm vc1})$ is able to provide the useful information of the voltage imbalance $(v_{C_2} - v_{C_1})$.

As shown in Fig. 9(b), the capacitor voltages are finally balanced after the proposed balancing control loop is applied and the enlarged steady-state waveforms are plotted in Fig. 10(b). It is clear that, the two voltages are closed to each other and the inductor current ripple Δi_L is reduced significantly to near 0.15 A. The reduced inductor current ripple also reduces the inductor loss and improves the circuit efficiency.

However, from the provided experimental results, the proposed voltage balancing control loop with sensing only inductor current is verified.

VII. Conclusion

In this paper, the MPPT and the voltage balancing control methods for three-level boost-type converter is proposed. By the proposed sampling strategy, the information of the PV power and the voltage imbalance can be provided for the proposed control methods. The simulation and experimental results show that the proposed methods with only sensing the inductor current are able to achieve the desired functions. The proposed methods reduce the sensor count and save the cost. In addition, the proposed voltage balancing control loop can be extended to other circuits which needs to avoid voltage imbalance.

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