Novel Ion Bombardment Technique for Doping Limited Cu Source in SiO_x-Based Nonvolatile Switching Layer

Sheng-Hsien Liu, Wen-Luh Yang, Yu-Hsien Lin, Chi-Chang Wu, and Tien-Sheng Chao

***Abstract*—A novel ion bombardment (IB) technique is presented to dope a limited Cu source in an SiO_x switching layer (SiO_x:Cu SL) for nonvolatile memory applications. Compared with other Cu-doping methods, this IB technique has many benefits, including a local-doping effect, room-temperature process, and compatibility with current IC manufacturing technology, besteading the $1T$-$1R$ integration. Through transmission electron microscopy and energy dispersive spectrometer analyses, an IB-induced SiO_x:Cu SL is confirmed. In contrast with the conventional Cu/SiO_x-stacked sample, this IB-induced SiO_x:Cu SL exhibits superior performance in terms of lower forming/RESET voltages, higher uniformity of SET/RESET voltages, and more stable high-temperature retention characteristics. Additionally, so far, this IB-induced TaN/SiO_x:Cu/TaN device has shown the best switching endurance properties for the general SiO_x-based Cu filament resistance random access memory.**

***Index Terms*—Cu-doped SiO_x, ion bombardment (IB), limited Cu source, resistance random access memory (ReRAM).**

I. INTRODUCTION

RECENTLY, SiO_x-based Cu filament (CF) switching layers (SLs) have been actively studied for resistance random access memory (ReRAM) applications [1]–[5]. That is because Cu and SiO_x materials have been widely used in semiconductor products and completely compatible with CMOS processing [6], [7]. Many reports indicated, however, the conventional CF ReRAM, consisting of Cu electrode/active layer/metal electrode, has unstable high-temperature retention problems because of the high Cu concentration in the SL [8]–[10]. For this reason, several Cu-doping technologies have been proposed to control and limit the Cu concentration in the SL such as thermal diffusion [11] and electric-field driving [12]. For the thermal diffusion method, it could be easy for the Cu concentration to be controlled by temperature and heating time, but a large thermal budget and isotropic doping limit the $1T$-$1R$ integration. For the electric-field driving process, local and anisotropic doping effects can be easily achieved, but this process is very complex and unsuitable for mass production in industry.

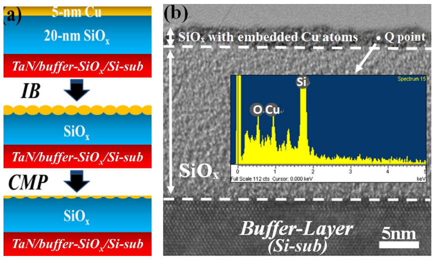

Fig. 1. (a) Schematic processing flows of the IB-induced SiO_x:Cu SL. (b) Cross-sectional TEM image of the IB-induced SiO_x:Cu SL. The sample was prepared on Si-substrate for material analyses. Inset: results of EDS analysis at Q point in the TEM image.

In this letter, a novel ion bombardment (IB) technique is proposed for fabricating a Cu-doped SiO_x (SiO_x:Cu) SL. Using the IB technique, a limited Cu source can be directly embedded in the SiO_x film without any thermal treatment. This IB technique is completely compatible with the CMOS processing and possesses the local and anisotropic doping effects. In addition, this method could avoid the difficulties in patterning etching of Cu processes for $1T$-$1R$ integration.

II. EXPERIMENTS

A TaN film was deposited on the prepared buffer-SiO_x/Si substrate as a bottom electrode. Subsequently, 20-nm thick SiO_x and 5-nm thick Cu films were sequentially deposited by plasma enhanced chemical vapor deposition and sputter, respectively. Afterward, the argon IB treatment for 5 s at room temperature (RT) was performed by high density plasma chemical vapor deposition. The critical plasma density and energy were controlled by RF (900 W) and dc (200 W) power, respectively. The IB treatment results in an increase in the roughness of ultrathin Cu film and causes the local Cu to sink in the SiO_x film. After that, the chemical mechanical polishing (CMP) process was used to remove the Cu that was on the surface of SiO_x film and retained the limited Cu in the SiO_xfilm. The processing diagram of IB-induced SiO_x:Cu SL is shown in Fig. 1(a). The plasma energy controls the

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S.-H. Liu is with the Ph.D. Program of Electrical and Communications Engineering, Feng Chia University, Taichung 40724, Taiwan.

W.-L. Yang is with the Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan (e-mail: wlyang@fcu.edu.tw).

Y.-H. Lin is with the Department of Electronic Engineering, National United University, Miaoli 36003, Taiwan.

C.-C. Wu is with the Graduate Institute of Biomedical Materials and Tissue Engineering, College of Oral Medicine, Taipei Medical University, Taipei 11031, Taiwan.

T.-S. Chao is with the Department of Electrophysics, National Chiao Tung University, Hsinchu 30010, Taiwan.

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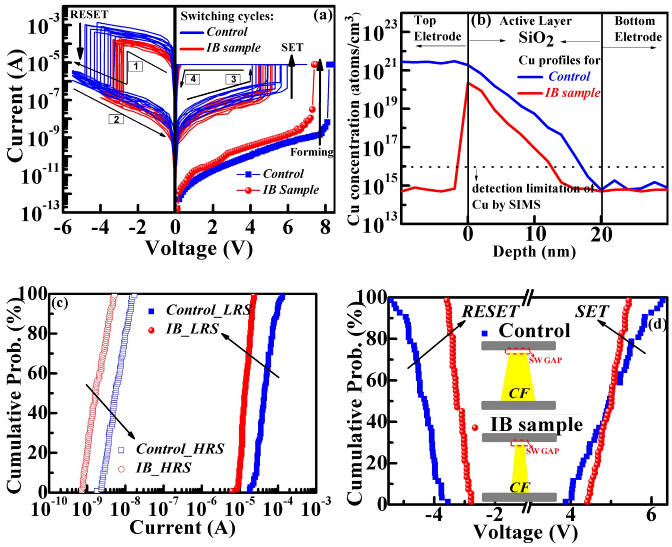

Fig. 2. (a) Typical bipolar I–V switching characteristics of the IB-induced SiO$_x$: Cu (IB sample) and Cu/SiO$_x$-stacked (control sample) SLs. In forming and SET processes, current compliance was set to 7.85×10^{-6} A to prevent the devices in hard-breakdown, and overshoot phenomena can be ignored. (b) Postforming Cu concentration profiles of the IB and control samples analyzed by backside SIMS. (c) Single-cell statistical distribution of the LRS and HRS current ($V_{\text{read}} = 0.3$ V). (d) Statistical distribution of the SET and RESET voltages.

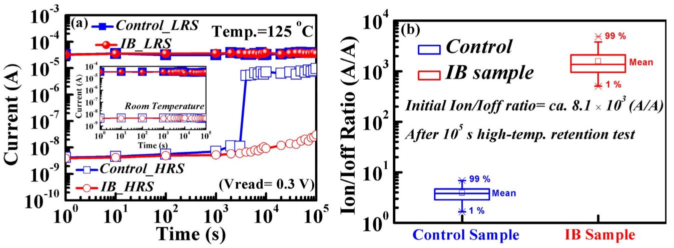

Fig. 3. (a) Resistive retention characteristics of the IB-induced SiO$_x$:Cu (IB sample) and Cu/SiO$_x$-stacked (control sample) SLs at RT and 125 °C, respectively. (b) (50 cells) Cell-to-cell statistical distribution of the maintainable LRS/HRS ratio for IB and control samples after 125 °C for 10^5 s test.

physical-impact intensity to further dominate the embedded depth of IB-induced Cu source. In addition, the plasma density and energy influence the roughness of ultrathin Cu film, as well as the amount of IB-induced Cu source. Finally, a TaN top electrode was deposited through metal mask by sputter. Additionally, a conventional Cu/SiO$_x$-stacked sample, Cu/SiO$_x$/TaN, was also prepared as the control sample. The diameters of the samples were 100 μm. In this letter, the electrical characteristics were tested in 1-R architecture.

III. RESULTS AND DISCUSSION

Fig. 1(b) shows a cross-sectional transmission electron microscopy (TEM) image of the IB-induced SiO$_x$:Cu SL. The inset demonstrates results of energy dispersive spectrometer (EDS) at Q point in the TEM image. There are Cu, Si, and O signals at the Q point. It implies that the Q point is composed of SiO$_x$ and Cu. Through the TEM and EDS analyses, therefore, it is confirmed that as an ultrathin Cu film deposited on SiO$_x$ film is treated with IB and CMP treatments chronologically, partial Cu atoms would be directly embedded in the SiO$_x$ film. The embedded depth of Cu atoms is estimated to be *ca.* 2 nm.

Fig. 2(a) shows I–V transients of the IB-induced SiO$_x$:Cu and Cu/SiO$_x$-stacked SLs. It is obvious that the IB-induced SiO$_x$:Cu SL shows a lower forming voltage than the Cu/SiO$_x$-stacked sample. This could be ascribed to the structural difference and the IB-induced degradation of SiO$_x$ film. Compared with the IB-induced SiO$_x$:Cu SL, the Cu/SiO$_x$-stacked sample requires additional energy to drive the Cu of electrode drifting into the SiO$_x$film and become interstitial impurities. Besides, the IB treatment could damage the surface of SiO$_x$ film to cause an increase of current before forming, as shown in Fig. 2(a). In contrast to the small current, however, the large current performance can produce and supply more thermal energy to devices during forming CF to further result in a decrease in the forming voltage. Fig. 2(b) shows postforming Cu concentration profiles of the IB-induced SiO$_x$:Cu and Cu/SiO$_x$-stacked samples. It is seen that the IB-induced SiO$_x$:Cu sample shows a lower Cu concentration profile in the SiO$_x$ film than the Cu/SiO$_x$-stacked sample. This could be ascribed to the difference between the limited and infinite Cu sources. This is because the flux of Cu during forming is dependent on the amount of Cu source. Therefore, it can be reasonably inferred that the CF size of the IB-induced SiO$_x$:Cu sample should be thinner than that of the Cu/SiO$_x$-stacked sample. This conjecture can be, however, observed from the difference in low resistance state (LRS) current between them, as shown in Fig. 2(a) and (c). This is because the LRS current is directly proportional to the CF thickness. Fig. 2(d) shows statistical distribution of the SET and RESET voltages. It is seen that the IB-induced SiO$_x$:Cu SL has a lower RESET voltage than the Cu/SiO$_x$-stacked sample. This is due to the thin CF of IB-induced SiO$_x$:Cu SL. It is easy for the thin CF to be ruptured under low applied-voltage. Additionally, it is found that the IB-induced SiO$_x$:Cu SL shows more uniform SET/RESET voltages in comparison with the Cu/SiO$_x$-stacked sample. This could be also attributed to the CF thickness. As compared with the thick CF, the thin CF has a smaller range of switching gap. In SET process, Cu around the switching gap requires sufficient energy for redox, migration, and agglomeration. For Cu atoms in the different positions, however, their requirement for the total energy could not be the same. This explains why the IB-induced SiO$_x$:Cu SL has better uniformity of the SET voltage than the Cu/SiO$_x$-stacked sample.

Fig. 3(a) shows retention characteristics of the IB-induced SiO$_x$:Cu and Cu/SiO$_x$-stacked SLs at RT and 125 °C, respectively. Before retention test, we adjusted the current compliance in the forming process for achieving the same initial current on the LRS and high resistance state (HRS). In the inset of Fig. 3(a), it is shown that they both demonstrate stable retention properties without apparent changes in the LRS and HRS at RT. As the test temperature is increased to 125 °C, the Cu/SiO$_x$-stacked sample shows disappointing

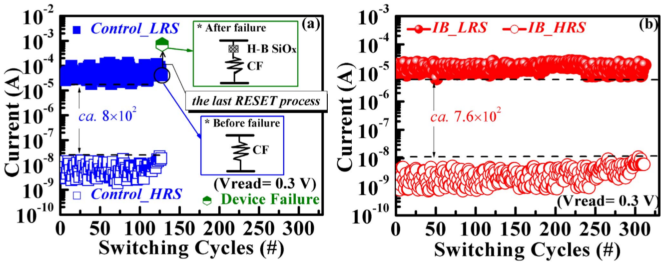

Fig. 4. Switching endurance characteristics of (a) the Cu/SiO$_x$-stacked (control sample) and (b) IB-induced SiO$_x$:Cu (IB sample) SLs under pulse-voltage cycles. To ensure that every resistance switching is working, the conditions of RESET/SET pulses for control and IB samples were (−5.5 V at 80 μs / 6.4 V at 300 μs) and (−3.7 V at 80 μs / 5.3 V at 300 μs), respectively.

high-temperature retention properties, as shown in Fig. 3(a). The HRS current of Cu/SiO$_x$-stacked sample increases abruptly after 3 × 10^3 s at 125 °C. It leads the HRS to return to the LRS suddenly. Fig. 3(b) shows cell-to-cell statistical distribution of the maintainable LRS/HRS ratio after 125 °C for 10^5 s thermal stress. By contrast, the IB-induced SiO$_x$:Cu SL exhibits excellent high-temperature retention properties. The LRS/HRS ratio of IB-induced SiO$_x$:Cu SL is still maintained *ca.* 1.4 × 10^3 for 10^5 s at 125 °C. The improvement in high-temperature retention is attributed to the limited Cu source and the elimination of Cu electrode [10], [12].

In previous reports, the SiO$_x$-based CF ReRAM generally showed incompetent switching endurance characteristics. For the SiO$_x$-based CF SL fabricated by general method, the number of resistance switching cycles has been *ca.* 100 [4], [5]. Fig. 4(a) and (b) shows switching endurance characteristics of the Cu/SiO$_x$-stacked and IB-induced SiO$_x$:Cu SLs, respectively. It is seen that the Cu/SiO$_x$-stacked sample shows disappointing endurance properties such as the conventional SiO$_x$-based CF SL. After *ca.* 130 switching cycles, a phenomenon of resistance switching failure is caused, which prevents LRS from returning to HRS. In the last RESET process, resistance decreases instead of increases. After that, the sample lies in LRS permanently. It could be ascribed to switching-gap SiO$_x$ hard-breakdown. Frequent RESET/SET stresses destroy the switching gap. Additionally, resistance temperature coefficient (RTC) of the LRS before failure can be estimated to 2.36 × 10^{-3} K^{-1}. This shows the LRS resistance before failure is mainly composed of CF [8]. After the switching-gap SiO$_x$ hard-breakdown, however, it is found that the relation between resistance and temperature is changed from linear to nonlinear relationships. That is because the LRS resistance after failure is composed of ruptured CF in series with Si deficiencies. The RTCs of Cu and Si are opposite polarity. By contrast, the IB-induced SiO$_x$:Cu SL exhibits better endurance properties. The improvement in endurance is attributed to the decrease in RESET voltage and the increase in uniformity of switching voltages. The low switching voltages significantly extend lifetime of the switching gap. Although the maximum of resistance switching cycles of IB-induced SiO$_x$:Cu SL is *ca.* 312, so far these endurance properties have been the most promising for the general SiO$_x$-based CF ReRAM [4], [5].

IV. CONCLUSION

We used the novel IB-induced Cu-doping technique to replace the use of conventional Cu electrode for SiO$_x$-based CF SL. Compared with the conventional Cu/SiO$_x$-stacked sample, this IB-induced SiO$_x$:Cu SL exhibits superior performance, including lower forming/RESET voltages, higher uniformity of SET/RESET voltages, and better high-temperature retention properties. These improvements in performance are attributed to the limited Cu source and the elimination of Cu electrode. Additionally, this IB-induced TaN/SiO$_x$:Cu/TaN device has shown the most promising switching endurance properties for the general SiO$_x$-based CF ReRAM thus far. This is due to the low and uniform switching voltages significantly increasing the lifetime of switching gap. For future development of SiO$_x$-based CF ReRAM, therefore, how to effectively enhance the lifetime of switching gap would be an important issue.

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