

A 0.6-V 0.33-mW 5.5-GHz Receiver Front-End Using Resonator Coupling Technique

Chun-Hsing Li, *Student Member, IEEE*, Yen-Lin Liu, and Chien-Nan Kuo, *Member, IEEE*

Abstract—In this study, a low-power and low-voltage 5.5-GHz receiver front-end circuit is designed using a resonator coupling technique. An on-chip transformer combined with the parasitic capacitances from a low-noise amplifier (LNA), a mixer, and the transformer itself comprises two coupled resonators of the resonator coupling network (RCN). The RCN functions as a balun, and couples energy from the LNA to the mixer. Under the critical coupling condition, the RCN gives a maximal current gain at resonance frequencies, equivalent to the same level by an ideal transformer. The analysis shows that the current gain is quite tolerable to the coupling coefficient variation, an advantageous feature for on-chip transformer design. The technique is verified by the receiver front-end in 0.18- μm CMOS technology. The RCN possess a current gain as high as 12 dB at 5.5 GHz. The measured input return loss, conversion gain, and third-order intermodulation intercept point of the entire circuit are 16 dB, 17.4 dB, and -1.5 dBm, respectively. The noise figure is 7.8 dB at the IF frequency of 1 MHz. The power consumption is only 0.33 mW from a 0.6-V supply. The required local oscillator power is only -9.5 dBm. This receiver front-end successfully demonstrates the resonator coupling technique.

Index Terms—Balun, low-noise amplifier (LNA), low power, low voltage, mixer, resonator coupling network (RCN), transformers.

I. INTRODUCTION

ULTRA-LOW power consumption is essential to numerous emerging applications in wireless communications with portable devices. It is especially critical to wireless sensor networks to allow long lasting use of sensor nodes, fixed or portable, without battery replacement after installation. This helps ubiquity in data collection, such as personal healthcare inspection in wireless body-area networks (WBANs) or alarm sensing in intelligent buildings. As pointed out in [1], average power consumption shall be limited to be in the order of $10 \mu\text{W}$ to ensure appropriate battery lifetime extension. This calls for maximum power consumption less than few milliwatts in low duty-cycle wireless data transmissions [2]. Published literature shows that the measured baseband power consumption can

be as low as a few tens of microwatts [3]. Since RF front-end circuits typically consume much more than that of the baseband circuitry, it is therefore worthy of great effort on power reduction in the RF circuits.

Low supply voltage is an effective method to reduce power consumption. It also meets the technology trend of scaling down gate length and increases the possibility of using a single solar-cell source of 400 mV. Consequently, the popular cascode topology that utilizes current reuse is inappropriate. The folded topology with two dc current paths also needs careful design to reduce the total current level.

Different techniques have been applied to the ultra-low power receiver design. The receiver front-end operated at 2.4 GHz and adopts a differential passive mixer without any low-noise amplifier (LNA) [1]. Although a passive topology consumes less power, it does not contribute conversion gain and it may need more power consumption in the latter stage to provide an adequate gain to the entire circuit. In [2], a dual-conversion receiver is implemented at 900 MHz using a self-biased CMOS-inverter LNA with a supply voltage of 1.6 V. Yet the circuit calls for a high supply voltage, not suitable for low-voltage application. Common-gate LNA as a transconductance of the mixer is employed in another approach using fully differential design [4]. The front-end circuitry, however, uses a cascode topology, inappropriate for low supply voltage.

The technique of using a transformer is an alternative in the front-end circuit design [5]. Placed between the LNA and mixer, a transformer not only acts as a balun, but also provides a voltage gain or a current gain. An ideal lossless transformer calls for a coupling coefficient k of unity and an inductance value of infinity. The theoretical current gain relies on the coil turn ratio n , a frequency-independent quantity to achieve the maximal power transfer condition. Hence, a high turn ratio is desired to supply a high gain. For instance, n of 4 is used in [6]. In practice, however, k of an on-chip transformer cannot easily achieve unity [7]. A high turn ratio also usually causes a low self-resonance frequency because of large parasitic capacitance. Moreover, a transformer with a high turn ratio usually occupies a large area, which increases the cost dramatically. Consequently the current gain is very limited.

In this work, the resonator coupling technique is applied to overcome the aforementioned disadvantage of using a transformer alone. The resonator coupling network (RCN) can provide a high current gain at resonance, in addition to the single-to-differential conversion. The RCN has been applied to implement a wideband LNA [8], a wideband multimode voltage-controlled oscillator (VCO) [9], [10], and a low-power downconversion mixer [11]. Nevertheless, the physics behind it is not well

Manuscript received September 24, 2010; revised February 20, 2011; accepted February 25, 2011. Date of publication April 11, 2011; date of current version June 15, 2011. This work was jointly supported by the National Science Council, Taiwan, under Grant NSC 98-2220-E-009-064 and the Ministry of Economic Affairs (MOEA) under Project 98-EC-17-A-03-S1-005.

C.-H. Li and C.-N. Kuo are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: chli.ee99g@nctu.edu.tw; cnkuo@mail.nctu.edu.tw).

Y.-L. Liu was with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan. She is now with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan (e-mail: ylliu@tsmc.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2011.2130534

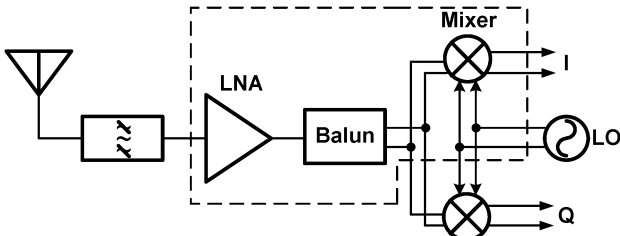


Fig. 1. Direct downconversion receiver front-circuit under consideration, including the LNA, balun, and mixer. The balun is implemented by an RCN.

explained. It will be shown soon that the RCN gives the same maximal current gain (MCG) as an ideal transformer in the critical coupling condition.

A low-power receiver front-end is designed in 0.18- μm RF CMOS technology. The circuit is for the application of wireless sensor nodes operated at the 5-GHz industrial–scientific–medical (ISM) unlicensed frequency band. Several techniques are combined to achieve sub-milliwatt power consumption, including the folded topology with 0.6-V low supply voltage and the RCN for signal current gain. The device biasing condition is optimized by inspecting a composite figure of merit (FOM). A guideline is introduced for design optimization. All the design efforts successfully ensure low power consumption. In Section II, design consideration of each sub-circuit is discussed. The measurement data are presented and summarized in Section III. Finally, Section IV concludes this paper.

II. DESIGN CONSIDERATION

The receiver front-end architecture under consideration is shown in Fig. 1. The direct conversion architecture is adopted for the concern of the minimal number of components. This architecture eliminates the need of an image filter. Circuit blocks inside the dashed box are designed, including an LNA, a balun, and a double-balanced mixer. Applied to the sensor node of short-distance body-area networks, the receiver does not require a high sensitivity level. On the other hand, power constraint is the major concern in order to prolong the battery life. From the viewpoint of system design, most of the gain budget shall be assigned to the LNA, and therefore it contributes the most to power consumption.

Fig. 2 shows the proposed front-end circuit, which makes use of the resonator coupling technique. For the supply voltage as low as 0.6 V, it calls for a single-transistor microwave amplifier for the LNA [12] to avoid transistor stacking. However, the low supply voltage may limit the linearity due to small voltage headroom. Therefore, LNA signaling is preferred to be in the current domain. The LNA is single-ended to account for the typical antenna configuration. It takes a balun to convert signals into the differential form for better noise immunity in the receiver path. The differential currents at the balun output are commuting by the switching stages of the mixer for the purpose of frequency conversion. The self-mixing issue related to local oscillator (LO)-to-RF isolation in the mixer design is critical to receivers adopting the direction conversion architecture. Since LO leakages appear out of phase in the double-balanced mixer input, LO-to-RF isolation is high and the self-mixing issue is minimized.

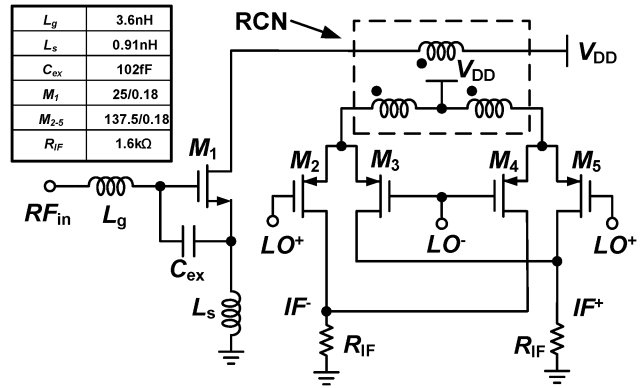


Fig. 2. Circuit schematic of the receiver front-end, including a single transistor LNA, a double-balanced mixer, and an RCN functioned as a balun and provides current gain.

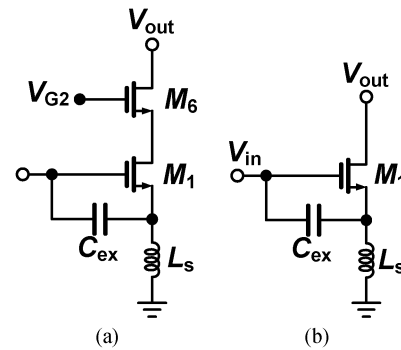


Fig. 3. (a) Cascode LAN circuit. (b) Single-transistor LNA for low supply voltage.

Although active implementation of a balun [13], [14] contributes signal gain, they consume dc power while contributing additional noise to the receiver front-end. On the other hand, passive transformers, causing no dc voltage drop, are attractive in this power-constraint project. The proposed RCN not only functions as a balun, but also provides current amplification by impedance transformation without power consumption. Moreover, the dc block characteristic allows the LNA and the mixer connected in a folded topology. Low supply voltage is therefore feasible.

In this design, only the mixer in the in-phase (I) channel is designed. Another mixer for the quadrature (Q) channel can be implemented similarly. Offering I and Q signal channels might be viable to realize modern modulation schemes in some reliability-critical applications such as healthcare monitoring.

A. LNA Circuit Design

As shown in Fig. 3(a), the conventional cascode configuration has good stability and high reverse isolation [15]. The minimum dc biasing at the output node, however, is limited to keep both transistors at saturation [16]. The low supply voltage of 0.6 V yields to insufficient headroom to sustain good linearity performance. As mentioned in [17], a larger effective voltage results in higher linearity of a transistor. This leads to the design using a single transistor, as shown in Fig. 3(b). The external components, C_{ex} and L_s , allow the LNA to simultaneously achieve power matching and noise matching [18].

The transistor M_1 shall be biased optimally to take into account several requirements such as gain, linearity, noise performance, and power consumption. The fundamental device parameters include drain current I_D , transconductance g_m , cutoff frequency f_T , and minimum noise figure (NF) NF_{\min} . Instead of simply biasing the transistor in the weak inversion, as in [19] for low-power purpose, it is better to inspect an overall FOM to find the optimal biasing condition.

Several FOM definitions are first reviewed to determine the bias condition. The FOM of g_m/I_D evaluates the conversion efficiency of dc power to transconductance, or gain, and usually leads to the biasing condition in the weak inversion region [20]. For RF design, the FOM of $g_m f_T/I_D$ was proposed to include f_T , taking the device frequency response into consideration [21]. This FOM represents the gain-bandwidth product to evaluate the performance of the high-frequency circuit. Furthermore, it is also critical to include the linearity and noise performance as far as an LNA circuit is concerned. Since the FOM of a tuned LNA is usually defined as [22]

$$\text{FOM}_{\text{LNA}} = \frac{G \times \text{IIP}_3 \times f}{(\text{NF} - 1) \times P_{\text{DC}}} \quad (1)$$

it is then meaningful to define a FOM for transistor biasing as

$$\text{FOM}_{\text{MOS}} = \frac{g_m \times \text{IIP}_{3,\text{MOS}} \times f_T}{(\text{NF}_{\min} - 1) \times I_D} \quad (2)$$

where $\text{IIP}_{3,\text{MOS}}$ represents the device third-order linearity under a given bias condition without any impedance matching network.

Fig. 4(a) and (b) plots each device parameter and FOM of an nMOS transistor, respectively, with respect to the current density under the supply voltage of 0.6 V. The optimal FOM position is dependent on R_L , the LNA load resistance, since it affects the linearity performance due to the nonlinearity of the output conductance g_o . As R_L is small, IIP_3 is dominated by the nonlinearity of g_m . When R_L becomes large, the nonlinearity of g_o becomes remarkable, and tends to cancel the g_m nonlinearity at smaller V_{GS} . Larger R_L could give higher $\text{IIP}_{3,\text{MOS}}$, but the result is more sensitive to bias current. Therefore, given the effective loading resistance from the RCN, current density is chosen as $8.8 \mu\text{A}/\mu\text{m}$ in the final design, somewhat adjusted to optimize the overall performance.

One major concern of the single-transistor LNA is the stability issue. The electrical feedback due to the gate–drain capacitance C_{gd} is significant such that bilateral amplifier design is necessary. This undesired feedback causes the amplifier to appear as conditionally stable at 5.5 GHz. The load stability circle typically cuts into the upper region of the Smith chart, as shown in Fig. 5, which means a capacitive load is preferred to avoid instability. An inductive load, however, is necessary to tune out the capacitive output impedance at the drain port to enlarge the gain level. To the cascode LNA circuit in Fig. 3(a), this is not an issue at all since the load impedance presented by the common-gate M_6 transistor is low and capacitive. Not only the Miller feedback of C_{gd} is decreased, but also the load impedance sits in the stable region.

To alleviate the stability issue, the transistor shall be stabilized by adding external components without much degradation

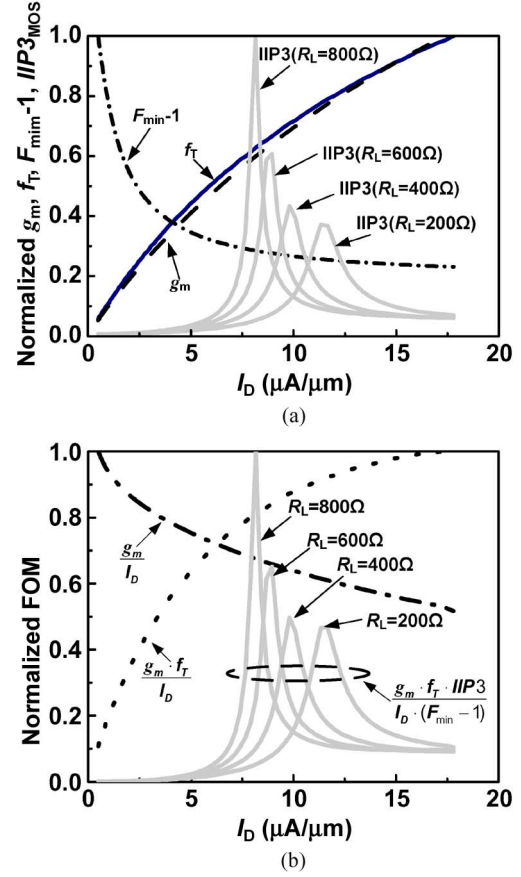


Fig. 4. (a) Variation of each device parameter versus the drain current density. (b) Calculated FOMs to determine the biasing condition. Each FOM has been normalized to the highest value within the supply current range.

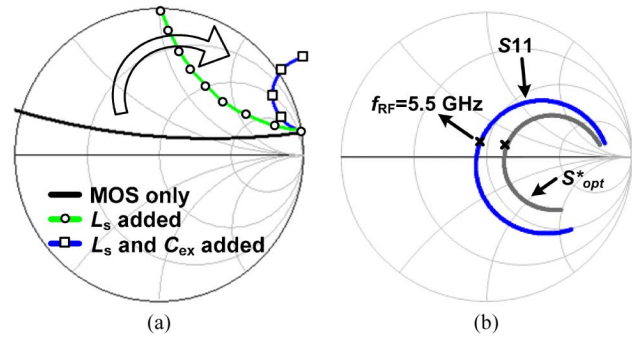


Fig. 5. (a) Load stability circles of the single-transistor LNA at 5.5 GHz with and without reactive stabilization. (b) Smith chart showing the noise and power matching when C_{ex} and L_s are included. S_{opt}^* means the complex conjugate of S_{opt} .

to the noise performance. It turns out that the two reactive components, the gate–source capacitor C_{ex} and the source inductor L_s , also benefit stabilization. Fig. 5(a) shows that the load stability circles move out of the Smith chart after adding L_s of 0.91 nH and C_{ex} of 0.1 pF. This gives room for impedance matching without the stability concern. In addition to the operating frequency, the stability condition is inspected over a large frequency range from 100 MHz to 10 GHz to ensure that the LNA is stable. C_{ex} and L_s also help the LNA to achieve noise

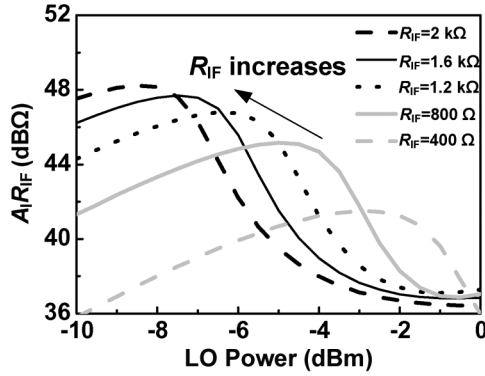


Fig. 6. Conversion trans-impedance gain versus LO power for different load resistances. A_I is the current conversion gain from the mixer input to IF output. LO power is referred to 50Ω .

and power matching at the frequency of interest, as illustrated in Fig. 5(b).

The output resistance of the LNA should be as high as possible to possess a high MCG while the transistor still stays in the best FOM. Consequently the LNA size is chosen as $25 \mu\text{m}$ to present the output resistance and capacitance of $7.68 \text{ k}\Omega$, and 30 fF , respectively.

B. Mixer Circuit Design

A double-balanced mixer is preferred for better port-to-port isolation and less even-order distortion. The latter is especially critical in the direct downconversion receiver.

The mixer circuit typically consists of a transconductor stage and a current-switching stage, such as the Gilbert cell. The transconductor transfers the RF input voltage into current. In this design, the LNA is directly utilized as the transconductor. The scheme can reduce the required power consumption. The switching stage (M_{2-5}) performs current switching for frequency conversion. pMOS transistors are chosen in the switching pair due to their lower flicker noise as compared to nMOS transistors. Ideally only one switching path of the switching stage is on at a time. Nonideal switching, however, degrades circuit performance, such as gain and noise contribution. To make the switching more ideal, a large transistor is chosen and the biasing point is set near threshold voltage. Such biasing reduces power consumption. Although it may degrade the noise performance, a high NF is tolerable for the application to wireless sensor networks.

Consideration of mixer optimization is twofold. One is to maximize the trans-impedance conversion gain, and the other is to lower the required LO level. The former typically calls for a large LO level. The latter is important to decrease the power consumption in the LO generation circuit. The optimization relies on careful choice of the load resistance R_{IF} .

Fig. 6 shows the conversion gain of the mixer under different R_{IF} values versus LO power for the given V_{SG} bias of 0.44 V . The LO power is referred to $50\text{-}\Omega$ impedance. The maximum conversion gain tends to be larger for larger R_{IF} , and the LO power for the maximum gain moves toward a smaller value. If the V_{SG} bias of pMOS becomes larger, the LO power for the maximum gain can be even smaller. The largest R_{IF} is actually

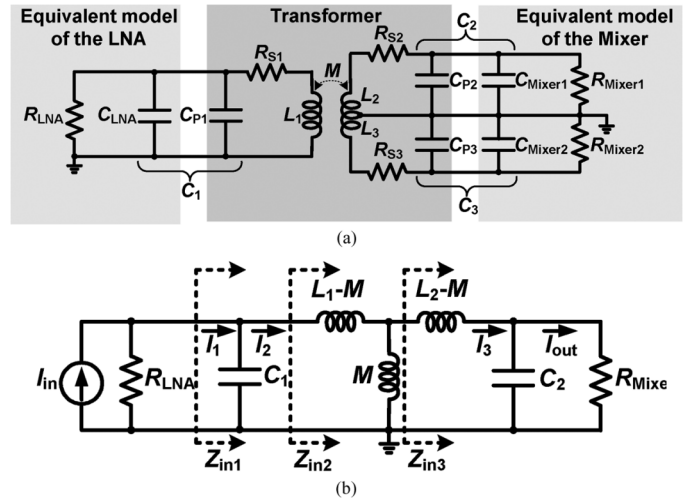


Fig. 7. (a) Proposed RCN and (b) equivalent circuit of the RCN consisting of the equivalent models of the LNA, mixer, and transformer.

limited by linearity performance. R_{IF} is selected as $1.6 \text{ k}\Omega$ in this design. The required LO power is -6.5 dBm for the maximum gain, but it is determined as -9 dBm for the sake of better tradeoff between gain and linearity, with a decrease of 1.4 dB in the gain level.

The input resistance of the mixer is required to be small for a high current gain, which, in turn, calls for high g_m in M_{2-5} . The value of g_m is chosen as 3.62 mA/V to make a tradeoff between the LO power and RCN gain. Hence, the transistor size is chosen as $137.5 \mu\text{m}$, resulting in the resistance of 276Ω and the capacitance of 100 fF at the mixer input.

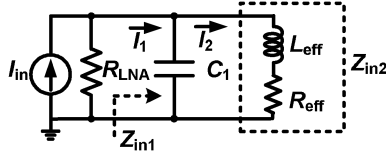
C. RCN Formulation

Between the LNA and mixer, an RCN needs to be designed carefully to convert the single-ended RF signal into the differential form, while it also provides a high current gain by impedance transformation.

In the proposed front-end, the RCN can be modeled as illustrated in Fig. 7(a). One resonator (L_1 and C_1) is connected to the output of the LNA, and two resonators (L_2 , C_2 , L_3 , and C_3) are connected to the mixer input using a center-tapped coil. The magnetic coupling in the transformer transfers the current signal from one resonator to the others. The mutual inductance between the primary and secondary coils is designated as M . The coupling coefficient k is defined as

$$k \equiv \frac{M}{\sqrt{L_1 L_2}}. \quad (3)$$

$C_{P1}, C_{P2}, C_{P3}, R_{S1}, R_{S2}$, and R_{S3} represent the parasitics of the transformer. The LNA output impedance and the mixer input impedance are modeled by R_{LNA} , C_{LNA} , R_{Mixer} , and C_{Mixer} , respectively. Since the transformer is symmetric to the virtual ground of the secondary coil, the RCN can be analyzed by a two-port network, as shown in Fig. 7(b), without loss of generality. The coupled coils are replaced with an equivalent T-circuit. The ohmic resistors R_{S1} and R_{S2} are neglected to simplify the analysis. Therefore, the RCN includes the parasitics of the LNA, mixer, and transformer.


 Fig. 8. Equivalent circuit of that in Fig. 7(b) for the analysis of I_2/I_1 .

The current gain $G(s)$, I_{out}/I_{in} of the RCN can be derived by current division formulation at each node using the impedances Z_{in1} , Z_{in2} , and Z_{in3} . In [11], the design parameters of an RCN are obtained by numerical simulations. The current gain formula appears too complicated to give much insight. Actually it will be shown soon that the MCG condition only depends on the ratio of the LNA output resistance to the mixer input resistance. For convenience, ω_1 and ω_2 are defined as the resonant frequencies of those two uncoupled resonators with the frequency ratio of m ,

$$\omega_1 \equiv \frac{1}{\sqrt{L_1 C_1}} \quad \omega_2 \equiv \frac{1}{\sqrt{L_2 C_2}} \quad \text{and} \quad \omega_1 \equiv m\omega_2. \quad (4)$$

In the coupled network, the natural resonance frequencies can be expressed in term of m , k , and ω_2 as

$$\omega_L = \omega_2 \sqrt{\frac{1 + m^2 - \sqrt{m^4 + 2(2k^2 - 1)m^2 + 1}}{2(1 - k^2)}} \quad (5)$$

$$\omega_H = \omega_2 \sqrt{\frac{1 + m^2 + \sqrt{m^4 + 2(2k^2 - 1)m^2 + 1}}{2(1 - k^2)}}. \quad (6)$$

At these two natural resonance frequencies, signal can be coupled from the LNA into the RCN, and transferred to the mixer in the most efficient manner. Either one can be chosen as the circuit operating frequency, designated as ω_o hereafter. In the following analysis, it is assumed that the quality factors of Z_{in1} , Z_{in2} , and Z_{in3} are large enough, higher than 3.

The current division ratio of I_1/I_{in} at resonance is determined by Z_{in1} , and can be derived as

$$\begin{aligned} \left| \frac{I_1}{I_{in}} \right|_{\omega_H, \omega_L} &= \frac{R_{LNA}}{R_{LNA} + Z_{in1}|_{\omega_H, \omega_L}} \\ &= \frac{R_{LNA}}{R_{LNA} + \left[\frac{nm^2(1-r^2)}{k} \right]^2 R_{Mixer}} \end{aligned} \quad (7)$$

where r is the frequency ratio of ω_o normalized to ω_2 and n is the transformer turn ratio defined as

$$n \equiv \sqrt{\frac{L_1}{L_2}}. \quad (8)$$

Z_{in1} at resonance increases rapidly when k is small and n is high. Thus, high magnetic coupling and a low turn ratio are desired to make I_1/I_{in} close to the maximal value of 1.

The current gain I_2/I_1 is derived using the resonator quality factor. As illustrated in Fig. 8, Z_{in2} can be modeled as an in-

ductor L_{eff} and a resistor R_{eff} in series. Hence, the current gain at resonance is simply the quality factor Q_1 of the resonator of L_{eff} and C_1 , acquired as

$$\left| \frac{I_2}{I_1} \right|_{\omega_H, \omega_L} = Q_1 = \frac{\omega_o L_{eff}}{R_{eff}} = \left(\frac{R_{Mixer}}{\omega_o L_2} \right) \left[\frac{m(1-r^2)}{k} \right]^2. \quad (9)$$

Note that I_2/I_1 depends linearly on R_{Mixer} and increases as k decreases, in agreement with the trends to improve Q_1 . That is, it is preferred to make weak magnetic coupling to enlarge the current gain I_2/I_1 . The opposite requirements on k to optimize I_2/I_1 and I_1/I_{in} result in an optimal k value to achieve the maximal total gain.

I_3/I_2 can be obtained by current division of M and Z_{in3} . Actually, the maximum gain of I_3/I_2 occurs at the resonance frequency ω_2 of the resonator comprised by M and Z_{in3} and equals to the tank quality factor Q_2 at ω_2 . Since the circuit operating frequency ω_o deviates from ω_2 , I_3/I_2 becomes somewhat less. It can be derived as

$$\begin{aligned} \left| \frac{I_3}{I_2} \right|_{\omega_H, \omega_L} &= \omega_o M \sqrt{\frac{1 + \omega_o^2 C_2^2 R_{Mixer}^2}{R_{Mixer}^2 (1-r^2)^2 + \omega_o^2 L_2^2}} \\ &\approx \frac{\omega_o M}{R_{Mixer} (1-r^2)} \sqrt{1 + \omega_o^2 C_2^2 R_{Mixer}^2}. \end{aligned} \quad (10)$$

The approximation is valid since $\omega_o^2 L_2^2 \ll R_{Mixer}^2 (1-r^2)^2$ in the frequency band of interest. Finally, I_{out}/I_3 is given by

$$\left| \frac{I_{out}}{I_3} \right|_{\omega_H, \omega_L} = \frac{1}{\sqrt{1 + \omega_o^2 C_2^2 R_{Mixer}^2}}. \quad (11)$$

It can be observed from (10) and (11) that the effects of C_2 on the total gain cancel with each other, indicating that the maximum current gain level is independent of C_2 .

The total current gain I_{out}/I_{in} can be obtained simply by multiplying (7) and (9)–(11) together

$$\begin{aligned} \left| \frac{I_{out}}{I_3} \right|_{\omega_H, \omega_L} &= \frac{\overbrace{\left| \frac{I_1}{I_{in}} \right|_{\omega_H, \omega_L}}}{R_{LNA} + \left[\frac{nm^2(1-r^2)}{k} \right]^2 R_{Mixer}} \\ &\quad \times \frac{\overbrace{\left| \frac{I_{out}}{I_1} \right|_{\omega_H, \omega_L}}}{\sqrt{1 + \omega_o^2 C_2^2 R_{Mixer}^2}} \\ &\quad \times \frac{\overbrace{\left| \frac{I_3}{I_2} \right|_{\omega_H, \omega_L}}}{\sqrt{1 + \omega_o^2 C_2^2 R_{Mixer}^2}}. \end{aligned} \quad (12)$$

It is more convenient for design to replace m with other quantities by using (5) and (6). The total gain can be rewritten as

$$\begin{aligned} \left| \frac{I_{out}}{I_{in}} \right|_{\omega_H, \omega_L} &= \frac{R_{LNA}}{R_{LNA} + \left\{ \frac{n}{k} [1 - (1 - k^2)r^2] \right\}^2 R_{Mixer}} \\ &\quad \times \frac{n}{k} [1 - (1 - k^2)r^2] \\ &= \frac{AR_{LNA}}{R_{LNA} + A^2 R_{Mixer}}, \end{aligned} \quad (13)$$

where $A \equiv \frac{n}{k} [1 - (1 - k^2)r^2]$.

TABLE I
COMPARISON BETWEEN THE REQUIREMENT OF THE
TRANSFORMER AND THE RCN FOR MCG

Parameter	Transformer	RCN
n	Constrained to $\sqrt{R_{LNA}/R_{Mixer}}$	$< \sqrt{R_{LNA}/R_{Mixer}}$
k	1	< 1
$f_{\text{self-resonance}}$	As high as possible	Medium*
Bandwidth	Broadband	Narrowband
Area	Large	Small
MCG	$\frac{1}{2}\sqrt{R_{LNA}/R_{Mixer}}$	$\frac{1}{2}\sqrt{R_{LNA}/R_{Mixer}}$

* The parasitic capacitance of the transformer can be absorbed into the design.

Consider the case if an ideal transformer with the turn ratio t is applied as the balun. The current gain follows the impedance transformation as

$$\left| \frac{I_{\text{out}}}{I_{\text{in}}} \right|_{\text{transformer}} = \frac{tR_{LNA}}{R_{LNA} + t^2R_{Mixer}}. \quad (14)$$

The maximum value is $t/2$ when $R_{LNA} = t^2R_{Mixer}$ or in the impedance match condition. The value can hold up over a wide frequency range.

In the RCN case, the on-chip coupling coefficient k hardly achieves unity as an ideal transformer. To explore the MCG condition, (13) is differentiated with respect to n and k . It leads to the result

$$R_{LNA} = Z_{\text{in}}|_{\omega_o} = \frac{n^2}{k^2} [1 - (1 - k^2)r^2]^2 R_{Mixer}. \quad (15)$$

Essentially it represents impedance matching at the LNA output. It also meets the critical coupling condition that energy is coupled from the LNA to the RCN with the highest efficiency. The impedance match condition also holds at the mixer input. This can explain why the RCN presents the MCG at resonance frequencies. Given the critical coupling condition, the MCG is

$$\left| \frac{I_{\text{out}}}{I_{\text{in}}} \right|_{\text{max}, \omega_H, \omega_L} = \frac{1}{2} \sqrt{\frac{R_{LNA}}{R_{Mixer}}}. \quad (16)$$

The results of those two cases are very interesting. The MCG is determined only by the ratio of R_{LNA} and R_{Mixer} . Although $k < 1$, the maximum gain of the RCN gets to the same result as an ideal transformer if n and k are chosen properly by (15) without the condition of $k = 1$ and infinite inductance. This greatly eases the design of an on-chip transformer where unity k is very unlikely to be realized. Furthermore, it is also possible that the turn ratio n of the RCN is smaller than t , which is constrained by $R_{LNA} = t^2R_{Mixer}$. The advantage simply comes from the tradeoff of bandwidth. The comparison between the requirement of the transformer and the RCN designed for MCG is summarized in Table I to emphasize the benefits of using the RCN.

D. RCN Design

By designing the LNA and mixer to have a high resistance ratio of R_{LNA}/R_{Mixer} , the RCN can give a high current gain without any power consumption. As aforementioned, R_{LNA} is 7.68 k Ω and R_{Mixer} is 276 Ω . The design goal is an MCG at

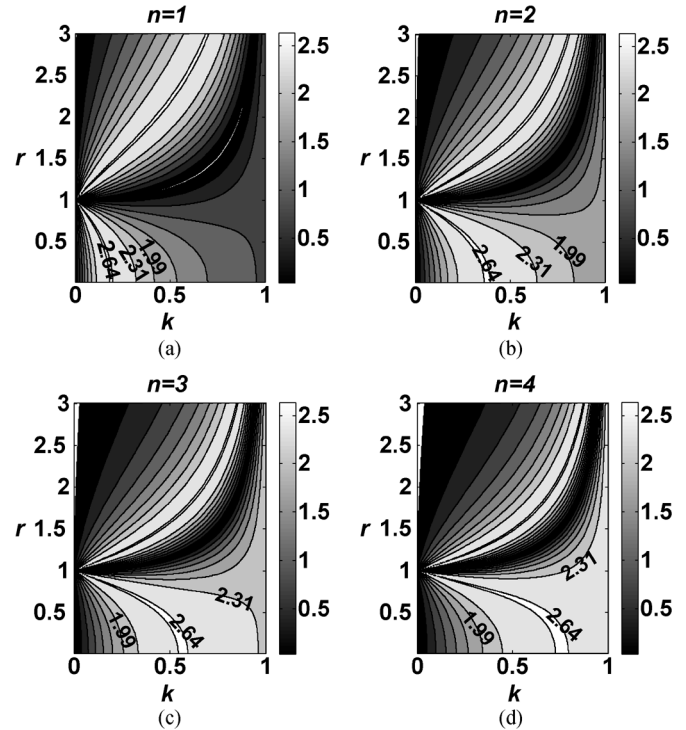


Fig. 9. Contour plots of the current gain with respect to the coupling coefficient k and r . (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, and (d) $n = 4$.

the center frequency ω_o of 5.5 GHz. If designed by an ideal transformer, the required turn ratio is larger than 5.

RCN design is governed by (13) and (15). Current gain is generally determined by (13). If the combination of n , r , and k deviates from the condition of (15), the critical coupling fails. Indeed there are infinite solutions of the combination. A contour plot of the current gain can be exploited to optimize the RCN design. Fig. 9 illustrates the contour plots in various n values from 1 to 4 over the range of r from 0 to 3. Note that the regions of $r \leq 1$ and $r > 1$ correspond to the cases of $\omega_o = \omega_L$ and $\omega_o = \omega_H$, respectively. It can be observed that the MCG reaches the ideal value of 2.64 calculated by (16), no matter what the n value is. It can be also found that the MCG occurs in both $r < 1$ and $r > 1$, different from that in [11], where only $r < 1$ is chosen to obtain a higher gain. When $r > 1$, however, the bandwidth appears to be narrow, and it is not easy to implement the element values on chip. Moreover, the contour lines change more slowly when $r < 1$, indicating that the current gain is less sensitive to k variation. It is, therefore, preferred to choose $r < 1$, i.e., ω_o is designed at ω_L . More specifically, r is chosen around 0.5 in this work.

The RCN input impedance over the frequency of interest affects LNA linearity, as demonstrated in Fig. 4. In order to investigate the influence of the RCN parameters on the LNA linearity, the contour plot of the RCN input impedance is plotted in Fig. 10. The RCN input impedance shows a similar trend as that of the current gain. When n is larger and r is smaller, the impedance is less susceptible to k variation, and so does the LNA linearity. Furthermore, Fig. 4 shows that the LNA bias current remains similarly for the highest third-order intermodulation intercept point (IIP3) when R_L is large. If the implemented

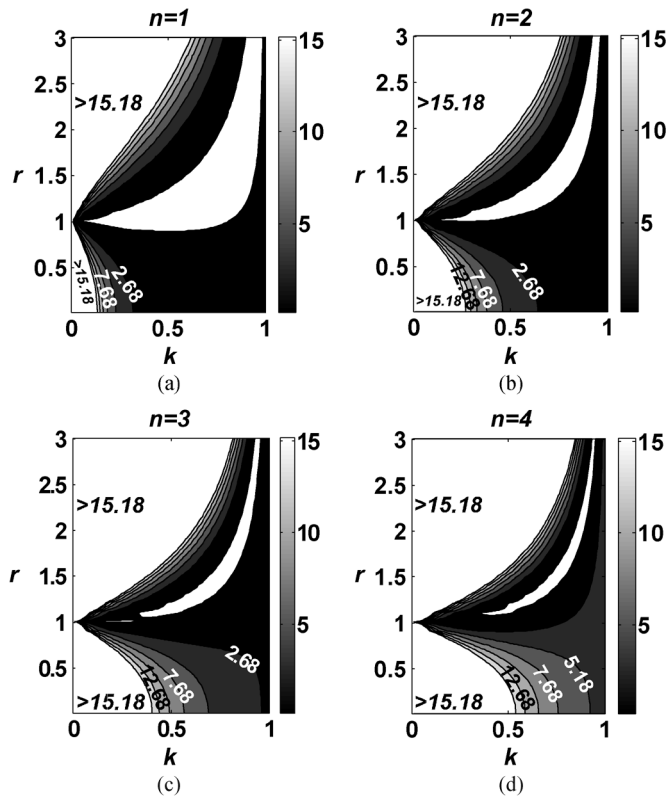


Fig. 10. Contour plots of the RCN input impedance with respect to the coupling coefficient k and r . (a) $n = 1$, (b) $n = 2$, (c) $n = 3$, and (d) $n = 4$. The unit is $k\Omega$.

RCN does not translate exactly optimal load to the LNA, the LNA bias can be finely tuned for higher IIP3.

The design flow of the RCN can be arranged as follows. First, n is selected as 3. The optimal coupling coefficient k is obtained to be 0.46 by (15), but it can range from 0.4 to 0.7 without much degradation of the current gain according to Fig. 9(c). The ratio m of 0.52 then can be determined from (5). With r and m known, ω_1 and ω_2 are also decided to be 5.72 and 11 GHz, respectively. L_1 and L_2 are related by the turn ratio n . With the consideration of on-chip transformer feasibility, L_1 and L_2 are designed as 4.5 and 0.5 nH, respectively. Finally, C_1 and C_2 are determined as 172 and 418 fF, respectively. Since the values of C_1 and C_2 are close to the total parasitic capacitances from the resonators, LNA, and mixer, no additional capacitor is required. The design flow is summarized in Fig. 11.

The designed transformer is shown in Fig. 12, where the p_1 port of the primary coil is connected to the LNA, and p_2 and p_3 of the secondary are linked to the double-balanced mixer. The design needs to meet the high difference ratio of L_1 and L_2 . The width w_2 of the secondary coil is set as $10\ \mu\text{m}$, and w_1 of the primary is $8\ \mu\text{m}$. The outside dimension (OD) is designed as $260\ \mu\text{m}$ such that the line length reaches the self-inductance requirements of L_1 and L_2 . The square root of the physical turn ratio is only 2. When the mutual inductance is taken into consideration, the effective turn ratio is expected to be close to the required value of 3. Since the transformer allows significant k variation, the spacing s of $2\ \mu\text{m}$ is chosen to make the occupied area as small as possible. It takes the electromagnetic (EM) simulator of

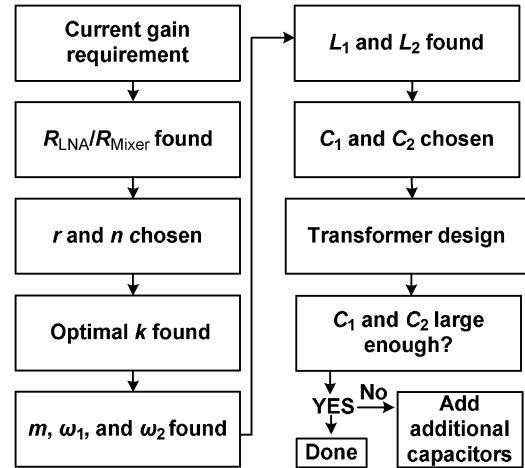


Fig. 11. Design flow for RCN design.

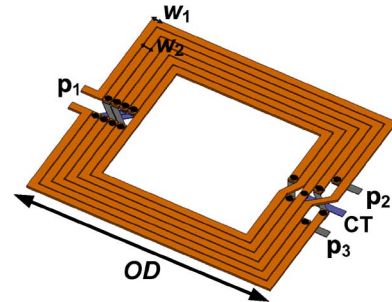


Fig. 12. Proposed transformer in the RCN. w_1 and w_2 are the width of primary and secondary inductors, respectively. OD is the outside dimension.

Ansoft Designer only a few moments of iteration to determine the final physical dimension.

The extracted parameters from the EM simulation yield to k of 0.64, n of 2.76, L_1 of 4.41 nH, and L_2 of 0.58 nH. The difference between the desired and implemented values of n and k is quite tolerable for the current gain design. Nevertheless, the parasitic ohmic resistance, R_{S1} of $8.04\ \Omega$ and R_{S2} of $2.41\ \Omega$, causes the MCG to further drop down to 2.1. Thus, the RCN differentially provides a current gain of 4.2 (~ 12 dB).

Although n of 3 is demonstrated in this design, small n as 1 as one and small k of 0.14 are sufficient to achieve the MCG. Consequently, the chip area can be smaller than that by using an ideal transformer. The tradeoff is an accurate design of the coupling coefficient k .

III. EXPERIMENTAL RESULTS

The front-end circuit is fabricated in Taiwan Semiconductor Manufacturing Company (TSMC) $0.18\text{-}\mu\text{m}$ RF CMOS technology. The micrograph is shown in Fig. 13. The die size is $1.16 \times 0.75\ \text{mm}^2$, including bonding pads. Measurements were conducted by chip-on-board setup. DC pads are wire-bonded on a printed circuit board (PCB) board. High-frequency signals are through on-wafer probing with a ground-signal-ground (GSG) probe for the RF input and a ground-signal-ground-signal-ground (GSGSG) probe for the LO signal. The differential IF output signal is converted to a single-ended form by an on-board OP amplifier with

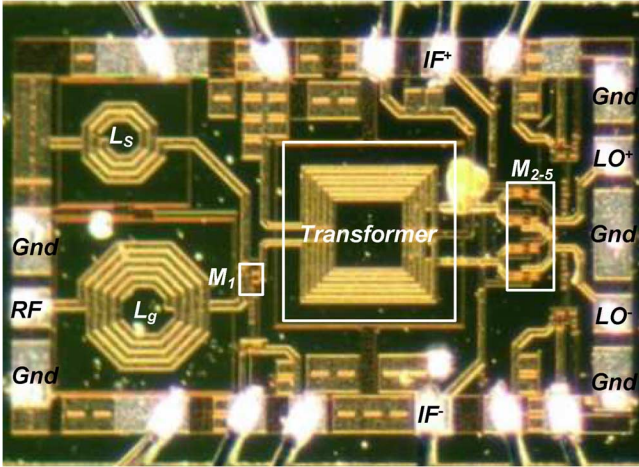


Fig. 13. Micrograph of the fabricated low-power receiver front-end circuit in 0.18- μm RF CMOS technology.

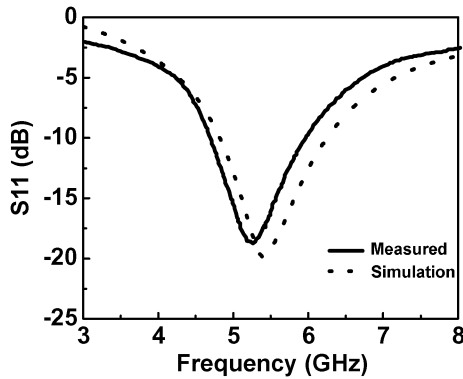


Fig. 14. Measured input return loss.

model of AD8011 from Analog Devices connected in unit gain. The differential input impedance of the OP amplifier is chosen as 16 k Ω to emulate a high IF loading impedance. A 50- Ω resistor is added in series at the OP amplifier output for impedance matching to 50- Ω measurement systems such that a 6-dB voltage gain shall be compensated in all the gain measurements.

The supply voltage V_{DD} is set as 0.6 V in the measurements. The total quiescent dc power consumption is 0.33 mW. The power becomes 0.53 mW as the LO signal of -9.5 dBm is injected under operation. Even if an additional mixer is taken into account for both I/Q channels, the total front-end power consumption is still around 1 mW. Fig. 14 plots the measured input return loss with a small frequency shift to 5.25 GHz. However, S_{11} at 5.5 GHz is still better than 16 dB. The bandwidth is around 1 GHz, of which the input return loss is better than 10 dB.

Fig. 15 illustrates the conversion gain versus LO power. The trend is similar to Fig. 6. The LO power is chosen as -9.5 dBm to obtain the highest gain of 17.4 dB, and this LO power is used in the measurements of IF bandwidth and linearity. Fig. 16 shows the measured IF bandwidth around 7 MHz, different from the simulated one around 300 MHz. This bandwidth

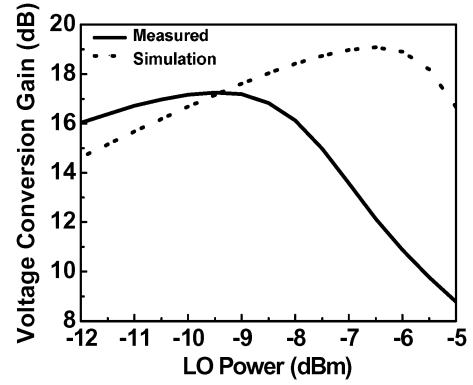


Fig. 15. Measured conversion gain versus LO power. The LO power of -9.5 dBm corresponds to the highest voltage conversion gain.

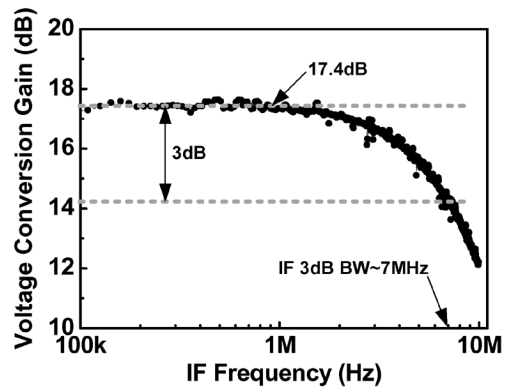


Fig. 16. Measured voltage conversion gain is about 17.4 dB with the IF bandwidth of 7 MHz, limited by the OP amplifier output buffer.

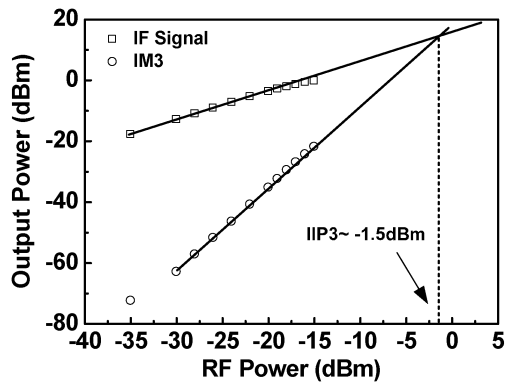


Fig. 17. Measured IIP_3 is around -1.5 dBm.

discrepancy arrives from the frequency response of the OP amplifier output buffer. It can be improved by using a wideband OP amplifier.

The IIP_3 measurement is conducted by a two-tone test. The measured IIP_3 is -1.5 dBm, as indicated in Fig. 17. The 1-dB compression point is also measured as -14 dBm. The measured NF is 7.8 dB at the IF frequency of 1 MHz. Table II summarizes the circuit performance and makes a comparison with previous works. The receiver front-end using the RCN shows excellent performance of the best FOM.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER FRONT-END CIRCUITS

Reference	RF Frequency (GHz)	Supply Voltage (V)	Conversion Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	P _{1dB} (dBm)	Power (mW)	FOM ⁽⁷⁾	Tech
[23]	5	1.0	25	12	-6.5	N/A	0.87	104.4	0.18μm
[24]	2.4	1.0	30.5	10.1 (10 MHz IF)	N/A	-31	0.5	96.7 ⁽⁴⁾	0.18μm
[25]	2.4	1.8	30	7.3 (1 MHz IF)	-8	-18	1.8	106.8	0.18μm
[26] ⁽²⁾	5.6	0.5	17.1	8.6(20 MHz IF)	-17.9	N/A	19.4 ⁽²⁾	78.7 ⁽⁵⁾	0.18μm
[27] ⁽³⁾	2.5	1.2	24	7 (10 MHz IF)	-21.5	-30.5	0.73	91.8	0.18μm
[28] ⁽¹⁾⁽²⁾	2.4	1.8	21.4	13.9 (2 MHz IF)	-10	-18	6.5	83.4 ⁽⁶⁾	0.18μm
[29]	2.3	1.8	24.5	13.5 (10 MHz IF)	-19	N/A	2.52	81.8	0.18μm
This Work	5.5	0.6	17.4	7.8 (1 MHz IF)	-1.5	-14	0.33	111.1	0.18μm

(1) Using single balanced mixer. (2) Power consumption contains I and Q mixers. (3) Including electrostatic discharge (ESD) protection in the input. (4) IIP3 of -21 dBm estimated from P_{1 dB}. (5) Half total power consumption of 9.7 mW is used for fair comparison. (6) Since it contains I and Q mixers using single-balanced topology, power consumption of 6.5 mW is still used in the FOM calculation. (7) FOM is defined as follows: FOM = 10log[(Gain × IIP3 × f)/(P_{DC} × (NF - 1))], where f, P_{DC} are calculated in Hz and mW, respectively.

IV. CONCLUSION

The resonator coupling technique for the MCG has been successfully employed to design a low-power and low-voltage 5.5-GHz receiver front-end fabricated in 0.18-μm CMOS technology. The RCN achieves the MCG condition when the resonators are critically coupled to the LNA. The most important one is that the RCN can achieve the same MCG level as an ideal transformer does, but without the constraint of unity coupling coefficient *k* and infinite inductance. This MCG in the RCN is only related to the ratio of the output resistance of the LNA and the input resistance of the mixer. Therefore, the RCN can utilize small *n* and small *k* to achieve the MCG so the chip area can be small to lower the cost. By using this resonator coupling technique, the receiver front-end only consumes 0.33 mW from a supply voltage of 0.6 V. The conversion gain, IIP3, and NF at IF frequency of 1 MHz are 17.4 dB, -1.5 dBm, and 7.8 dB, respectively. The proposed ultra-low power receiver front-end is very suitable for the applications of a wireless sensor network.

ACKNOWLEDGMENT

The authors would like to acknowledge the Chip Implementation Center (CIC), Hsinchu, Taiwan, for circuit fabrication support, the ANSYS, Taipei, Taiwan, for design support, and T.-N. Yu, Sunplus Technology Corporation, Hsinchu, Taiwan, for chip measurement.

REFERENCES

[1] B. W. Cook, A. D. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "An ultra-low power 2.4 GHz RF transceiver for wireless sensor networks in 0.13 μm CMOS with 400 mV supply and an integrated passive RX front-end," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2006, pp. 1460-1469.

[2] A. Molnar, B. Lu, S. Lanzisera, B. W. Cook, and K. S. J. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2004, pp. 401-404.

[3] J.-Y. Yu, C.-C. Chung, W.-C. Liao, and C.-Y. Lee, "A sub-mW multi-tone CDMA baseband transceiver chipset for wireless body area network applications," in *Proc. IEEE Int. Solid-State Circuit Conf. Tech. Dig.*, 2007, pp. 364-609.

[4] J. A. M. Jarvinen, J. Kaukovouri, J. Rynanen, J. Jussila, K. Kivekas, M. Honkanen, and K. A. I. Halonen, "2.4-GHz receiver for sensor applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1426-1433, Jul. 2005.

[5] E. Ragonese, A. Italia, M. F. Seminara, and G. Palmisano, "A transformer-based receiver front-end for 5-GHz WLANs," in *Proc. IEEE RFIC Symp.*, 2006, pp. 416-420.

[6] H.-C. Chen, T. Wang, S.-S. Lu, and G.-W. Huang, "A monolithic 5.9-GHz CMOS I/Q direct-down converter utilizing a quadrature coupler and transformer-coupled subharmonic mixers," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 4, pp. 197-199, Apr. 2006.

[7] G. Theodoratos, Y. Papananos, and G. Vitzilaios, "A low-voltage 5-GHz downconversion mixer employing a second harmonic injection linearization technique," *IEEE Tran. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 964-968, Nov. 2007.

[8] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A millimeter-wave (23-32 GHz) wideband BiCMOS low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 289-299, Feb. 2010.

[9] A. Bevilacqua et al., "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Tran. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293-297, Apr. 2007.

[10] B. Catli and M. Mostafa Hella, "A 1.94 to 2.55 GHz, 3.6 to 4.77 GHz tunable CMOS VCO based on double-tuned, double-driven coupled resonators," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2463-2477, Sep. 2009.

[11] C. Hermann, M. Tiebout, and H. Klar, "A 0.6-V 1.6-mW transformer-based 2.5-GHz downconversion mixer with +5.4-dB gain and -2.8-dBm IIP3 in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 488-495, Feb. 2005.

[12] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 1996.

[13] H. Ma, S. J. Fang, F. Lin, and H. Nakamura, "Novel active differential phase splitters in RFIC for wireless applications," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2597-2603, Dec. 1998.

[14] M. A. Do, W. M. Lim, J. G. Ma, and K. S. Yeo, "Design of a phase splitter for 3rd ISM band," in *IEEE Electron Devices Solid-State Circuits Conf.*, 2003, pp. 237-240.

[15] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[16] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[17] A. A. Abidi, G. J. Pottie, and W. J. Kaiser, "Power-conscious design of wireless circuits and systems," *Proc. IEEE*, vol. 88, no. 10, pp. 1528-1545, Oct. 2000.

[18] T. K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433-1442, May 2004.

[19] B. G. Perumana, S. Chakraborty, C.-H. Lee, and J. Laskar, "A fully monolithic 260-μW, 1-GHz subthreshold low noise amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 6, pp. 428-430, Jun. 2005.

[20] F. Silveira, D. Flandre, and P. G. A. Jespers, "A *g_m/I_D* based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1314-1319, Sep. 1996.

[21] A. Shamelil and P. Heydari, "A novel power optimization technique for ultra-low power RFICs," in *Proc. Int. Low-Power Electron. Design Symp.*, 2006, pp. 274-279.

[22] R. Brederlow et al., "A mixed-signal design roadmap," *IEEE Design Test Comput.*, vol. 18, no. 6, pp. 34-46, Nov.-Dec. 2001.

- [23] T. Hsu, Y.-L. Liu, S.-H. Yen, and C.-N. Kuo, "Sub-mW 5-GHz receiver front-end circuit design," in *Proc. Silicon Monolithic Integr. Circuits RF Syst. Topical Meeting*, 2007, pp. 205–208.
- [24] T. Song, H.-S. Oh, E. Yoon, and S. Hong, "A low-power 2.4 GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1012–1022, May 2007.
- [25] T.-K. Nguyen, V. Krizhanovskii, J. Lee, S.-K. Han, S.-G. Lee, N.-S. Kim, and C.-S. Pyo, "A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18- μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4062–4071, Dec. 2006.
- [26] H.-C. Chen, T. Wang, H.-W. Chiu, T.-H. Kao, and S.-S. Lu, "0.5-V 5.6-GHz CMOS receiver subsystem," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 2, pp. 329–335, Feb. 2009.
- [27] L. Moreno, D. Gomez, J. L. Gonzalez, D. Mateo, X. Aragones, R. Berenguer, and H. Solar, "A low-power RF front-end for 2.5 GHz receivers," in *Proc. IEEE Int. Circuits Syst. Symp.*, 2008, pp. 976–979.
- [28] F. Beffa, R. Vogt, W. Bachtold, E. Zellweger, and U. Lott, "A 6.5-mW receiver front-end for Bluetooth in 0.18 μm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2002, pp. 501–504.
- [29] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk, "An energy-aware CMOS receiver front-end for low-power 2.4 GHz applications," *IEEE Tran. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2675–2684, Oct. 2010.



Chun-Hsing Li (S'10) received the B.S. degree in electrophysics and M.S. degree in electronics engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 2005 and 2007, respectively, and is currently working toward the Ph.D. degree at NCTU.

After one year of military service as a Second Lieutenant with the Marine Corps, he was a Research Assistant with the RF System Integration Laboratory, NCTU, until June 2009. In Fall 2009, he joined the Department of Electrical Engineering, University of

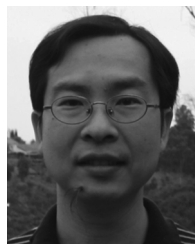
California at Los Angeles (UCLA). In Winter 2010, he was with the Department of Electrical and Computer Engineering, University of California at Santa Barbara. Since April 2010, he has been with NCTU. His current research is focused on the RF and terahertz circuit design.

Mr. Li was a corecipient of the Best Paper Award of the 13th IEEE International Conference on Electronics, Circuits, and Systems, Nice, France, 2006.



Yen-Lin Liu received the B.S. degree (with honors) in electrophysics and M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2005 and 2007, respectively.

She is currently with the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.



Chien-Nan Kuo (S'93–M'97) received the B.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1988, the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1990, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles (UCLA), in 1997.

In 1997, he joined ADC Telecommunications, San Diego, CA, as a Member of Technical Staff with the Mobile System Division, where he was involved in wireless base-station design. In 1999, he joined Broadband Innovations Inc. In 2001, he joined the Microelectronics Division, IBM. He is currently an Associated Professor with the Department of Electronics Engineering, National Chiao Tung University. His research interests include reconfigurable RF circuit and system integration design, low-power design for the application of wireless sensor networks, and development of circuit-package co-design in the system-in-package (SiP) technique.

Dr. Kuo has served as a Program Committee member of the IEEE Asian Solid-State Circuits Conference since 2005 and IEEE Silicon Monolithic Integrated Circuits in RF Systems since 2007. He was a recipient of the IEEE Graduate Fellowship Award in 1996. He was a corecipient of the 2006 Best Paper Award presented at the 13th IEEE International Conference on Electronics, Circuits, and Systems.