A Near-Threshold 480 MHz 78 μW All-Digital PLL With a Bootstrapped DCO

Yingchieh Ho, *Member, IEEE*, Yu-Sheng Yang, ChiaChi Chang, and Chauchin Su, *Member, IEEE*

***Abstract*—This paper presents a near-threshold low-power all-digital PLL (ADPLL). It includes a 9-bit bootstrapped DCO (BDCO) to reduce supply voltage and power consumption, a weighted thermometer-controlled resistor network (WTRN) to achieve high linearity, and a 4-bit sigma-delta modulator to improve the resolution through dithering. The ADPLL is fabricated in a 90 nm SPRVT low-K CMOS process with a core area of 0.057 mm². The measured results demonstrate that the bootstrapped ring oscillator (BTRO) oscillates at 602 MHz under a supply of 0.5 V and consumes 49.1 μW. The ADPLL operates at 480 MHz (48 MHz) with a power consumption of 78 μW (2.4 μW) under a supply voltage of 0.5 V (0.25 V).**

***Index Terms*—All-digital phase-locked loop (ADPLL), bootstrapped circuit, energy-efficient design, low-power, low-voltage, near-threshold circuit.**

I. Introduction

ULTRA-LOW power design is essential to prolonging the battery lives of sustainable electronic devices. According to $P = fCV^2$, scaling down the supply voltage is the most effective way to reduce power consumption. A forecast in the International Technology Roadmap for Semiconductors (ITRS) reveals that the supply voltage will be scaled down to 0.5 V for the next generation of low-power applications [1]. Recently, some 0.5 V biomedical applications have been reported [2], [3]. Some important analog building blocks have been developed with a 0.5 V supply to operate at 1–10 MHz [4], [5]. [6] demonstrated a processor with a wide range of voltages 0.28–1.2 V that exhibited an entire order of improvement of energy efficiency at near-threshold supply.

Phase-locked loops (PLLs) are key building blocks in integrated circuits. Numerous clock circuits that are scaled to 0.5 V and based on analog approaches that have been reported [7], [8]. Actually, low-voltage PLLs are very effective and energy-efficient for low power applications. For example, USB 2.0 is a popular data link interface and is still widely used in applications that involve frequencies of several tens to hundreds MHz [9]. USB 2.0 has high-speed, full-speed, and low-power modes, which operate at 480 MHz, 12 MHz and 1.5 MHz, respectively. Clock circuits with frequencies of 48 MHz are also used in USB microcontrollers in the full-speed mode [10], [11]. Low-voltage PLLs can be utilized in more applications, such as Intra-Body Communication (IBC) systems [12] and Wireless Sensor Networks (WSN) [13], which target several kHz to tens MHz.

All-digital PLLs (ADPLLs) are popular alternatives to analog PLLs owing to their portability and scalability. They exhibit no DC power dissipation. The oscillator is the most power-hungry building block of a PLL, even when scaled to the near-threshold region. Although LC oscillators have superior phase noise, ring oscillators are commonly preferred for reasons of power consumption and occupied area. The digitally controlled oscillator (DCO) that was presented by Chen [14] is composed of a 12-bit DAC and a current-controlled oscillator that uses a 260 μA bias current. However, a high-resolution DAC requires higher power and has a higher area overhead. To enhance driving capability and the linear control range, Cheng proposed a bulk-driven, 0.5 V 8-phase voltage-controlled oscillator (VCO) [8]. It successfully modulates the threshold voltage V_{th} by slightly increasing the leakage current. [15] took an all-digital approach and utilized a large number of digital delay cells and paths, which consumed much power owing to its parasitic loads. Several DCOs are composed of a supply-regulated ring oscillator and a digitally-controlled resistor network (DRN) [16], [17]. The major issues in the design of such DRNs are linearity and complexity.

This paper presents a near-threshold supply ADPLL with a bootstrapped digitally-controlled ring oscillator (BDCO) to operate at 0.25–0.5 V. The BDCO consists of a bootstrapped ring oscillator (BTRO) and a weighted thermometer-controlled resistor network (WTRN). The proposed BDCO generates a boosted gate voltage swing to improve driving capability. It also keeps the transistors functioning in linear region to have high linearity even under a near-threshold supply.

The rest of this paper is organized as follows. Section II introduces the proposed ADPLL. Section III presents analyses of performance. Section IV describes the test chip and provides the experimental results. Finally, Section V compares the results with some reported works and draws conclusions.

II. Architecture of Proposed All-Digital PLL

The proposed ADPLL, shown in Fig. 1, consists of a phase frequency detector (PFD) to detect the phase error, a phase selector (PS) to reroute the signal path, a time-to-digital converter

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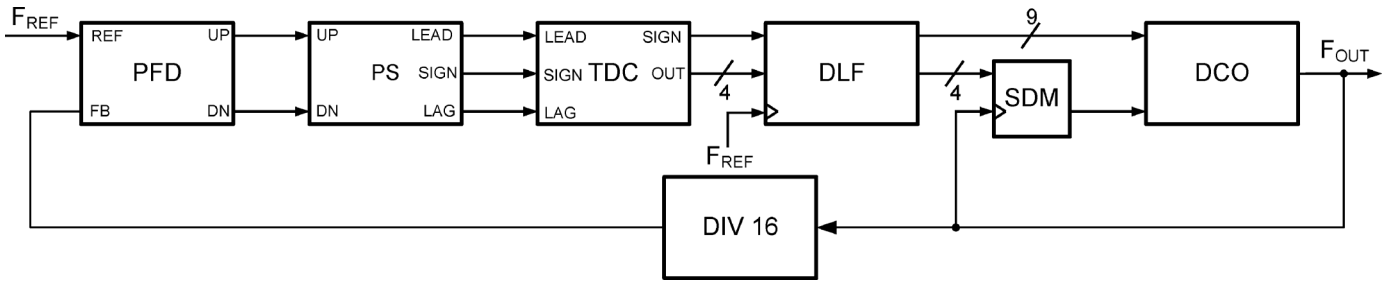


Fig. 1. Block diagram of the proposed ADPLL.

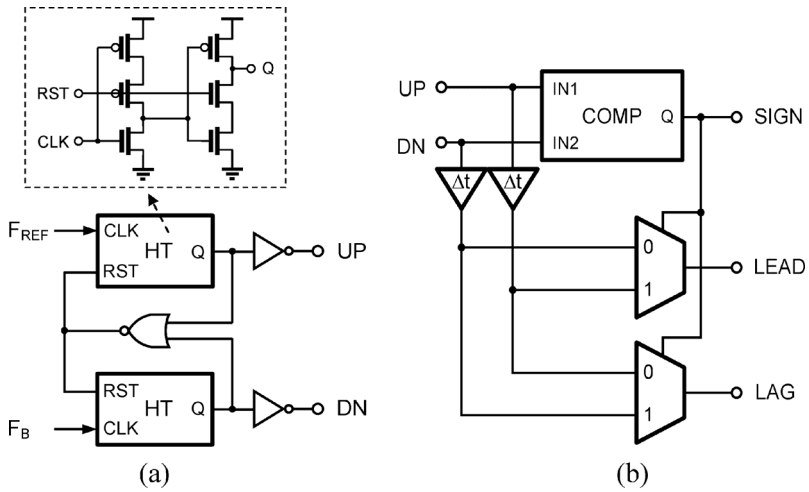


Fig. 2. Circuit schematics of (a) PFD and (b) PS.

(TDC) to convert the phase error into digital code, a digital loop filter (DLF) to filter out the high frequency noise, a DCO to generate the required output frequency, and a divider (DIV) to divide and feed back the output frequency. A 4-bit sigma-delta modulator (SDM) is used for dithering to improve the resolution of the DCO. The division ratio should be determined according to the speed of the sub-circuits. In the design herein, the output frequency is divided by 16. In our earlier work [18], the proposed BTRO exploited a gate-boosting technique for operation at low voltage. To extend this approach to an ADPLL, a BTRO control circuit and other circuit designs should be used to deal with the issues that arise in near-threshold operation. When the ADPLL operates at near-threshold supply, very close to the turn-on condition, the gate delay is degraded by approximately an order of magnitude. Therefore, circuit topologies, such as static CMOS logics, are utilized to reduce power consumption. Besides, no more than two stacked devices are selected to operate with such low-voltage headroom.

In the design procedure of Kratyuk [19], the mathematical representation of the proposed ADPLL is obtained by transforming the S-domain system model of a charge-pump PLL (CPPLL). According to the parameters in the conventional CPPLL model, z-domain parameters can be estimated by bilinear transformation.

A. PFDC and DLF

PFD, PS and TDC can together be regarded as comprising a phase/frequency-to-digital converter (PFDC). PFD produces UP and DN signals that indicate the phase error. Fig. 2(a) shows the circuit diagram. PFD is designed as a dynamic circuit to operate at high frequency. To provide the correct phase arrangement for the TDC, two signals are rerouted by PS, as illustrated in Fig. 2(b) [17]. TDC is based on a Vernier delay line, as shown in Fig. 3 [20]. It requires the proper phase order for the time-to-digital conversion. As LEAD and LAG signals propagate in their independent delay chain, the timing difference between the two signals decreases by ΔT in each stage, where ΔT is defined as the resolution of the Vernier TDC. A Vernier-based delay line generates a timing ruler according to differences between gate delays. As a result, the TDC achieves high resolution even at low voltage supply. Based on the simulation results, the 4-bit TDC is designed with a resolution of 15 ps (156 ps) at the 0.5 V (0.25 V) TT corner. The phase comparators compare the phases of the delayed LEAD and LAG signals and produce a 16-bit thermometer code. Each comparator is composed of two cross-coupled latches, as shown in Fig. 3. Finally, a thermometer-to-binary (T2B) decoder converts the thermometer code to a 4-bit binary one. Fig. 4 shows the characteristics of the TDC in different corners at 0.5 V.

The DLF is a 2nd-order digital filter whose parameters are obtained by a bilinear transformation from those of its analog counterpart, as depicted in Fig. 5. It contains two signal paths—the proportional path (K_P) and the integral path (K_I). The transfer function is

$$H(s)_{ALF} = \frac{V(s)}{I(s)} = R + \frac{1}{sC}. \quad (1)$$

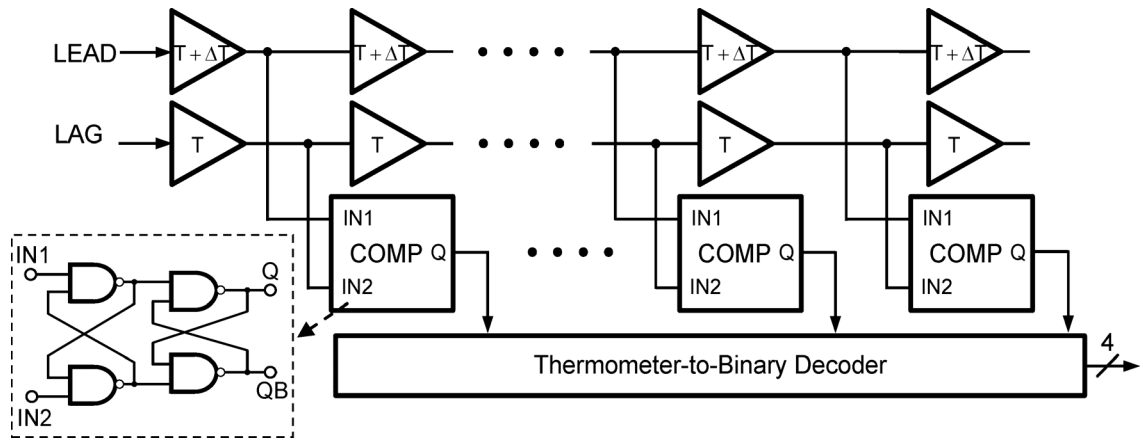


Fig. 3. Circuit schematic of the TDC.

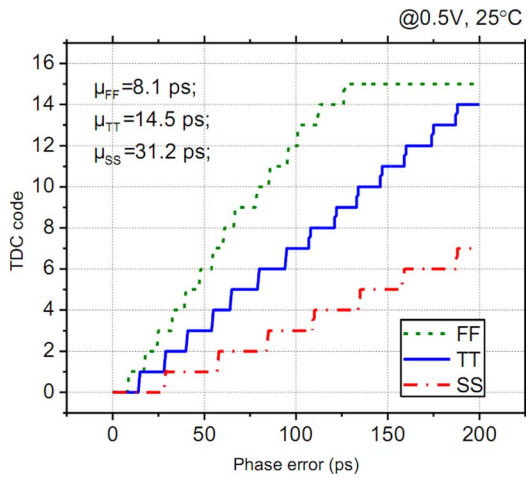


Fig. 4. Transfer curve of the TDC at different corners.

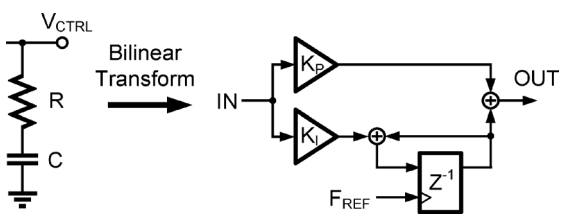


Fig. 5. Circuit schematic of DLF.

The Z-domain transfer function is

$$\mathrm{H_{DLF}(z)} = \mathrm{K_P} + \mathrm{K_I}\frac{1}{1-\mathrm{z}^{-1}} = \frac{(\mathrm{K_P}+\mathrm{K_I}) - \mathrm{K_P z}^{-1}}{1-\mathrm{z}^{-1}}. \quad (2)$$

B. BDCO

For near-threshold operation, the driving capability, linearity and variability are major concerns. In the proposed ADPLL, BDCO is used to address these issues and support high speed and energy efficiency. It is composed of a 5-stage BTRO with its supply voltage V_{C} controlled by a WTRN, as shown in Fig. 6. The details of its operations are introduced as follows.

1) BTRO: As in our previous work [18], a BTRO that can operate in the near-threshold region has been proposed. The bootstrapped delay cell ideally generates an output swing of $-V_{\mathrm{C}}$ to $2V_{\mathrm{C}}$. When $\mathrm{V_{in}} = 2V_{\mathrm{C}}$, $\mathrm{N_{OP}} = 0$ and $\mathrm{N_{BP}}$ is precharged to V_{C} by $\mathrm{M_{P1}}$. After $\mathrm{V_{in}}$ transits to $-V_{\mathrm{C}}$, $\mathrm{N_{OP}}$ rises to V_{C} and boosts $\mathrm{N_{BP}}$ to $2V_{\mathrm{C}}$. The boosted $2V_{\mathrm{C}}$ at $\mathrm{N_{BP}}$ is transferred to V_{out} via $\mathrm{M_{P2}}$. An output voltage of $2V_{\mathrm{C}}$ ($-V_{\mathrm{C}}$) pushes the NMOS (PMOS) transistors in the next bootstrapped delay cell into the super-threshold region and increases their driving capability. It also exponentially suppresses the PMOS (NMOS) leakage current. Therefore, the operating frequency can be increased without causing the leakage problem that arises when large-width transistors are used. Furthermore, since transistors are operated in the super-threshold region, they have better linearity and immunity against process variation than is achieved in near-threshold or sub-threshold operation.

2) WTRN: As mentioned above, the BTRO exhibits high linearity with respect to the supply voltage, as will be discussed later. Therefore a WTRN is designed to regulate its V_{DD} using a 9-bit digital controlled PMOS array, as illustrated in Fig. 7. The resistor network consists of 9-bit PMOS transistor array, a binary-to-thermometer (B2T) code converter and an SDM. The total of 13 control bits comprise two for coarse tuning, three for medium tuning, four for fine tuning, and four for dithering by an SDM to further improve the resolution.

Resistor networks are used to form a voltage divider with DCOs [16], [17]. Therefore, the equivalent output V_{C} can be regarded as the supply voltage of the DCOs. However, full thermometer control in [16] occupied a large area and complicated wiring. The hybrid architecture of binary and thermometer control in the work of Lin [17] was not sufficiently linear. Here, a WTRN design is used. The PMOS switches are designed with weighted sizes as determined by their equivalent resistance behavior to improve linearity. Fig. 8 plots the DCO output frequency as a function of the coarse and medium control codes at 0.5 V. As compared to the binary-weighted control, the proposed WTRN has better linearity with a gain of 563 kHz/code in TT corner.

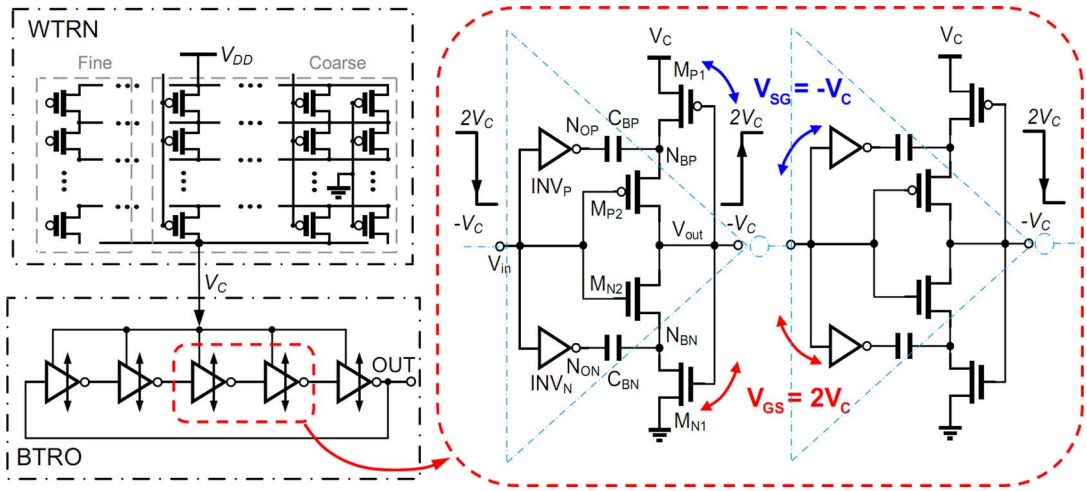


Fig. 6. Circuit schematic of the BDCO and BTRO.

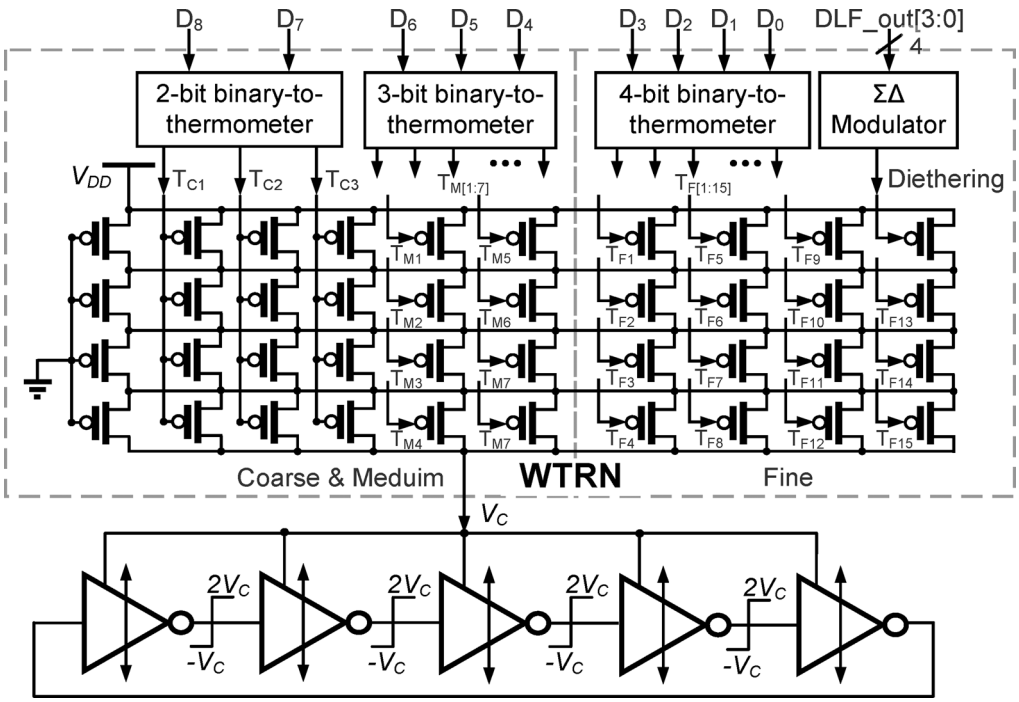


Fig. 7. Detail circuit schematic of the BDCO with the WTRN.

C. SDM

To improve the resolution of the BDCO, a 4-bit 1st-order SDM is used to dither the least-significant bit (LSB). Fig. 9 shows its block diagram. It consists of a 4-bit adder and a register. With SDM dithering, the BDCO exhibits equivalently a 16-fold improvement in resolution. Table I lists the parameters of the ADPLL at 0.25 V and 0.5 V.

III. Detailed Evaluation on BTRO

A. Power Analysis of BTRO

As mentioned above, an oscillator is consumed most of the power in a PLL. Unlike an analog VCO, in which the constant biasing current is the major consumer of power, DCO consumes no DC current. However, dynamic power is the major concern, especially for a BTRO, owing to its large output swing from $-\beta V_{\rm C}$ to $\beta 2V_{\rm C}$, where β is the boosting efficient factor [18]. As shown in Fig. 10, the total capacitance is sum of the output capacitance $C_{\rm OP}$ at node V_{out} and the input capacitance C_{IP} at node $V_{\rm in}$. C_{INV} denotes the total capacitance at the output nodes of the $\rm INV_P$ and $\rm INV_N$, where the output swings are from GND to $V_{\rm C}$. The total dynamic power consumption of a 5-stage BTRO is

$$P_{BTRO} \approx 5f\left[\left(C_{IP}+C_{\rm OP}\right)\left(\beta 2V_{\rm C}+\beta V_{\rm C}\right)^2+C_{INV}V_{\rm C}^2\right] \approx f\left[45\beta^2\left(C_{IP}+C_{\rm OP}\right)+5C_{INV}\right]V_{\rm C}^2. \quad (3)$$

Although a bootstrapped delay cell has several leakage current paths, leakage current can be reduced by a negative overdrive voltage. As shown in Fig. 10, when $V_{\rm in} = \beta 2V_{\rm C}$, one of

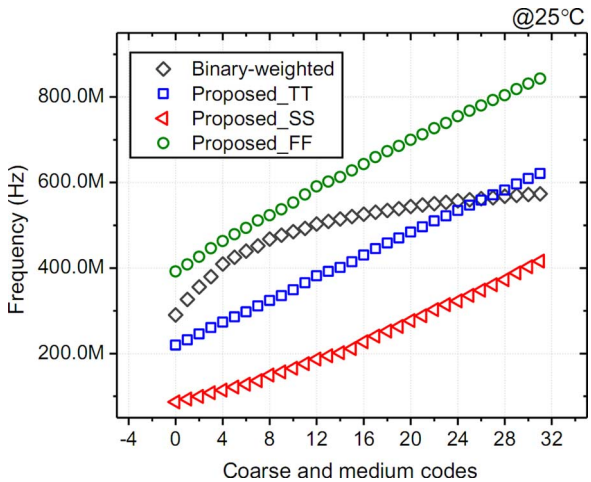


Fig. 8. DCO output frequency versus coarse and medium codes in corners.

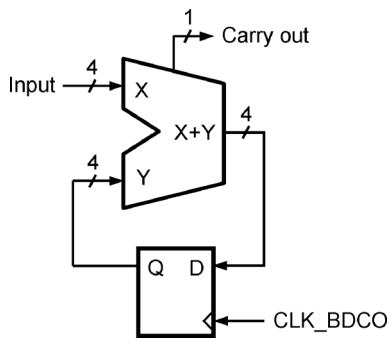


Fig. 9. Block diagram of the SDM.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED ADPLL

Parameter name	Value (0.25V)	Value (0.5V)
Reference frequency	3MHz	30MHz
Loop bandwidth	125kHz	1.25MHz
Phase margin	65.7°	60°
K_{DCO} (simulation)	213 kHz/code	563kHz/code
TDC resolution (TT corner)	156ps	15ps
Output frequency	48MHz	480MHz
Divider number	16	16
DLF coefficients	$K_P = 2^{-1}; K_I = 2^{-4}$.	$K_P = 2^{-1}; K_I = 2^{-4}$.

the leakage paths is from pre-charge node N_{BP} to the output through M_{P2}, and another is from the ground to the boosted node through M_{N1}. Since $\beta 2V_C$ is applied to the gate on M_{P2} and $-\beta V_C$ to the gate on M_{N1}, all of these transistors are biased with negative V_{GS}. Similarly, V_{in} functions the other two paths on the INV_P and INV_N. As a result, all leakage currents are substantially reduced to an extent that they can be neglected, making the BTRO more energy efficient.

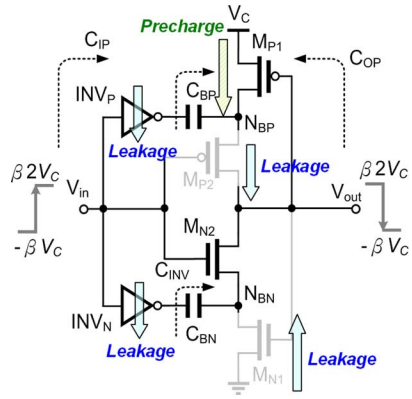


Fig. 10. Power analysis example of the BTRO.

B. Linearity Analysis of BTRO

An inverter-based ring oscillator can serve as a supply-regulated VCO. However, its poor linearity in the near-threshold region affects the tracking and locking behavior as well as the jitter performance. The period T of an N-stage inverter-based ring oscillator is

$$T = 2N \times T_D, \tag{4}$$

where T_D is the delay time of a single stage. Assume that the rising and falling times are not exactly the same; T_D can then be given by

$$T_D = 0.5\left(\tau_{PHL} + \tau_{PLH}\right), \tag{5}$$

where τ_{PHL} and τ_{PLH} are the propagation delays The linearity can be analyzed with reference to the propagation delays. Assume that C_L is the effective load capacitance at output node of a single stage,

$$\tau_{PHL} = \int_{0.5V_{DD}}^{V_{DD}} \frac{C_L}{I_{DN}} dV_{out}. \tag{6}$$

In the single stage of an inverter-based ring oscillator, C_L is discharged by the NMOS with $V_{GS} = V_{DD}$. τ_{PHL_C} is the expression of the delay time of an inverter-based delay cell. As determined by the discharging characteristics in the near-threshold region, τ_{PHL_C} has one of two forms, depending on whether V_{DD} exceeds the threshold voltage V_{th} [21]. The switching operation is either in the saturation region or in sub-threshold region. Thus, (6) can be rewritten as

$$\tau_{PHL\_C} = \begin{cases} \tau_{PHL\_Sat}, & V_{DD} \geq V_{th} \\ \tau_{PHL\_Sub}, & V_{DD} < V_{th}. \end{cases} \tag{7}$$

From the I-V expressions in saturation region and in sub-threshold region [22], we can derive τ_{PHL_C} from (6) and (7) as (8) and (9):

$$\tau_{PHL\_Sat} = 2C_L \left[\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{th})\right]^{-1}, \tag{8}$$

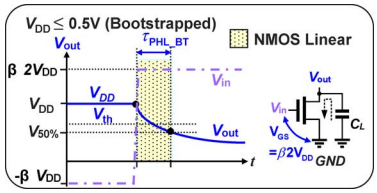


Fig. 11. Delay time calculation for the BTRO.

$$\tau_{PHL\_Sub} = C_L \left[\mu_n C_{\text{dep}} \frac{W}{L} V_T^2 \cdot \exp\left(\frac{V_{\text{DD}} - V_{th}}{nV_T}\right) \left(V_{th} - \frac{V_{\text{DD}}}{2}\right) \right]^{-1}, \quad (9)$$

where μ_n is the effective mobility; C_{ox} is the gate oxide capacitance per unit area; W and L are the width and length of the device; and C_{dep} is the depletion capacitance; V_T is the thermal voltage; and n is the factor of sub-threshold slope. In (8), channel-length modulation is neglected. According to (9), τ_{PHL_Sub} is not proportional to the reciprocal of V_{DD}. As a result, the frequency of the inverter-based ring oscillator is not linear as regulating supply voltage.

Unlike an inverter-based ring oscillator, the BTRO behaves highly linearly throughout the period of operation period. It features boosted swings from $-\beta V_{\text{DD}}$ to $\beta 2V_{\text{DD}}$, which push the operation of the INV_P and INV_N into the triode region. Fig. 11 displays the falling edge. Equation (10) plots the driving current.

$$I_{D,BT} = \mu_n C_{ox} \frac{W}{L} \left[(\beta 2V_{\text{DD}} - V_{th}) V_{out} - \frac{1}{2} V_{out}^2 \right]. \quad (10)$$

We can derive τ_{PHL_BT} from (6) and (10) as

$$\tau_{PHL\_BT} = C_L \cdot \ln \left| \frac{(8\beta - 1)V_{\text{DD}} - V_{th}}{(4\beta - 1)V_{\text{DD}} - V_{th}} \right| \cdot \left[\mu_n C_{ox} \frac{W}{L} (2\beta V_{\text{DD}} - V_{th}) \right]^{-1}. \quad (11)$$

Assume that the supply voltage is set between 0.25–0.5 V and β is 90%, then (11) can be approximated by

$$\tau_{PHL\_BT} \approx 3C_L \cdot \left[\mu_n C_{ox} \frac{W}{L} (2\beta V_{\text{DD}} - V_{th}) \right]^{-1}. \quad (12)$$

The period of the BTRO can be determined from τ_{PHL_BT} and τ_{PLH_BT}. As a result, the frequency of the BTRO is highly proportional to $(2\beta V_{\text{DD}} - V_{th})$, and so the BTRO is suitable for use as a supply-regulated VCO in the near-threshold region.

Fig. 12 plots results of a simulation of a 5-stage supply-regulated VCO at 25°C in different process corners. The BTRO has higher linearity than an inverter-based VCO in the near-threshold region, and is less affected by the process variation.

IV. Experimental Results and Comparisons

A. Chip Implementation

The proposed ADPLL has been fabricated using 90 nm 1P9M SPRVT CMOS process. According to technical documents from the foundry, the nominal V_{th} values of NMOS and PMOS devices are 240 mV and 180 mV, respectively. The test chip includes two test circuits, the proposed BTRO and the ADPLL. Fig. 13 shows the block diagram of the test circuits. Multi-stage bootstrapped level shifters with an intermediate supply voltage of $V_{\text{M\_I/O}}$ are used to drive open drain devices. Fig. 14 shows the chip micrograph. The overall active areas of the BTRO and the ADPLL are 31.5 μm × 61.5 μm and 326 μm × 175 μm, respectively. The test chip is mounted on an FR4 test board with SMA connectors, as shown in Fig. 15. An Agilent 81130A pulse generator provides the reference clock; an Agilent 54382D and an MSO9404A are used to measure output waveforms and jitter. A Keithley 2400 power meter provides DC power and measures power consumption. Phase noise was measured using an Agilent E4440A Spectrum Analyzer.

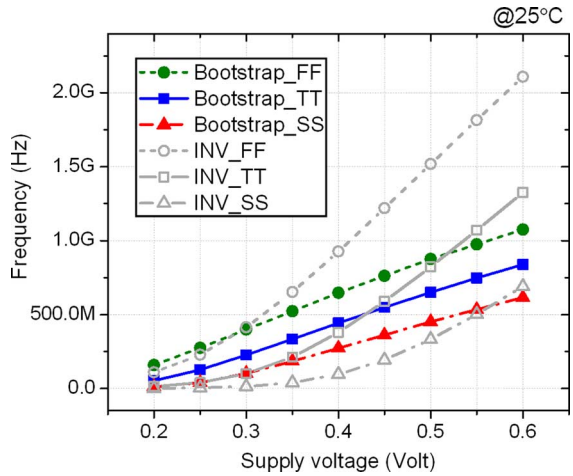


Fig. 12. Transfer curves of two supply-regulated VCOs.

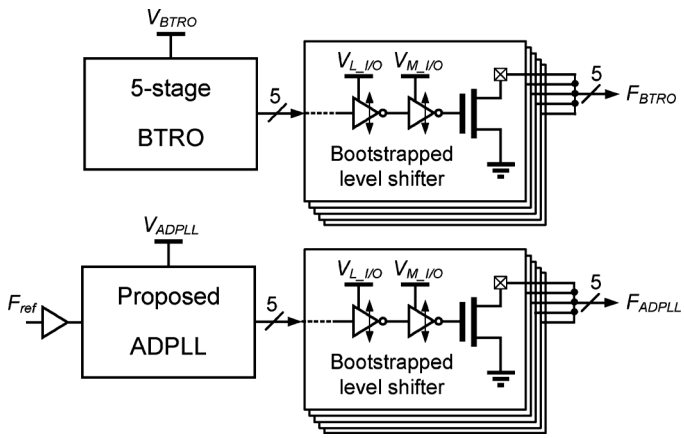


Fig. 13. Block diagram of the test circuits.

B. Measured Results

Figs. 16(a) and (b) show the measured output waveforms of the BTRO at 0.2 and 0.6 V. Fig. 17 plots in detail frequency/power of the BTRO versus voltage between 0.2 and 0.6 V. These measured results match the simulated ones in the TT

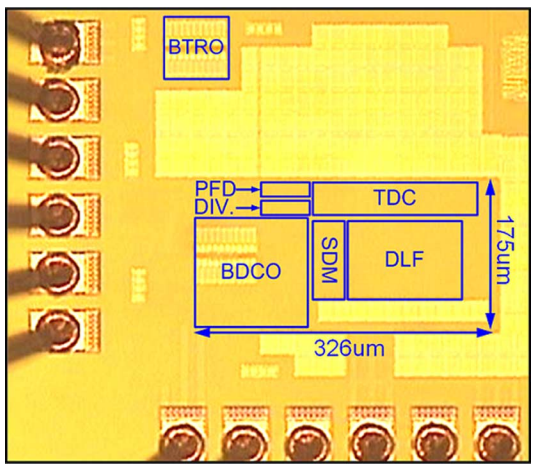


Fig. 14. Micrograph of the test chip.

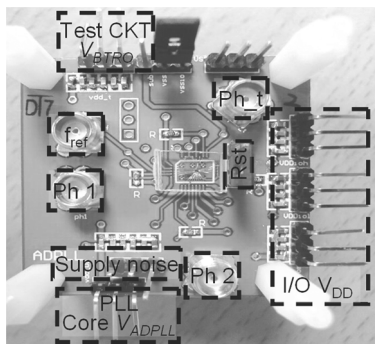
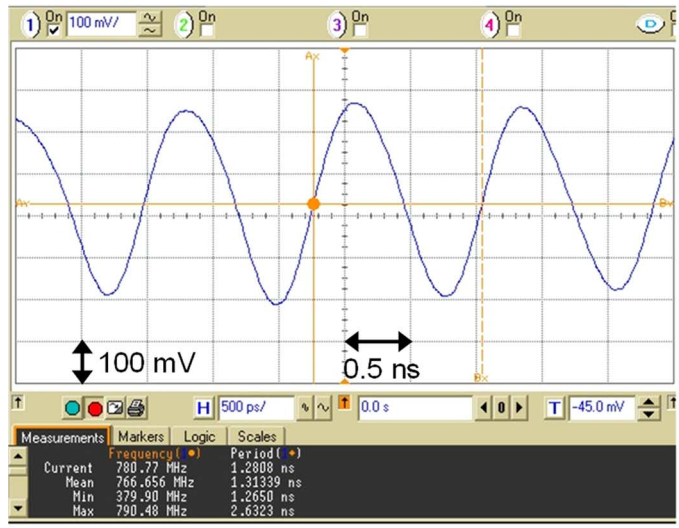
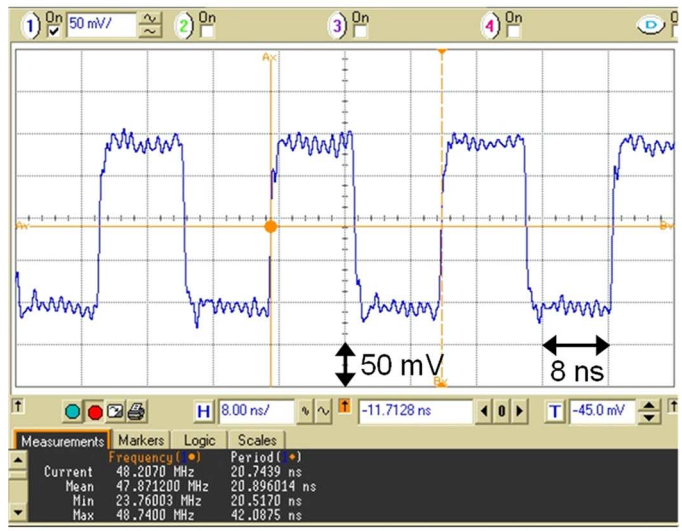


Fig. 15. Photo of the test board.



(a)



(b)

Fig. 16. Measured output waveforms of the BTRO at (a) 0.6 V V_{DD} ; (b) 0.2 V V_{DD}.

corner. The BTRO exhibits a relatively linear oscillation frequency versus supply voltage near the threshold and in the subthreshold region.

The range of measured output frequencies of the proposed ADPLL is from 176 to 480 MHz at a supply voltage of 0.5 V and 36.8 to 48 MHz at a supply voltage of 0.25 V. Fig. 18 plots locked clock waveform at 480 MHz. The jitter histogram shows that the output RMS jitter and peak-to-peak jitter are 7.93 ps and 61.1 ps, respectively. Figs. 19 and 20 plot the measured output spectrum and phase noise at 0.5 V and 0.25 V, respectively. With a reference of 30 MHz (3 MHz), the measured spur at 480 MHz (48 MHz) under a 0.5 V (0.25 V) V_{DD} is 42.5 dB (39.8 dB) below the carrier. The phase noise is -94.0 dBc/Hz (-89.8 dBc/Hz) at a 1 MHz offset and -85.3 dBc/Hz (-78.2 dBc/Hz) at a 10 kHz offset when the output frequency is 480 MHz (48 MHz). The noise peaks in Figs. 19 and 20 are associated with DCO noise. This ADPLL is designed for general low-power applications and the loop bandwidth in the proposed design cannot be adjusted to suppress high-frequency DCO noise. Accordingly, a power-performance trade-off is made. Finally, Table II summarizes the major characteristics of the test chip.

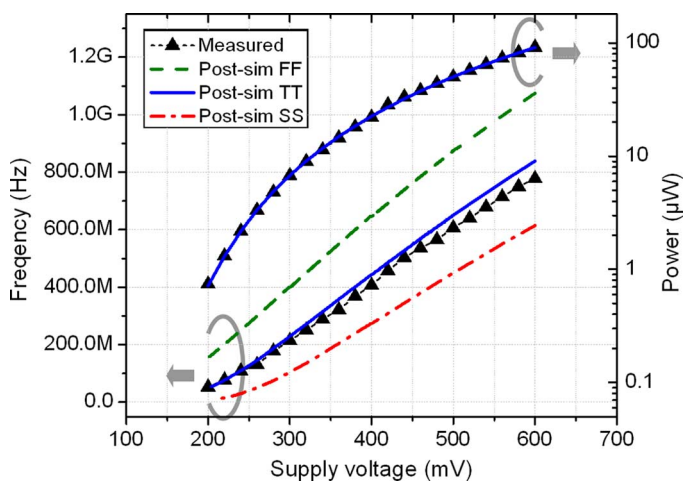


Fig. 17. Comparisons with measured and simulation results.

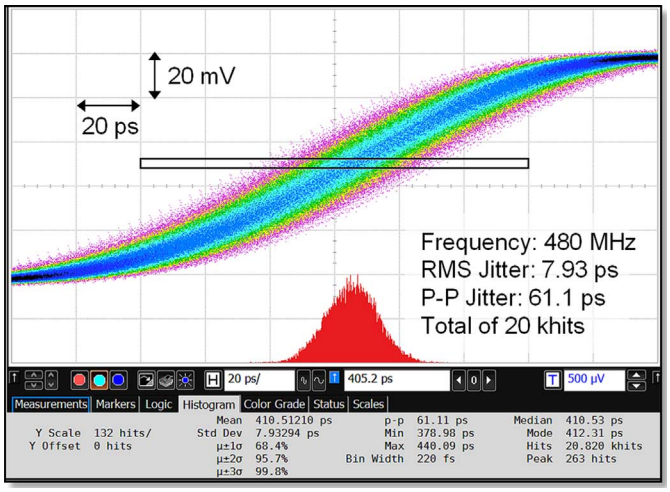


Fig. 18. Measured jitter histogram at 480 MHz.

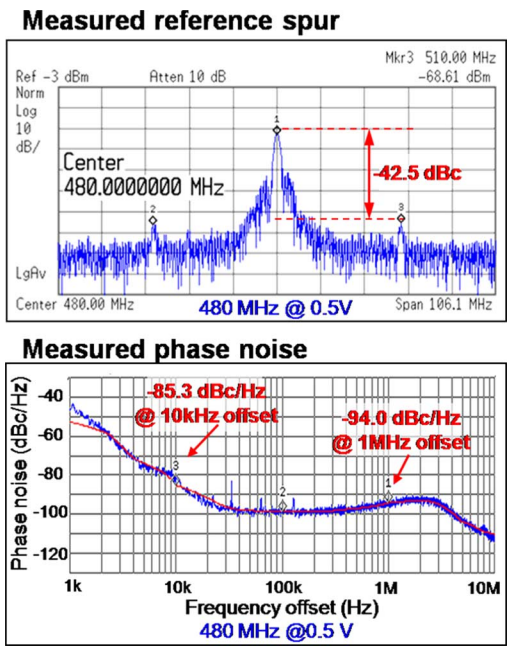


Fig. 19. Measured spectrum and phase noise at 0.5 V.

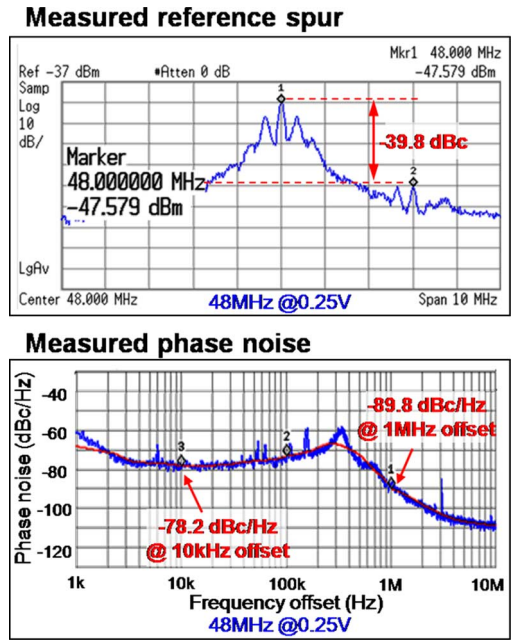


Fig. 20. Measured spectrum and phase noise at 0.25 V.

TABLE II
TEST CHIP SUMMARY

Process		90nm 1P9M SPRVT	
V_{th}		NMOS: 240mV; PMOS: 180mV	
Core Supply Voltage		0.25V	0.5V
Max output frequency		48MHz	480MHz
Power		2.95μW	78μW
Phase Noise @1MHz offset		-89.8dBc/Hz	-94.0dBc/Hz
Layout Area	BTRO	31.5μm x 61.5μm	
	ADPLL	326μm x 175μm	

C. Comparisons

Table III compares low-voltage VCOs and DCOs in terms of their performance. The BTRO can operate at a supply voltage of as low as 0.2 V. Additionally, the measured energy per cycle indicates that the BTRO is power-efficient. Table IV summarizes recent state-of-the-art PLLs using a near-threshold supply. Previous works [7], [26] have realized LC-VCO with very favorable low phase noise. However, the designs therein occupy a large die area using passive resonant elements and provide only two or four phases of output frequency. On the contrary, ring-VCO PLLs are area-efficient; have more phases of output frequency, but have inherently inferior phase noise. The proposed ADPLL has 10-phase output frequency and consumes 78 μW at 480 MHz under a V_{DD} of 0.5 V; 53.8% of the area that is occupied by the DCO. The proposed design is effective even at $V_{DD} = 0.25$ V with a lock range of 36.8 to 48 MHz. The *figure of merit* (FoM) in pJ/cycle is almost an order of magnitude better than that of the DCO in [24].

V. CONCLUSIONS

This work presented a near-threshold ADPLL. A BTRO was proposed to be less affected by the PVT variation and to reduce the supply voltage. The oscillation frequency was 602 MHz at 0.5 V and 40 MHz at 0.2 V. To improve the control of the linearity and resolution, a weighted thermometer-controlled resistor network was proposed for the voltage regulation. The ADPLL was designed and implemented using a 90 nm 1P9M SPRVT CMOS process. It could operate at a frequency of 480 MHz with a 7.9 ps RMS jitter and a phase noise of -94 dBc/Hz at a 1 MHz offset. Its energy efficiency was 163 fJ/cycle at 0.5 V. At 0.25 V, its oscillation frequency was 36.8 to 48 MHz. The RMS jitter was 103 ps at 48 MHz consistent with Table IV and its phase noise was -89.8 dBc/Hz at 1 MHz.

TABLE III
PERFORMANCE COMPARISONS OF LOW-VOLTAGE OSCILLATORS

	JSSC'05 [23]	JSSC'08 [24]	TCASII'09 [25]	TCAS1'10 [26]	TCAS1'11 [8]	BTRO
Process	180 nm	65 nm	130 um	180 nm	90 nm	90 nm
Supply voltage (V)	0.5	0.5	0.5	0.6	0.5	0.2-0.6
OSC-type	LC-VCO	Ring-DCO	Ring-VCO	LC-VCO	Ring-VCO	Ring-VCO
Output phase	2	N/A	6	4	8	10
Tuning range	3.65-3.97 GHz	0.09-1.25 GHz	306-725 MHz	2.4-2.64 GHz	0.4-2.24 GHz	40-771 MHz
Phase noise @1 MHz offset	-119 dBc/Hz @3.8 GHz	N/A	-95 dBc/Hz @ 550 MHz	N/A	-87 dBc/Hz @2.24 GHz	-89 dBc/Hz @771 MHz
Power	570 µW @3.8 GHz	0.9 mW @1.0 GHz	210 µW @ 550 MHz	10.8 mW @2.64 GHz	1.157 mW @2.24 GHz	87.6 µW @771 MHz
Area	0.23 mm^2	N/A	0.017 mm^2	N/A	0.0017 mm^2	0.0019 mm^2
*Figure of merit	0.15 pJ	0.9 pJ	0.382 pJ	4.09 pJ	0.517 pJ	0.114 pJ

$$* \text{ Figure of merit (FoM)} = \frac{\text{Power } (\mu W)}{\text{Freq. (MHz)}} = \text{ Energy per cycle (pJ)}$$

TABLE IV
COMPARISONS OF LOW-VOLTAGE PLLS

	ISSCC'07 [7]	JSSC'08 [24]	TCAS1'10 [26]	JSSC'10 [27]	T.CAS1'11 [8]	This work	
Process	90 nm	65 nm	180 nm	130 nm	90 nm	90 nm	
Supply voltage (V)	Analog: 0.5 Digital: 0.65	0.5	0.6	0.6-1.6	0.5	0.25	0.5
Oscillator type	LC-VCO	Ring-DCO	LC-VCO	Ring-DCO	Ring-VCO	Ring-DCO	
Output phase	2	N/A	4	N/A	8	10	
Operating frequency	2.4-2.6 GHz	0.09-1.25 GHz	2.4-2.64 GHz	10-500 MHz	0.4-2.24 GHz	36.8-48 MHz	0.176-0.48 GHz
Power (mW)	6	1.65 mW @1.0 GHz	14.4 mW @2.5 GHz	7.2 mW @0.5 GHz	2.08 @2.24 GHz	0.003 @48 MHz	0.078 @0.48 GHz
RMS jitter (ps)	N/A	3 @1.0 GHz	N/A	39 @191 MHz	2.22 @2.24 GHz	103 @48 MHz	7.9 @0.48 GHz
Reference spur (dBc)	-52 @2.6 GHz	N/A	-39.83 @2.56 GHz	N/A	-40.28 @2.24 GHz	-39.8 @48 MHz	-42.5 @0.48 GHz
Area (mm^2)	0.14	0.03	1.68 (w/i pads)	0.09	0.074	0.057	
Phase noise (dBc/Hz) @1MHz offset	-121 @2.6 GHz @3MHz offset	N.A.	-105 @2.56 GHz	N/A	-87 @2.24 GHz	-89.8 @48 MHz	-94.0 @0.48 GHz
FoM (pJ)	2.4	1.65	5.76	14.4	0.93	0.062	0.163

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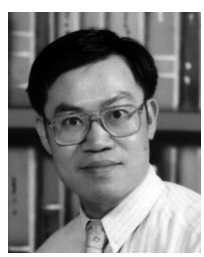

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