Robust ESD Protection Design for 40-Gb/s Transceiver in 65-nm CMOS Process

Chun-Yu Lin, *Member, IEEE*, Li-Wei Chu, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*— To protect a 40-Gb/s transceiver from electrostatic discharge (ESD) damages, a robust ESD protection design has been proposed and realized in a 65-nm CMOS process. In this paper, diodes are used for ESD protection and inductors are used for high-speed performance fine tuning. Experimental results of the test circuits have been successfully verified, including high-speed performances and ESD robustness. The proposed design has been further applied to a 40-Gb/s current-mode logic (CML) buffer. Verified in silicon chip, the 40-Gb/s CML buffer with the proposed design can achieve good high-speed performance and high ESD robustness.**

***Index Terms*— 40 Gb/s, CMOS, electrostatic discharge (ESD), high speed.**

I. Introduction

As CMOS technologies advanced, the high-speed integrated circuits have been designed and fabricated in nanoscale CMOS processes because of their advantages of high integration and potential for mass production [1]–[3]. The high-speed integrated circuits operating at multigiga-bit/second typically adopt core transistor with ultrathin gate oxide. However, the core transistor currently used in nanoscale CMOS technologies is vulnerable to electrostatic discharge (ESD) events [4]–[6]. Furthermore, the thinner metal layer and shallower diffusion junction increase the resistance and local heat of the ESD protection devices, which make the high-speed ESD protection difficult [7].

To sustain the required ESD robustness, such as 2 kV in human-body model (HBM), the on-chip ESD protection device must be large enough [8], [9]. However, the large ESD protection device introduces the large parasitic capacitance (C_{ESD}) at the I/O pads to obviously degrade the circuit performance, as shown in Fig. 1 [10].

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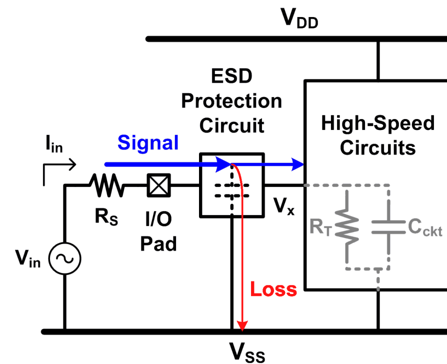

Fig. 1. Signal loss at I/O pad of IC with ESD protection circuit.

There are two major considerations in ESD protection design for high-speed integrated circuits. First, the ESD protection design for high-speed circuits must sustain high enough ESD robustness to effectively protect the MOS transistor in the internal circuits against ESD stresses. Second, the performance degradations of the high-speed circuits because of the parasitic effects of the ESD protection design need to be minimized.

To effectively protect high-speed circuits and to minimize the parasitic effects of ESD protection circuits, several high-speed ESD protection designs have been reported [11]–[19]. The conventional high-speed ESD protection designs will be reviewed in Section II. In Sections III and IV, a robust ESD protection design for 40-Gb/s integrated circuits is presented and verified in a 65-nm CMOS process. The application of the proposed ESD protection circuit to a 40-Gb/s transceiver is presented in Section V.

II. Conventional ESD Protection Designs for High-Speed Applications

A. Dual Diodes

The conventional ESD protection design of dual diodes (D_P and D_N) is shown in Fig. 2, where two ESD protection diodes at I/O pad are assisted with the power-rail ESD clamp circuit [11]–[13]. When D_P and D_N are under forward-biased condition, they can provide efficient discharging paths from I/O pad to V_{DD} and from V_{SS} to I/O pad, respectively. In addition, the power-rail ESD clamp circuit provides the ESD current paths between V_{DD} and V_{SS}.

Fig. 3 shows the simulated transfer function (V_x/I_{in}) of the high-speed circuits with 200-fF capacitance and the dual diodes with 100-fF capacitance, where the dual diodes are expected to sustain 2-kV HBM stress. The transfer function is

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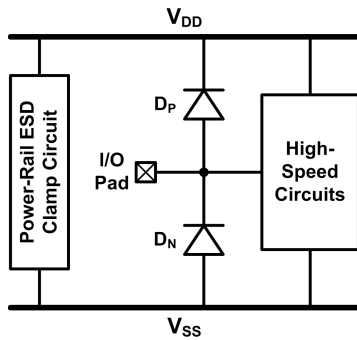

Fig. 2. Dual diodes for high-speed ESD protection.

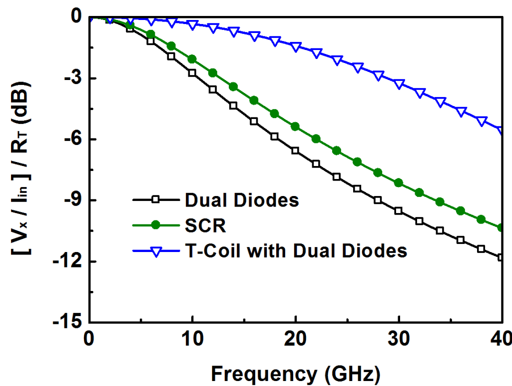

Fig. 3. Simulation results on transfer function of conventional designs.

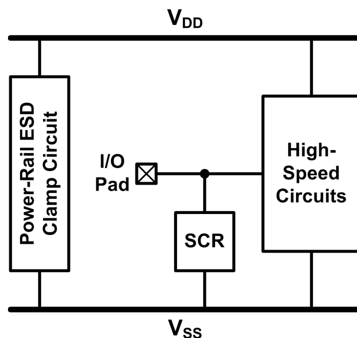

Fig. 4. SCR for high-speed ESD protection.

normalized to the termination resistance ($R_T = 50\ \Omega$). At high frequency, the performance of the high-speed circuits will be seriously degraded because of the parasitic capacitance.

B. Silicon-Controlled Rectifier

The silicon-controlled rectifier (SCR) device has been reported to be useful for high-speed ESD protection design because of its higher ESD robustness within a smaller layout area and lower parasitic capacitance [11], [14], [15]. In addition, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage. The ESD protection design of SCR is shown in Fig. 4, where one SCR provides the ESD current paths between I/O pad and V_{SS}, and the power-rail ESD clamp circuit provides the ESD current paths between V_{DD} and V_{SS}.

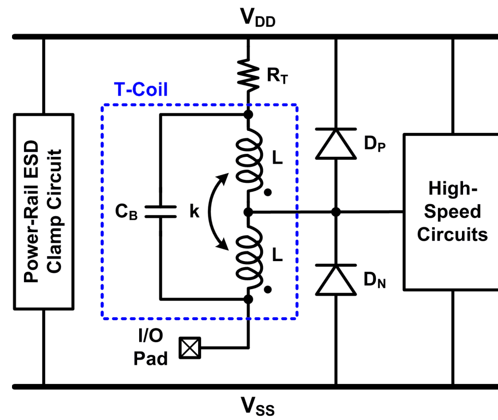

Fig. 5. T-coil with ESD protection devices for high-speed ESD protection.

Fig. 3 shows the simulated transfer function of the high-speed circuits with 200-fF capacitance and the SCR with 50-fF capacitance, where the SCR is expected to sustain 2-kV HBM stress. Even the parasitic capacitance is reduced to 50 fF, the SCR device is still hard to operate up to 40 Gb/s [13].

C. T-Coil With ESD Protection Devices

The T-coil with ESD protection devices for high-speed ESD protection has been reported, as shown in Fig. 5 [16]–[18]. With proper design, this circuit can be recognized that at low and high frequencies, L and C_B short the input to R_T, respectively. This circuit can provide a purely resistive input impedance of R_T, and large ESD protection devices can be used without seriously degrading high-speed performance.

The transfer function of the T-coil network can be calculated as (1), is shown at the top of the next page [20], where C_L denotes the parasitic capacitance of ESD protection devices and high-speed circuits. The simulated transfer function of the T-coil with ESD protection devices is shown in Fig. 3, where the parasitic capacitances of the ESD protection devices and the high-speed circuit are 100 and 200 fF, respectively. The 100-fF ESD protection devices are expected to sustain 2-kV HBM stress. The T-coil network performs inductive peaking with better performance than the dual diodes or SCR.

The T-coil with dual diodes for 40-Gb/s circuit has been realized in submicrometer CMOS process [16]. The SCR has also been used as the ESD protection device in the T-coil-based ESD protection design for 8.5-Gb/s transmitter in 65-nm CMOS process [17]. However, their ESD robustness of the T-coil-based ESD protection designs has not been tested in those works. The nMOS and pMOS transistors with gate-coupled technique are also used in the ESD protection design with T-coil. The T-coil with ESD protection MOS for 10-Gb/s circuit has been realized in 0.18-μm CMOS process with 1-kV HBM ESD robustness [18]. The ESD robustness of the T-coil-based ESD protection designs has to be improved.

III. Proposed ESD Protection Design for High-Speed Applications

In this paper, a robust ESD protection design for 40-Gb/s integrated circuits is presented in a 65-nm CMOS process.

$$\frac{V_x}{I_{\text{in,T-coil with dual diodes}}} = R_{\text{T}} \frac{1 + \frac{L(1+k)}{R_{\text{T}}} s + 2C_{\text{B}} L(1+k) s^2}{1 + C_{\text{L}} R_{\text{T}} s + [2C_{\text{B}} L(1+k) + C_{\text{L}} L] s^2 + 2C_{\text{B}} C_{\text{L}} R_{\text{T}} L(1+k) s^3 + C_{\text{B}} C_{\text{L}} L^2 (1-k^2) s^4} \quad (1)$$

$$\frac{V_x}{I_{\text{in,Proposed design}}} = \frac{R_{\text{T}}}{1 + sC_3 R_{\text{T}}} \times \frac{1 + \frac{L(1+k)}{R_{\text{T}}} s + 2C_{\text{B}} L(1+k) s^2}{1 + C_2 R_{\text{T}} s + [2C_{\text{B}} L(1+k) + C_2 L] s^2 + 2C_{\text{B}} C_2 R_{\text{T}} L(1+k) s^3 + C_{\text{B}} C_2 L^2 (1-k^2) s^4} // \frac{1}{sC_1} \quad (2)$$

Fig. 6 shows the proposed ESD protection circuit. Such ESD protection design consists of a pair of inductors (L) with coupling factor (k), a terminate resistor (R_{T}), and three pairs of ESD protection diodes (D_{P1}, D_{N1}, D_{P2}, D_{N2}, D_{P3}, and D_{N3}). The distributed diodes can reduce the ESD-generated heat across each diode, and the ESD robustness can be improved. Suppose the parasitic capacitances of D_{P1}–D_{N1} pair, D_{P2}–D_{N2} pair and high-speed circuits, and D_{P3}–D_{N3} pair are C_1, C_2, and C_3, respectively. This design can be recognized that at low frequencies, L shorts the input to R_{T}, and at high frequencies, C_{B} plays the same role while L, C_1, C_2, and C_3 are also matched using distributed ESD protection scheme [21]. The transfer function ($V_{\text{x}}/I_{\text{in}}$) of the proposed ESD protection circuit can be calculated as (2), is shown at the top of the page. The distributed diodes are used to improve the ESD robustness. The sizes of inductors and ESD protection diodes can be designed to expand the bandwidth and minimize the performance degradations.

When the ESD protection diodes are under forward-biased condition, they can provide efficient discharging paths from I/O pad to V_{DD} or from V_{SS} to I/O pad. In addition, the power clamp that consists of an RC-inverter-triggered nMOS provides the ESD current paths between V_{DD} and V_{SS}. As positive-to-V_{DD} (PD) [negative-to-V_{SS} (NS)] ESD stresses at I/O pad, the ESD current is discharged through the paths of D_{P1}, D_{P2}, and D_{P3} (D_{N1}, D_{N2}, and D_{N3}). As positive-to-V_{SS} (PS) [negative-to-V_{DD} (ND)] ESD stresses at I/O pad, the ESD current is discharged to the floating V_{DD} (V_{SS}) first, and then discharged to the grounded V_{SS} (V_{DD}) through the turn-on efficient power clamp. The proposed ESD protection circuit provides the corresponding current discharging paths among the ESD test pin combinations. Under normal circuit operating conditions, the ESD protection diodes are kept off with some parasitic capacitance.

Fig. 7 shows the transfer function of the proposed design with different diode sizes. The transfer function is normalized to the termination resistance. In Fig. 7, the parasitic capacitances of D_{P1}–D_{N1}/D_{P2}–D_{N2}/D_{P3}–D_{N3} pairs have been chosen as (a) 20/60/20 fF, (b) 40/20/40 fF, and (c) 50/0/50 fF. These capacitances are estimated as the input level is 200 mV. The 100-fF ESD protection devices are expected to sustain 2-kV HBM stress. The parasitic capacitance of the high-speed circuit is kept at 200 fF. The simulated transfer function of the proposed design can compete with that of the T-coil network, even if the frequency is up to 40 GHz. The proposed design is suitable for broadband ESD protection.

IV. Verification in Silicon

A. Test Circuits

The proposed ESD protection circuit was split with different sizes of ESD protection diodes for tests, including proposed designs A and B. In the proposed design A, the width of D_{P1}, D_{P2}, and D_{P3} (D_{N1}, D_{N2}, and D_{N3}) are selected to 24, 12, and 24 μm, respectively. In the proposed design B, the width of D_{P1}, D_{P2}, and D_{P3} (D_{N1}, D_{N2}, and D_{N3}) are selected to 30, 0, and 30 μm, respectively, where the 0 μm means D_{P2} and D_{N2} are removed in the test circuit. The inductors are all ~0.23 nH in the proposed designs.

For comparison purpose, the T-coil with dual diodes is also implemented in this paper. The widths of D_{P} and D_{N} are selected to 60 μm. The inductors are ~0.25 nH in the T-coil network.

The simulated eye diagrams of the received data of each design are shown in Figs. 8 and 9. The input level is kept at 200 mV, and the data rate is kept at 40 Gb/s. The eye height and width are defined according to [22]. The simulated eye diagrams of T-coil with dual diodes, proposed design A, and proposed design B at 40 Gb/s exhibit eye height (eye width) of 80 mV (17 ps), 90 mV (19 ps), and 95 mV (18.8 ps), respectively.

The test circuits have been fabricated in a 65-nm CMOS process. Each test circuit occupies an area of 85 × 95 μm^2. To facilitate two-port measurement on a probe station, the test circuits are arranged with ground-signal-ground pads. Fig. 10 shows one of the test circuits (proposed design A).

B. Measurement Results

The eye diagrams of the test circuits have been measured on the probe station using a 40-Gb/s bit stream generated by multiplexing four 10-Gb/s random data channels. The input level is kept at 200 mV. Figs. 11–13 show the measured eye diagrams. The test environment (including cable and probe) also causes the performance degradation. The eye diagram with degradation because of the cable and probe is shown in Fig. 11, where its eye height (eye width) at 40 Gb/s is 23.7 mV (17.28 ps). The eye diagram of T-coil with dual diodes is shown in Fig. 12, where its eye height (eye width) at 40 Gb/s is 20.7 mV (18.53 ps). The eye diagrams of proposed design A and B at 40 Gb/s exhibit eye height (eye width) of 22.8 mV (18.76 ps) and 23.9 mV (18.86 ps), as shown in Fig. 13.

The HBM ESD robustness is tested according to the ESDA/JEDEC (Joint Electron Device Engineering Council)

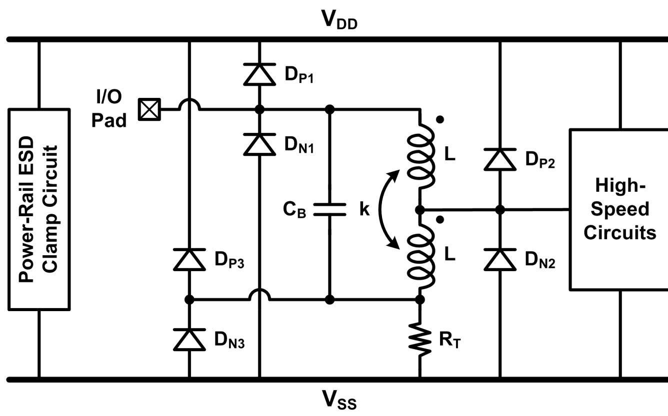

Fig. 6. Proposed design for high-speed ESD protection.

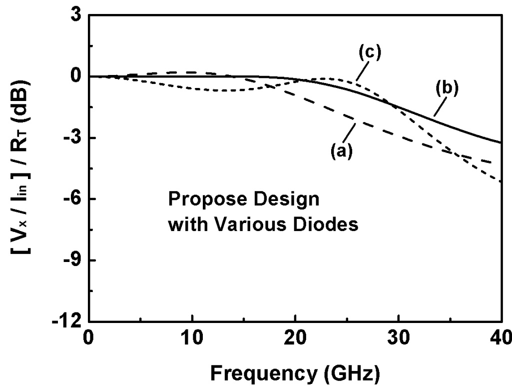

Fig. 7. Simulation results on transfer function of proposed design.

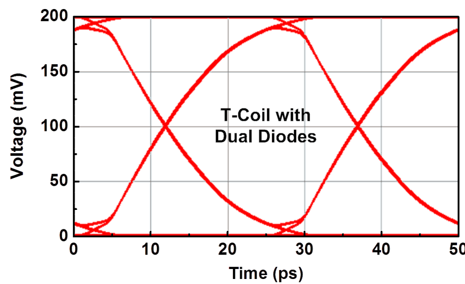

Fig. 8. Simulation result on eye diagram of T-coil with dual diodes.

joint standard [23]. The positive and negative zapping are stressed to I/O pad with V_{DD} or V_{SS} connected to ground. The failure criterion is defined as the I–V characteristics shifting over 30% from its original curve after ESD stressed at every ESD test level. The PS, PD, NS, and ND HBM ESD robustness of all the test circuits are measured, as listed in Table I. The measured HBM ESD robustness of the T-coil with dual diodes, proposed design A, and proposed design B are 1.75, 2.5, and 2.25 kV, respectively, which are obtained from the lowest levels among the ESD test pin combinations.

A transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulsewidth is used to evaluate the secondary breakdown current (It_2), which suggested the current-handling ability in the time domain of HBM ESD event, of ESD protection circuit. Fig. 14 shows the measured TLP

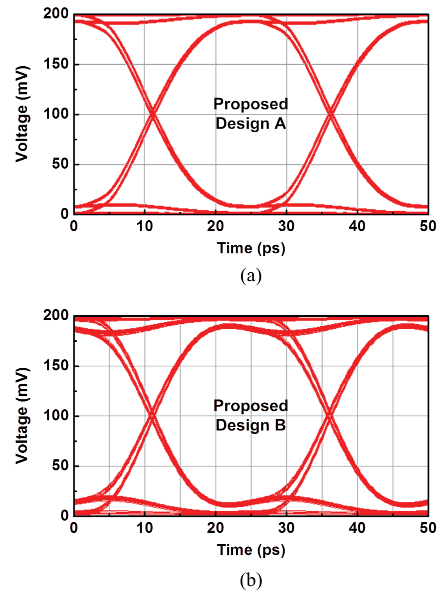

Fig. 9. Simulation result on eye diagram of (a) proposed design A and (b) proposed design B.

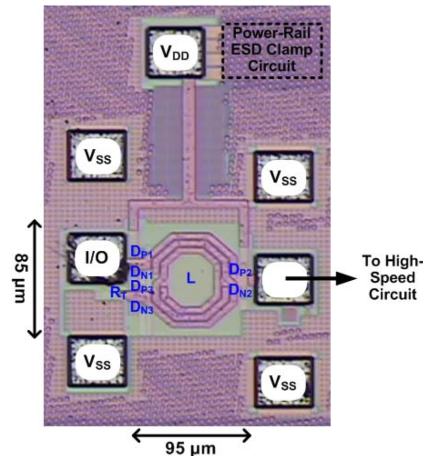

Fig. 10. Chip micrograph of proposed design A.

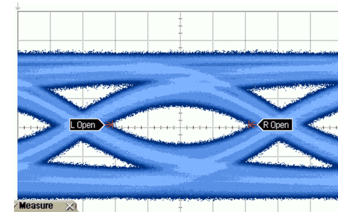

Fig. 11. Measurement result on eye diagram with degradation because of test environment. Horizontal scale: 5 ps/div. Vertical scale: 50 mV/div.

I–V curves of the test circuits. The T-coil with dual diodes, proposed design A, and proposed design B can achieve the TLP-measured It_2 of 1.08, 1.75, and 1.61 A, respectively.

Another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulsewidth is also used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) event. Fig. 15 shows the measured VF-TLP I–V curves of the test circuits. The

TABLE I
ESD PROTECTION DESIGNS

	Test Environment	ESD Protection Circuit			CML Buffer	
		T-Coil with Dual Diodes	Proposed Design A	Proposed Design B	T-Coil with Dual Diodes	Proposed Design A
D_{P1}, D_{N1}	N/A	N/A	24μm	30μm	N/A	24μm
D_{P2}, D_{N2}	N/A	N/A	12μm	0μm	N/A	12μm
D_{P3}, D_{N3}	N/A	N/A	24μm	30μm	N/A	24μm
Total ESD Diodes	N/A	60μm	60μm	60μm	60μm	60μm
Circuit Area	N/A	85x95μm^2	85x95μm^2	85x95μm^2	280x650μm^2	280x650μm^2
Eye Amplitude at 40Gb/s	113.9mV	73.5mV	74.0mV	74.2mV	124.0mV	127.0mV
Eye Height at 40Gb/s	23.7mV	20.7mV	22.8mV	23.9mV	10.0mV	34.0mV
Eye Width at 40Gb/s	17.28ps	18.53ps	18.76ps	18.86ps	15.31ps	17.14ps
PS HBM Level	N/A	1.75kV	2.5kV	2.25kV	1.75kV	2.5kV
PD HBM Level	N/A	2kV	2.5kV	2.25kV	2kV	2.5kV
NS HBM Level	N/A	2.5kV	3.5kV	3kV	2.5kV	3.5kV
ND HBM Level	N/A	2.5kV	3.5kV	3kV	2.5kV	3.5kV
TLP It_2	N/A	1.08A	1.75A	1.61A	1.05A	1.69A
VF-TLP It_2	N/A	1.71A	2.95A	2.88A	1.77A	2.99A

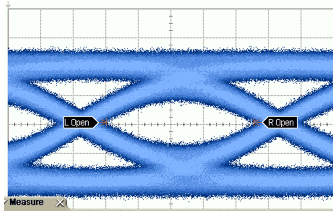

Fig. 12. Measurement result on eye diagram of T-coil with dual diodes. Horizontal scale: 5 ps/div. Vertical scale: 50 mV/div.

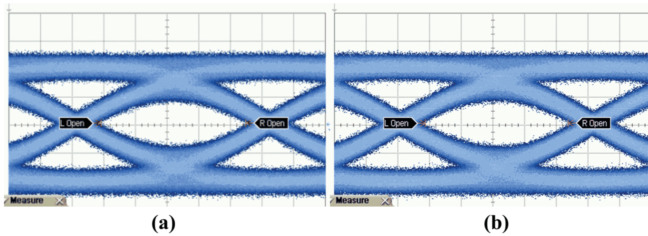

Fig. 13. Measurement result on eye diagram of (a) proposed design A and (b) B. Horizontal scale: 5 ps/div. Vertical scale: 50 mV/div.

VF-TLP-measured It_2 of T-coil with dual diodes, proposed design A, and proposed design B are 1.71, 2.95, and 2.88 A, respectively. The measured peak overshoot voltage versus VF-TLP current under such fast-transient CDM-like stress condition is shown in Fig. 16.

V. ESD PROTECTION DESIGN APPLIED TO 40-Gb/s CML

CMOS current-mode logic (CML) style was introduced to implement ultrahigh speed buffers, latches, multiplexers and demultiplexers, and frequency dividers [24]–[26]. The CML circuits can operate with lower signal voltage and higher operating frequency at lower supply voltage than static CMOS circuits, so the CML buffers are suitable for high-speed applications. The other advantage of the differential CML buffer includes its large-signal behavior in response to a differential input signal. Moreover, the differential CML buffer exhibits high bandwidth. This paper presents a CML buffer design and introduces ESD protection.

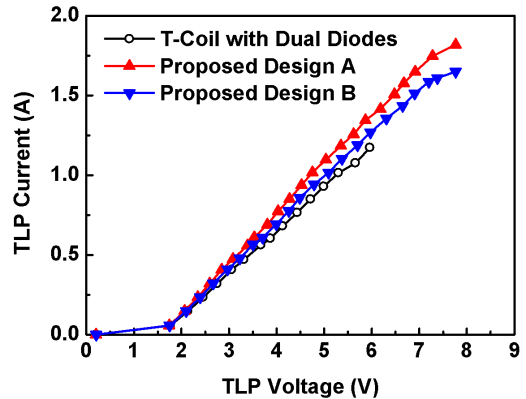

Fig. 14. TLP I–V curves of test circuits.

Fig. 17 shows the 40-Gb/s CML buffer with differential architecture. The tail currents controlled by the V_B provide the input-independent biasing for the circuit. The ESD protection circuits, proposed design A and T-coil with dual diodes have been applied to the CML buffers, as shown in Fig. 17. These CML buffers with ESD protection circuits have been fabricated in the same 65-nm CMOS process. Fig. 18 shows the chip micrographs of the CML buffer with the proposed design A.

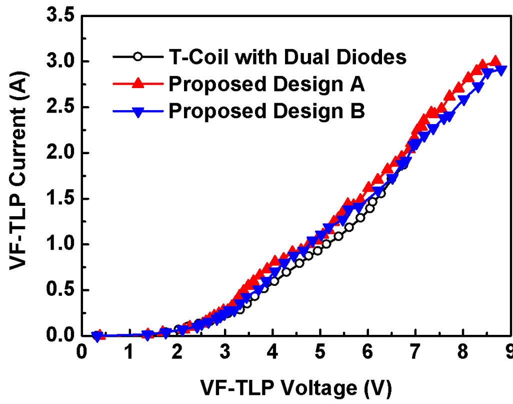

Fig. 15. VF-TLP I–V curves of test circuits.

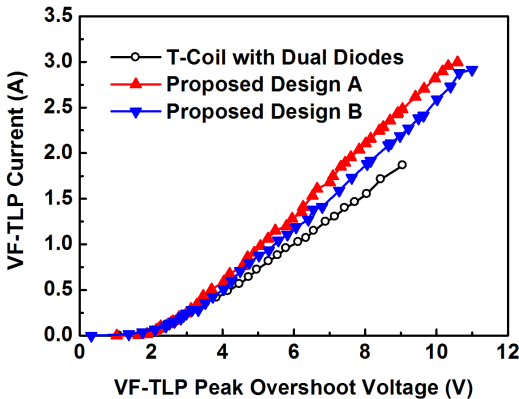

Fig. 16. VF-TLP-measured peak overshoot voltage of test circuits.

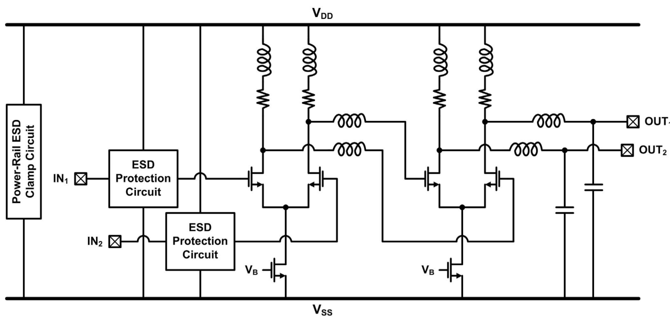

Fig. 17. Circuit schematic diagram of 40-Gb/s CML with ESD protection circuits.

The eye diagrams of the test circuits have been measured on the probe station. The input level is kept at 200 mV. Fig. 19(a) and (b) shows the measured eye diagrams of CML buffer with T-coil ESD protection at 35 and 40 Gb/s, respectively. After the proposed ESD protection circuit is applied at the I/O pads of CML buffer, Fig. 20(a) and (b) shows the measured eye diagrams of CML buffer with proposed design A at 35 and 40 Gb/s, respectively. The eye amplitude, eye height, and eye width [22] of CML buffer with T-coil ESD protection at 40 Gb/s are 124.0 mV, 10.0 mV, and 15.31 ps, respectively, whereas those of CML buffer with proposed design A at 40 Gb/s are 127.0 mV, 34.0 mV, and 17.14 ps, respectively.

The ESD robustness and TLP testing of the ESD-protected CML buffers have also been evaluated. The PS, PD, NS, and ND HBM ESD robustness of both CML buffers are measured. The measured HBM ESD robustness of the CML buffers with T-coil ESD protection and that with proposed design A are 1.75 and 2.5 kV, respectively. The TLP-measured It_2 of the CML buffers with T-coil ESD protection and that with proposed design A are 1.05 and 1.69 A, respectively, whereas the VF-TLP-measured It_2 are 1.77 and 2.99 A, respectively. These measurement results are summarized in Table I.

To verify the ESD protection ability of the ESD protection circuits, the eye diagrams of both CML buffers after ESD tests are remeasured. After 1.75-kV HBM ESD stresses to the CML buffer with T-coil ESD protection, the eye height and width at 40 Gb/s are 10.0 mV and 15.85 ps, respectively. Once 2.5-kV HBM ESD stresses to the CML buffer with proposed design A, the eye height and width at 40 Gb/s are 34.0 mV and 16.22 ps, respectively. The measured eye diagrams can be still satisfactory.

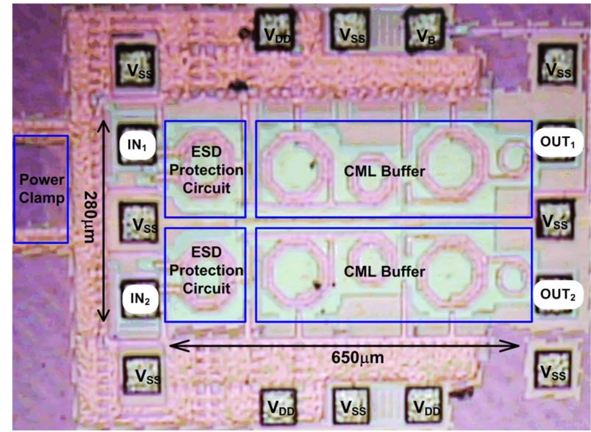

Fig. 18. Chip micrograph of 40-Gb/s CML with ESD protection circuits.

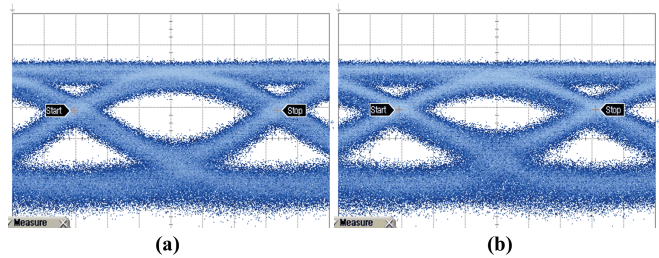

Fig. 19. Measurement results on eye diagrams of CML with T-coil ESD protection at (a) 35 and (b) 40 Gb/s. Horizontal scale: 5 ps/div. Vertical scale: 50 mV/div.

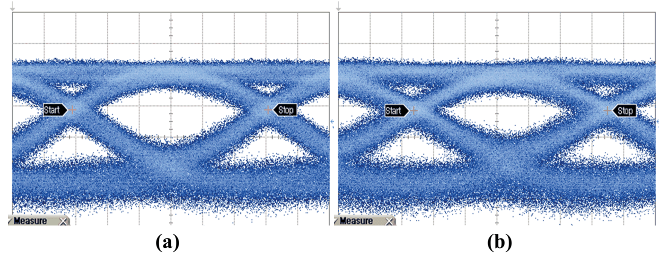

Fig. 20. Measurement results on eye diagrams of CML with proposed ESD protection at (a) 35 and (b) 40 Gb/s. Horizontal scale: 5 ps/div. Vertical scale: 50 mV/div.

VI. Conclusion

The new ESD protection design with good high-speed performance and high ESD robustness has been developed for the 40-Gb/s applications. The test circuits have been investigated in 65-nm CMOS process, in which the proposed design A with 22.8-mV (18.76 ps) eye height (eye width) at 40 Gb/s and 2.5-kV HBM ESD robustness has been applied to a CML buffer. The experimental results validate the feasibility of the ESD protection design on the 40-Gb/s CML buffer with 34.0-mV (17.14 ps) eye height (eye width) at 40 Gb/s and 2.5-kV HBM ESD robustness in the same 65-nm CMOS process.

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