Statistical Model and Rapid Prediction of RRAM SET Speed–Disturb Dilemma

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Abstract—A comprehensive study of SET speed—disturb dilemma in resistive-switching random access memory (RRAM) is presented using statistically based prediction methodologies, accounting for the stochastic nature of SET. An analytical percolation model has been successful in explaining the statistical Weibull distribution of SET time and SET voltage in addition to the power-law voltage-time dependence. Two prediction methodologies using constant voltage stress (CVS) and ramp voltage stress (RVS) are proposed to evaluate the SET speed—disturb properties. The RVS method reduces analysis time and cost and yields equivalent results as the CVS method. Furthermore, the RVS method is used to evaluate the device design space and the current status of RRAM technology to meet the strict requirement of the SET speed—disturb dilemma.

Index Terms—Disturb, ramp voltage stress (RVS), resistiveswitching random access memory (RRAM), SET speed, SET statistics.

I. INTRODUCTION

RESISTIVE-SWITCHING random access memory (RRAM) has the potential to become the front-runner of future nonvolatile memory because of its simple structure, fast switching speed, low operating voltage, and excellent scalability. The resistive-switching (RS) mechanism has been explained by the partial connection and rupture of conducting filaments (CFs) in metal oxides [1]. The transition from a high resistance state (HRS) to a low resistance state (LRS) is called SET, and the opposite transition from LRS to HRS is called RESET. Reliability is one of the primary bottlenecks of RRAM before it can be put to commercial applications. In addition to long-term retention and cycling endurance, disturbance of resistance state is one of the most prominent reliability concerns. HRS disturbance occurs at two occasions in RRAM array. First, read disturb occurs when the selected HRS cell is not intended to be programmed but changes its state to LRS after numerous read operations. Second, in the crossbar RRAM array, the unselected HRS cells after

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numerous SET operations would suffer write disturb because of the voltage stress of one-third or one-half of the SET voltage (V_{SET}) when using the V/3 or V/2 write scheme [2].

HRS disturbance is analogous to SET and differs only in the magnitude of the applied voltage. In contrast to the requirement of a long read or write disturb time, a short SET pulse is required for high-speed applications. Additionally, while a higher read voltage is desirable to improve read speed and reduce sensing noise, a lower $V_{\rm SET}$ reduces power consumption and is more compatible with the operating voltage of the peripheral circuits. To fulfill the mentioned requirements, the tradeoff between the SET speed and disturb immunity has to be carefully engineered using a highly nonlinear voltagetime (V - t) dependence at SET [3]–[7]. This is also known as the SET speed-disturb dilemma [5]. However, most studies have not considered the random variation effect of the SET time (t_{SET}) on the SET speed-disturb dilemma. The t_{SET} variation is distributed across several orders of time [5], [6], causing unacceptable error in predicting the SET speeddisturb properties. Therefore, a statistical methodology for predicting the SET speed-disturb dilemma by considering the variation effect is needed.

The random nature of the SET behavior can be explained using a percolation model similar to that of dielectric breakdown [6], [7]. The general models of the SET process and oxide breakdown both indicate that the defects are first generated randomly in the oxide during voltage stress, thereby triggering the breakdown once a connected defect path permeates the entire oxide layer. The difference between the SET process and oxide breakdown is that the latter occurs in the entire oxide layer while the former occurs only in the ruptured CF region formed by the RESET process. To describe the random nature of the SET process, several numerical models have simulated the V_{SET} distribution by modeling the random generation of defects in the oxide layer [8], [9]. Long et al. also established an analytical model of the $V_{\rm SET}$ distribution by analogy with the cell-based percolation model proposed for oxide breakdown [10].

This paper describes a comprehensive analysis of the SET speed–disturb dilemma of RRAM by considering statistical SET variation. The theoretical framework, testing methodology, device design guideline, and present status of RRAM technology are discussed. The remainder of this paper is organized as follows. Section II describes the RRAM devices used in the testing. Section III introduces an analytical percolation model of $t_{\rm SET}$ statistics, which is also based on the

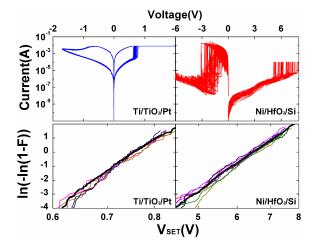


Fig. 1. (Top) Typical bipolar I–V switching characteristics of the HfO₂ and the TiO₂ devices. (Bottom) V_{SET} distribution of six devices at different wafer sites. The solid black line represents the collected distribution of all devices.

oxide breakdown theory [11]. The model provides a thorough explanation of the stochastic nature of the t_{SET} variation and voltage dependence of the experimental data. Based on the derived Weibull distribution and voltage acceleration relation in the model, Section IV presents a statistical projection procedure for SET speed-disturb properties using constant voltage stress (CVS). However, the conventional CVS testing requires substantial time. Section V shows that the essential parameters of the Weibull distribution and voltage acceleration relation measured by time-consuming CVS testing can be extracted directly using a ramped voltage stress (RVS) testing, and then proposes a rapid prediction method based on RVS to reduce the time and cost of reliability testing. Furthermore, a device design guideline for the desired SET speed-disturb properties is discussed. Finally, because of the rich RVS data available in the literature, Section VI discusses the current status of RRAM technology in meeting the strict requirement of the SET speed-disturb dilemma.

II. EXPERIMENTAL PROCEDURE

Fig. 1 shows typical dc current-voltage (I - V) switching curves of two distinct bipolar RRAM devices used in this paper. The Ti/TiO₂/Pt device is based on the valance-change RS mechanism [1], [12], and the Ni/HfO₂/Si device is based on both electrochemical and thermochemical RS mechanisms [1], [13]. The switching characteristics and mechanism have been discussed in detail elsewhere [12], [13]. The device area was 4 μ m² for TiO₂ devices and 10⁴ μ m² for HfO₂ devices. A voltage was applied to the top electrodes at room temperature, whereas the bottom electrodes were grounded. Both devices exhibited reproducible bipolar RS after the initial forming process. t_{SET} and V_{SET} were measured using conventional CVS and RVS procedures on cells that were first programmed to the HRS. Fig. 2 shows the typical currenttime traces and t_{SET} distribution for CVS. Current compliance was set to 8 mA and 100 μ A for the TiO₂ and HfO₂ devices, respectively, and the same values were applied to CVS and RVS. A minimum of 100 RS cycles were measured for every CVS and RVS condition. Random variation on

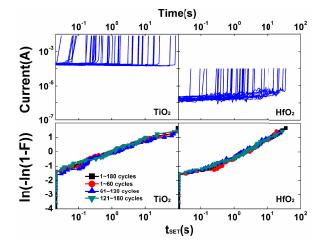


Fig. 2. (Top) Typical constant voltage stress (CVS) current–time traces of the TiO_2 device at 0.72 V and the HfO_2 device at 6 V. (Bottom) t_{SET} distribution of the TiO_2 device at 0.72 V and the HfO_2 device at 6 V for every 60 switching cycles.

resistance, $t_{\rm SET}$, and $V_{\rm SET}$ showed that no additional stress effect occurred during cycling. Although a relatively large spread of HRS current was observed in the HfO₂ device, no apparent trend between the HRS current and SET variation was observed in the sample.

The SET variation was substantial even for an identical device under cycling. Fig. 1 also shows that the variation of $V_{\rm SET}$ among different cells was significantly less than that of an identical cell under cycling. The percolation model in the next section presents an explanation of this intrinsic stochastic nature. Instead of measuring numerous cells, which would be susceptible to other extrinsic effects such as device uniformity, an identical cell was reset at a negative bias after every CVS or RVS measurement. To select the representative cell, an upfront screening using RVS was first applied to cells across the wafer.

III. SET TIME STATISTICS AND ANALYTIC MODEL

The SET process has been explained by the formation of a defect-related conduction path across the oxide layer. The large variation of $V_{\rm SET}$ and $t_{\rm SET}$ is related to the random nature of CF formation. Most RRAM statistical models are focused on interpreting the $V_{\rm SET}$ variation observed from fast RVS tests [10]. However, only the $t_{\rm SET}$ variation correlates directly to the pulse SET or read operation of practical applications. The $t_{\rm SET}$ variation deteriorates the SET speed–disturb dilemma and complicates the choice of a reliable SET or read condition. To properly understand the cause of $t_{\rm SET}$ variation, the analytic percolation model is used to describe the $t_{\rm SET}$ statistics in this section. This model also provides an explanation of the measured Weibull distribution and power-law voltage dependence of $t_{\rm SET}$, which are crucial for further prediction of the SET speed–disturb properties.

Fig. 3 shows a schematic of the cell-based percolation model [10], [11]. After the RESET process, the CF rupture formed an isolation region between the two virtual electrodes consisting of the remaining CF. This region is divided by cubic cells with a lattice constant a_0 . The isolation region is assumed to be divided into N_c columns, with each column composed of

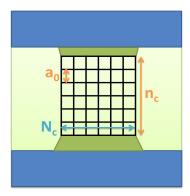


Fig. 3. Schematic of the cell-based SET model. The ruptured isolation region between two virtual electrodes is divided into N_C columns with each column composed of n_C cells.

 n_c cells. Therefore, the thickness $(T_{\rm gap})$ and area $(A_{\rm gap})$ of the isolation region can be expressed by $T_{\rm gap} = n_c a_o$ and $A_{\rm gap} = N_c a_o^2$. During the SET or read process, defects are randomly generated in the isolation region because of the electrical stress effect. A cubic cell turns into a defective state when a defect is generated in this cell. The SET event occurs once all the cells in one of the N_c columns become defective and create a conductive leakage path between the two virtual electrodes.

The cumulative failure distribution function (CDF) of each cell, λ , can be assumed to be the fraction of defective cells in the isolation region [11]. Therefore, the CDF of all n_c cells in one column that are defective is λ^{n_c} . Because SET occurs once any one of the N_c columns is thoroughly defective, the CDF of that SET does not occur and can be expressed as

$$1 - F(\lambda) = (1 - \lambda^{n_c})^{N_c} \tag{1}$$

where F is the CDF of SET. Previous studies have reported that F follows the Weibull distribution, which is typically plotted according to Weibit [5], [6]. The Weibit $W_{\rm SET}$ is given by

$$W_{\text{SET}} = \ln\{-\ln[1 - F(\lambda)]\} = \ln[-N_c \ln(1 - \lambda^{n_c})].$$
 (2)

Because $\lambda \ll 1$ is satisfied in HRS, it follows that $\ln(1-\lambda^{n_c}) \approx -\lambda^{n_c}$. $W_{\rm SET}$ can be approximated as

$$W_{\text{SET}} = \ln(N_c) + n_c \ln(\lambda). \tag{3}$$

To compare with the experimental data, λ follows a power law of stress time t in the oxide breakdown model [11], [14], i.e.,

$$\lambda(t) = \xi \cdot t^{\alpha} \tag{4}$$

where α is the power-law coefficient, which is roughly voltage-independent [15], and ξ is the defect generation efficiency which is strongly dependent on the stress voltage $(\xi \propto V^m)$ [14]. Equation (3) can be expressed as

$$W_{\text{SET}} = \ln(N_c) + n_c \ln \xi + n_c \alpha \cdot \ln(t_{\text{SET}})$$

$$= n_c \alpha \cdot \left\{ \ln(t_{\text{SET}}) - \ln \left[\xi^{\frac{1}{\alpha}} (N_c)^{\frac{1}{n_c \alpha}} \right]^{-1} \right\}$$
 (5)

which complies with the shape of the Weibull distribution as

$$W_{\text{SET}} = \ln[-\ln(1 - F)] = \beta[\ln(t_{\text{SET}}) - \ln(t_{63\%})]$$
 (6)

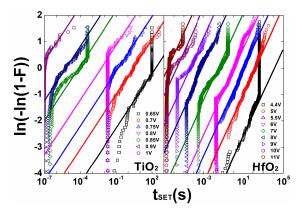


Fig. 4. t_{SET} Weibull distribution of the TiO₂ and the HfO₂ devices at different CVS voltages, showing constant β of 0.3 (TiO₂) and 0.37 (HfO₂).

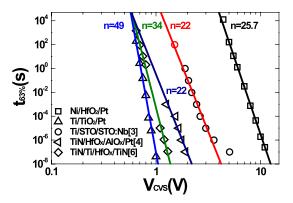


Fig. 5. $t_{63\%}$ as a function of $V_{\rm CVS}$ for the TiO₂ and the HfO₂ devices, showing a power-law V-t relation with different voltage acceleration factors n. Reported data of other RRAMs in the literature [3], [4], and [6] are also plotted for comparison.

where the Weibull slope β and the characteristic time at the 63rd failure percentile $t_{63\%}$ are given by

$$\beta = n_c \alpha \tag{7}$$

$$t_{63\%} = \xi^{-\frac{1}{\alpha}} \cdot N_c^{-\frac{1}{n_c \alpha}}.$$
 (8)

Fig. 4 shows $t_{\rm SET}$ Weibull distributions of the TiO₂ and HfO₂ devices measured at different CVS voltages $V_{\rm CVS}$. β shows little dependence on $V_{\rm CVS}$, in good agreement with (7). Furthermore, Fig. 5 plots $t_{63\%}$ as a function of $V_{\rm CVS}$ across 10 orders of magnitude in time, showing a highly nonlinear power-law V-t relation because

$$t_{63\%} \propto \xi^{-\frac{1}{\alpha}} \propto V^{-\frac{m}{\alpha}} \propto V^{-n} \tag{9}$$

where n is the voltage acceleration factor. The various V-t relations reported in different RRAMs [3], [4], and [6] also show a similar power-law dependence. The n values of different RRAM devices are between 20 and 50. This power-law V-t dependence is also consistent with the experimental results in the ultrathin oxide breakdown [14], further confirming that $T_{\rm gap}$ is much less than the entire thickness of the oxide layer. Furthermore, β and $t_{\rm 63\%}$ of the $t_{\rm SET}$ distribution are directly related to $T_{\rm gap}$ and $A_{\rm gap}$, respectively, by assuming a constant a_0 according to (7) and (8) [11], [16]. The $t_{\rm SET}$

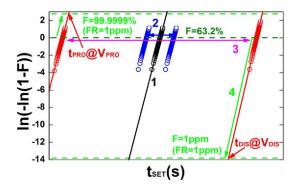


Fig. 6. Four-step program time (t_{PRO}) and disturb time (t_{DIS}) prediction procedure at used program voltage (V_{PRO}) and disturb voltage (V_{DIS}), for satisfying 1 ppm FR.

distributions of the measured devices in Fig. 2 show no cycling dependence. Therefore, $T_{\rm gap}$ and $A_{\rm gap}$ remain nearly constant during repeated cycling.

IV. STATISTICAL PREDICTION OF SET SPEED–DISTURB DILEMMA USING CVS

A statistical failure ratio (FR) criterion is used for evaluating the SET speed–disturb properties. The SET FR is the CDF of the unsuccessful SET event and is equal to (1-F). The disturb FR is the CDF of the disturb event from HRS to LRS and is equal to F. The FR should be adequately low for ensuring accuracy of the stored data. The SET speed–disturb properties for the required operation conditions and failure criteria can be projected based on data from conventional CVS tests once the distribution and acceleration behavior of $t_{\rm SET}$ are known.

The statistical prediction procedures of the SET speed–disturb properties using the CVS testing involve four main steps, as illustrated in Fig. 6.

- 1) First, the Weibull distribution of t_{SET} is collected at an accelerated voltage to extract the $t_{63\%}$ and β values by using (6).
- 2) The $t_{63\%}$ values at various accelerated test voltages are then used to extract the voltage acceleration factor n by using (9).
- 3) Because β shows less dependence with the stress voltage, the $t_{\rm SET}$ distributions can be projected to the used program voltage ($V_{\rm PRO}$) and disturb voltage ($V_{\rm DIS}$) by the power-law V-t relationship.
- 4) Finally, the $t_{63\%}$ values can be extrapolated to the low FR target to extract the program time (t_{PRO}) and the disturb time (t_{DIS}) values.

V. FAST RVS PREDICTION METHOD

Multiple test voltages to extract n in the mentioned CVS method require substantial measurement time especially when low test voltages are used. Compared to the conventional time-consuming CVS test, RVS is typically several orders of magnitude faster and widely used in the industry for evaluating oxide breakdown properties [17]. In this section, the conversion concept between the $V_{\rm SET}$ distribution of the RVS test and the $t_{\rm SET}$ distribution of the CVS test is first

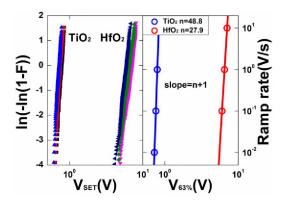


Fig. 7. (Left) V_{SET} distributions obtained using different RR values. (Right) $V_{63\%}$ versus RR in a double-logarithmic plot, where the slope corresponds to n+1.

discussed. By taking advantage of short measurement time of RVS, this paper proposes a method for rapidly predicting the SET speed–disturb properties.

RVS is equivalent to a series of discrete CVS with linearly ascending stress voltages. In [17], the complete conversion between RVS and CVS has been derived. The equivalent t_{SET} at any given V_{CVS} is given by

$$t_{\text{SET@}V_{\text{CVS}}} = \frac{V_{\text{CVS}}}{\text{RR} \cdot (n+1)} \cdot \left(\frac{V_{\text{SET}}}{V_{\text{CVS}}}\right)^{n+1}$$
(10)

where RR is the constant ramp rate. The power-law voltage dependence of t_{SET} is assumed. The V_{SET} distribution of the RVS also follows the Weibull distribution as

$$\ln[-\ln(1-F)] = \beta_{\text{RVS}}[\ln(V_{\text{SET}}) - \ln(V_{63\%})]$$
 (11)

where β_{RVS} and $V_{63\%}$ are the Weibull slope and characteristic voltage at the 63^{rd} failure percentile using RVS, and are given by

$$\beta_{\text{RVS}} = \beta \cdot (n+1),\tag{12}$$

$$V_{63\%} = \left[t_{63\%} \cdot \text{RR} \cdot (n+1) V_{\text{CVS}}^{n}\right]^{\frac{1}{n+1}}.$$
 (13)

Furthermore, because $t_{63\%}$ at a fixed V_{CVS} is constant in (13), the relationship between RR and $V_{63\%}$ of RVS is as follows:

$$(n+1) \cdot \ln(V_{63\%}) = \text{const.} + \ln(RR)$$
 (14)

which can be used to extract the voltage acceleration factor n. Fig. 7 shows that the measured $V_{63\%}$ of the TiO₂ and the HfO₂ devices follows the Weibull distribution at three different RRs. The extract n values for the TiO₂ and the HfO₂ devices are 48.8 and 27.9, respectively, using the RVS method. The values are nearly identical to those obtained using the CVS method in Fig. 5. Fig. 8 shows the excellent agreement between the converted $t_{\rm SET}$ from the RVS data using (10) and the measured CVS data regardless of the values of $V_{\rm CVS}$ and RR. The above results validate that the RVS method yields $t_{\rm SET}$ distributions and n equivalent to those of the time-consuming CVS method. The conversion is independent of the RS material (TiO₂ and HfO₂) and use conditions RR and $V_{\rm CVS}$.

Because the CVS parameters n, $t_{63\%}$, and β can be extracted from the RVS parameters RR, $V_{63\%}$, and β_{RVS} , the SET

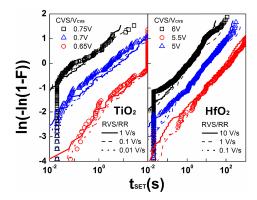


Fig. 8. t_{SET} of the TiO₂ and the HfO₂ devices measured by CVS (symbol) and converted from RVS (line). The excellent agreement in the RVS-CVS conversion using (10) is independent of RR and V_{CVS} .

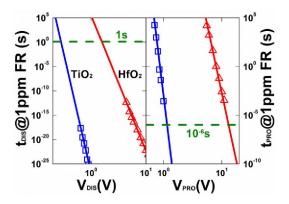


Fig. 9. (Left) t_{DIS} versus V_{DIS} , and (right) t_{PRO} versus V_{PRO} at 1 ppm FR. The symbols refer to the CVS measurement at multiple stress voltages, and the lines refer to the rapid RVS projection according to (15) and (16).

speed–disturb properties can be estimated directly using RVS. Substituting the $V_{\rm SET}$ of (10) into (11), the $V_{\rm DIS}$ and $V_{\rm PRO}$ of CVS at the acceptable FR criteria are the functions of $t_{\rm PRO}$ and $t_{\rm DIS}$, respectively, as follows:

$$\cong V_{63\%} \cdot \left[\ln \left(\frac{1}{1 - FR} \right) \right]^{\frac{1}{\beta_{RVS}}} \cdot \left(\frac{1}{RR \cdot t_{DIS}} \right)^{\frac{1}{n}} \cdot \left(\frac{1}{n+1} \right)^{\frac{1}{n}}$$

$$(15)$$

$$V_{PRO}$$

$$\cong V_{63\%} \cdot \left[\ln \left(\frac{1}{FR} \right) \right]^{\frac{1}{\beta_{RVS}}} \cdot \left(\frac{1}{RR \cdot t_{PRO}} \right)^{\frac{1}{n}} \cdot \left(\frac{1}{n+1} \right)^{\frac{1}{n}}$$

$$(16)$$

Fig. 9 shows the extracted dependence of $V_{\rm DIS}$ versus $t_{\rm DIS}$ and $V_{\rm PRO}$ versus $t_{\rm PRO}$ at 1 ppm FR by using both the CVS and RVS prediction methods. The RVS method yields prediction results equivalent to those from the time-consuming CVS method. Equations (15) and (16) can also be used to provide quantitative design guidelines of the $V_{63\%}$ and $\beta_{\rm RVS}$ at RVS, for meeting the desired SET speed–disturb criteria. One can show that large n and $\beta_{\rm RVS}$ (i.e., steep voltage acceleration and tight $V_{\rm SET}$ distribution) are desirable to increase the disturb immunity, i.e., increase the $V_{\rm DIS}/V_{\rm PRO}$ ratio, when FR is assumed to be small. For $V_{\rm DIS} > 0.5$ V and $V_{\rm PRO} < 3$ V at 1 ppm FR, $t_{\rm DIS} = 1$ s, and $t_{\rm PRO} = 1$ μ s. Fig. 10 presents

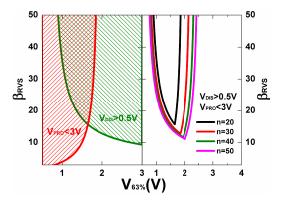


Fig. 10. (Left) Projected design space of $V_{63\%}$ and β_{RVS} for $V_{DIS} > 0.5$ V and $V_{PRO} < 3$ V at 1 ppm FR, $t_{PRO} = 1~\mu s$, and $t_{DIS} = 1$ s. A fixed n of 20 and RR of 1 V/s are assumed. (Right) Projected design space versus various n values.

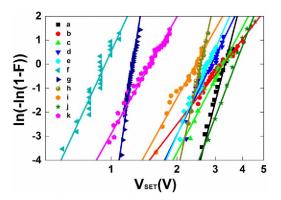


Fig. 11. V_{SET} distributions of various RRAM devices listed in Table I.

TABLE I $V_{63\%} \ {\rm AND} \ \beta_{\rm RVS} \ {\rm Extracted} \ {\rm from} \ {\rm Various} \ {\rm RRAM} \ {\rm Devices}$

	Material	V _{63%}	β _{RVS}	Reference
а	Cu/ZrO ₂ :Cu/Pt	3.32	15.41	M. Liu, EDL, 2008
b	Ru/Ta ₂ O ₅ /TiO ₂ /Ru/Ti	3.26	5.13	M. Terai, IEDM,2009
С	Ru/Ta ₂ O ₅ /TiO ₂ /Ru	3.26	7.54	
d	Ru/Ta ₂ O ₅ /TiO ₂ /Pt	2.88	8.08	
e	Pt/Ta ₂ O ₅ /TiO ₂ /Pt	2.79	8.91	M. Terai, IRPS, 2009
f	TiN/Ti/HfO₂/TiN	0.94	8.56	Y-S Chen, VLSI-TSA, 2009
g	TiN/Cu _x O/Cu	1.26	27.23	P. Zhou, IMW, 2009
h	NiSi/HfSiON/SiO _x /Si	2.57	18.24	N. Raghavan, EDL, 2012 (n=24.8, RR=12mV/s)
i	TaN/HfLaO/Pt	2.44	7.06	L. Chen, EDL, 2010
j	Ru/TaSiO/Cu	3.71	10.33	M. Tada, EDL, 2011
k	Ru/Y ₂ O ₃ /TaN	1.51	7.04	T-M Pan, ECS ,2011
I	Ti/TiO₂/Pt	0.79	15	This work, RR=0.1V/s
m	Ni/HfO₂/Si	6.5	10.5	

the available design space of $V_{63\%}$, β_{RVS} , and n. Typically, $\beta_{RVS} > 20$ and n > 20 are required to meet the desired specifications.

VI. CURRENT STATUS OF SET SPEED-DISTURB DILEMMA

In contrast to the lack of statistical data on the $t_{\rm SET}$ distribution, the cycling variation in RRAM devices is often tested by the dc voltage sweep in the literature, as shown in Fig. 11 and Table I. These dc cycling data are directly related to the RVS method. Therefore, the RVS method developed in this paper is applicable to the evaluation of the current

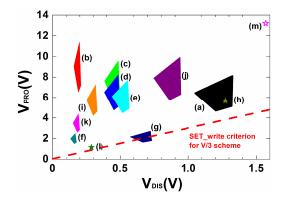


Fig. 12. Summary of the predicted V_{PRO} and V_{DIS} at 1 ppm FR, $t_{PRO}=1~\mu s$, and $t_{DIS}=1~s$ using RVS data reported in the literature from different RRAM devices. Detailed device characteristics are listed in Table I.

status of the SET speed-disturb dilemma of RRAM devices. These measurement data in Fig. 11 comply with the Weibull distribution, which is consistent with (11). The extracted $V_{63\%}$ and β_{RVS} values of these devices are used to predict the V_{PRO} and V_{DIS} at 1 ppm FR. Because the values of RR and n are not often reported in the literature, a reasonable range of RR and n is assumed. RR is assumed to be 0.1-10 V/s, which is a typical range used in semiconductor parameter analyzers. n is assumed to be 20–50 according to the V-trelationship in Fig. 5. Fig. 12 shows the predicted V_{PRO} and $V_{\rm DIS}$ of various RRAM devices. Most data show a large program voltage and low disturb immunity because of the poor extracted β_{RVS} < 20. The SET-write disturb criteria of the V/3 scheme (i.e., $V_{DIS}/V_{PRO} > 1/3$) in the crossbar RRAM is particularly difficult to satisfy. Improving the design space of the SET speed-disturb dilemma requires continuing research on the improved n factor and β_{RVS} .

VII. CONCLUSION

The statistical cell-based percolation model examined in this paper provides a thorough explanation of the stochastic nature and voltage dependence of $t_{\rm SET}$ distribution. Extracting the distribution characteristics ($t_{63\%}$ and β) and voltage acceleration factor n from rapid RVS tests is possible. The proposed RVS method reduces the analysis time and cost and yields equivalent results in predicting the SET speed—disturb properties, as compared to the conventional CVS method. The RVS method also enables evaluating the design space of satisfactory speed—disturb properties. Finally, by taking advantage of the rich RVS data available in the literature, this paper presented a discussion on the current status of the SET speed—disturb dilemma, which would probably continue to pose challenges in implementing high-density RRAM arrays in the future.

REFERENCES

- R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, 2009.
- [2] Y. C. Chen, C. F. Chen, C. T. Chen, J. Y. Yu, S. Wu, S. L. Lung, R. Liu, and C. Y. Lu, "An access-transistor-free (0T/IR) non-volatile resistance random access memory (RRAM) using a novel threshold switching, self-rectifying chalcogenide device," in *IEDM Tech. Dig.*, 2003, pp. 905–908.

- [3] S. Menzel, M. Waters, A. Marchewka, U. Böttger, R. Dittmann, and R. Waser, "Origin of the ultra-nonlinear switching kinetics in oxide-based resistive switches," *Adv. Funct. Mater.*, vol. 21, no. 23, pp. 4487–4492, Dec. 2011.
- [4] S. Yu, Y. Wu, and H.-S. P. Wong, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory," Appl. Phys. Lett., vol. 98, no. 10, pp. 103–514, Mar. 2011.
- [5] W. C. Luo, J. C. Liu, H. T. Feng, Y. C. Lin, J. J. Huang, K. L. Lin, and T. H. Hou, "RRAM SET speed-disturb dilemma and rapid statistical prediction methodology," in *IEDM Tech. Dig.*, 2012, pp. 215–218.
 [6] L. Zhang, R. Huang, Y. Y. Hsu, F. T. Chen, H. Y. Lee, Y. S. Chen,
- [6] L. Zhang, R. Huang, Y. Y. Hsu, F. T. Chen, H. Y. Lee, Y. S. Chen, W. S. Chen, P. Y. Gu, W. H. Liu, S. M. Wang, C. H. Tsai, M. J. Tsai, and P. S. Chen, "Statistical analysis of retention behavior and lifetime prediction of HfO_x-based RRAM," in *Proc. Int. Rel. Phys. Symp.*, 2011, pp. 847–851.
- [7] W. C. Luo, K. L. Lin, J. J. Huang, C. L. Lee, and T. H. Hou, "Rapid prediction of RRAM RESET-state disturb by ramped voltage stress," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 597–599, Apr. 2012.
- [8] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D. W. Kim, C. U. Jung, S. Seo, M. J. Lee, and T. W. Noh, "Random circuit breaker network model for unipolar resistance switching," *Adv. Mater.*, vol. 20, no. 6, pp. 1154–1159, Mar. 2008.
- [9] S. Yu, X. Guan, and H.-S. P. Wong, "On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization," in *IEDM Tech. Dig.*, 2011, pp. 413–416.
- [10] S. Long, C. Cagli, J. Buchley, Q. Liu, H. Lv, X. Lian, E. Miranda, D. Jimenez, M. Liu, and J. Suñé, "Set voltage statistics in unipolar HfO₂based RRAM," in *Proc. Solid State Devices Mater.*, 2012, pp. 636–637.
- [11] J. Sune, "New physics-based analytic approach to the thin-oxide breakdown statistics," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 296–298, Jun. 2001.
- [12] J. J. Huang, C. W. Kuo, W. C. Chang, and T. H. Hou, "Transition of stable rectification to resistive-switching in Ti/TiO₂/Pt oxide diode," *Appl. Phys. Lett.*, vol. 96, no. 26, pp. 262901-1–262901-3, 2010.
- [13] K. L. Lin, T. H. Hou, J. Shieh, J. H. Lin, C. T. Chou, and Y. J. Lee, "Electrode dependence of filament formation in HfO2 resistive-switching memory," *J. Appl. Phys.*, vol. 109, no. 8, pp. 084104-1–084104-7, 2011.
- [14] E. Y. Wu and J. Suñé, "Power-law voltage acceleration: A key element for ultra-thin gate oxide reliability," *Microelectron. Rel.*, vol. 45, no. 12, pp. 1809–1834, 2005.
- [15] A. Conde, C. Martínez, D. Jiménez, E. Miranda, J. M. Rafí, F. Campabadal, and J. Suñé, "Modeling the breakdown statistics of Al₂O₃/HfO₂ nanolaminates grown by atomic-layer-deposition," *Solid State Electron.*, vol. 71, pp. 48–52, May 2012.
- [16] E. Y. Wu and R.-P. Vollertsen, "On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination. Part I: Theory, methodology, experimental techniques," *IEEE Trans. Electron. Devices*, vol. 49, no. 12, pp. 2131–2140, Dec. 2002.
- [17] A. Kerber, L. Pantisano, A. Veloso, G. Groeseneken, and M. Kerber, "Reliability screening of high-k dielectrics based on voltage ramp stress," *Microelectron. Rel.*, vol. 47, nos. 4–5, pp. 513–517, May 2007.



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