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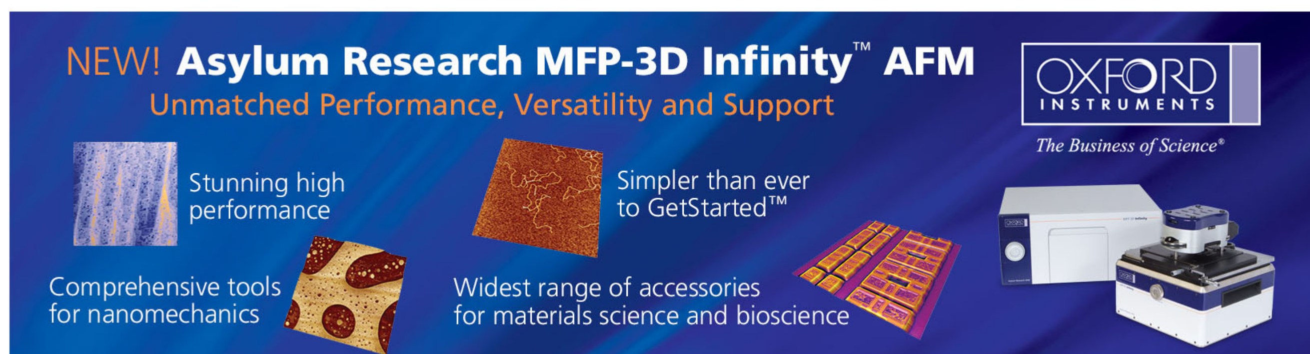

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APPLIED PHYSICS LETTERS **103**, 153102 (2013)

Low-voltage high-speed programming/erasing floating-gate memory device with gate-all-around polycrystalline silicon nanowire

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A gate-all-around polycrystalline silicon nanowire (NW) floating-gate (FG) memory device was fabricated and characterized in this work. The cross-section of the NW channels was intentionally made to be triangular in shape in order to study the effects of the corners on the device operation. Our results indicate that the channel corners are effective in lowering the programming and erasing (P/E) operation voltages. As compared with the charge-trapping type devices, a larger memory window is obtained with the FG scheme under low-voltage P/E conditions. A model considering the nature of the charge storage medium is proposed to explain the above findings. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4824817]

The invention of the floating-gate (FG) flash memory[1] sparked a revolution in microelectronics and continues to be one of the most prevailing non-volatile memories, which is widely used in memory products, such as Universal Serial Bus (USB) sticks, cell phones, solid-state drives, etc.[2,3] Although a huge commercial success, nowadays, the conventional planar FG flash memory has faced severe challenges in future scaling due to concerns of reliability as well as practical physical limitations.[3] For example, for NOR-type devices, usually channel hot-electron injection is employed to program the devices. For efficient programming, the drain-to-source bias voltage must be greater than 3.2 V so that an amount of channel electrons can gain sufficiently high energy to surmount the barrier at tunnel oxide/Si channel interface. This hinders the downscaling of NOR devices below 45 nm.[4] To solve the above issue, alternative *Fowler-Nordheim* (F-N) tunneling was proposed to program the devices, but the program/erasing (P/E) voltages would be high ($>$18 V).[5] In this work, we explore the feasibility of using gate-all-around (GAA) polycrystalline silicon (poly-Si) nanowire (NW) channels with an aim to lowering the P/E voltages. The deposition of poly-Si is mature and the capability for construction of three-dimensional multi-layer memory cells[6] has been demonstrated which can effectively increase the storage density of the chip. The combination of NW channel and GAA configuration[7,8] is attractive due to the advantages of enhanced gate controllability and field strength at the channel surface. Furthermore, since the corners of the NW are expected to enhance the F-N tunneling,[9] the P/E voltages are expected to be further reduced. This feature has indeed been demonstrated for charge trapping (CT) memory devices like silicon-oxide-nitride-oxide-silicon (SONOS).[10] In this work, both FG and SONOS devices built with poly-Si NWs were fabricated, characterized, and compared.

The schematic fabrication processes for the proposed device are shown in Fig. 1. First, a stack consisting of 80 nm (bottom) silicon nitride/ 150 nm (top) tetraethylorthosilicate (TEOS) oxide was deposited sequentially by low pressure chemical vapor deposition (LPCVD) on Si substrate capped with a thermal oxide [Fig. 1(a)]. After lithography, the top TEOS oxide layer was patterned by dry etching [Fig. 1(b)]. A 100-nm-thick amorphous-Si layer was then deposited by LPCVD [Fig. 1(c)] and subsequently annealed at 600 °C in N_2 ambient for 24 h to form poly-Si. Next, a phosphorous ion implantation (25 keV, 2×10^{15} cm^{-2}) was performed on the wafer. Note that the implant energy was kept low so that most implanted dopants were located near the top surface of the Si layer. The measure prevents the NW channels formed in the next step from being intentionally doped. The source/-drain (S/D) pad regions were defined simultaneously with the NW channels abutting the sidewalls of the oxide structure in a reactive plasma etching step after the S/D photoresist patterns were formed [Fig. 1(d)]. Note that the cross section of the resultant NW channels is triangular in shape, a consequence of the sidewall spacer etching. After the S/D activation process, the oxide and silicon nitride around the nanowire channels were selectively removed by wet etching [Fig. 1(e)], leaving the NW channels hanging between the source and drain studs. Then, 11 nm TEOS oxide, 25 nm n^+ poly-Si, 20 nm TEOS oxide, and 150 nm n^+ poly-Si were sequentially deposited and serve as the tunnel oxide, FG, blocking oxide, and control gate (CG), respectively. Afterwards, the control gate was defined [Fig. 1(f)]. Finally, a standard metallization was performed to complete the device fabrication. GAA NW SONOS memory devices with the same NW channels were fabricated simultaneously to benchmark the characteristics of the FG ones. For the SONOS devices, the tunnel oxide, trapping layer, and blocking oxide are 3 nm oxide, 7 nm silicon nitride, and 12 nm oxide, respectively. Figure 1(g) shows the cross-sectional

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TEM image of a NW channel of the fabricated GAA NW FG memory device. The lengths of three sides of NW channel are about 17 nm, 17 nm, and 30 nm, respectively, so the total edge length of a channel is roughly 64 nm.

For simplicity, the threshold voltage (V_{th}) is defined as the gate voltage at a drain current of 10^{-9} A in the transfer curve. Figure 2 shows the fresh transfer characteristics of a GAA NW FG memory device at V_d of 0.1 and 1 V. Despite the pretty thick stack (block oxide/FG/tunnel oxide) of 56 nm between the control gate and the channel, this device shows steep subthreshold swing (S.S.) (112 mV/dec) at V_d of 0.1 V, negligible drain induced barrier lower (DIBL) effect and high I_{on}/I_{off} current ratio ($\sim 10^8$). The steep S.S. and low DIBL effect are ascribed to the enhanced electric field on the surface of the slim NW channels and GAA configuration.

For P/E operation, a high voltage is applied to the gate while both source and drain are grounded. Figures 3(a) and 3(b) show the programming and erasing characteristics, respectively, for both GAA NW FG and SONOS memory devices under low programming (8∼10 V) and erasing

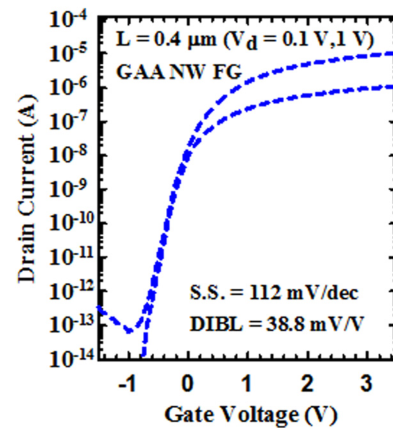

FIG. 2. Transfer characteristics of a GAA NW FG device.

(−6∼−8 V) bias conditions. For conventional FG devices, the magnitude of the P/E voltages is typically larger than 18 V.[5] For the GAA NW FG memory devices, although the P/E voltages are low, high P/E efficiencies are achievable. The V_{th}

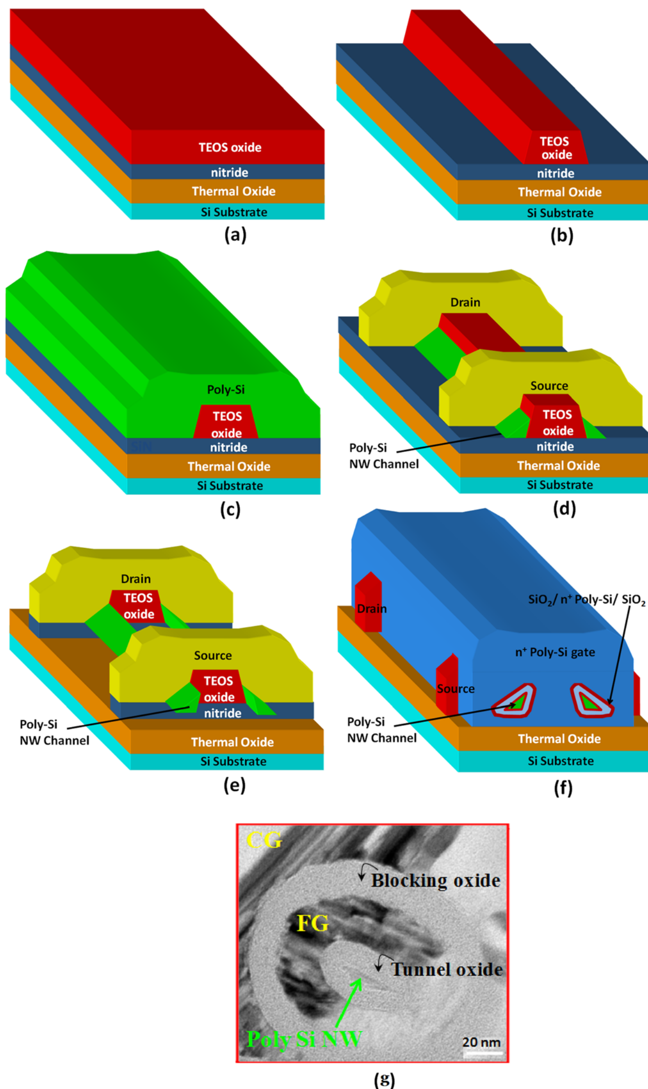

FIG. 1. (a)–(f) Major fabrication process steps of the GAA NW FG memory device. (g) Cross-sectional TEM image of a NW channel of the fabricated GAA NW FG memory device.

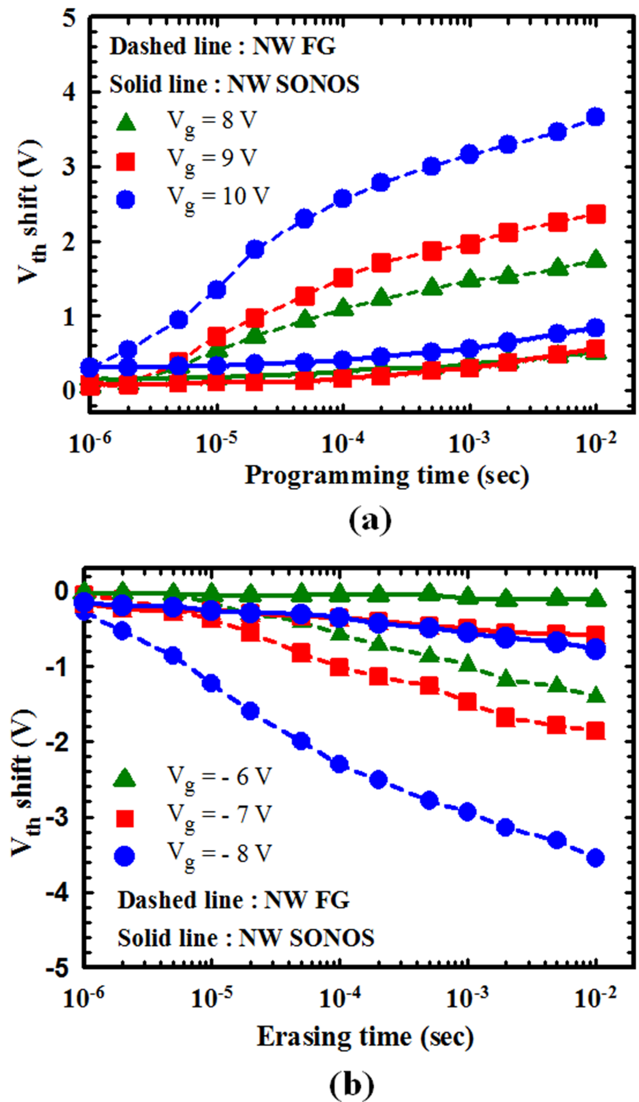

FIG. 3. Comparison of (a) programming characteristics, (b) erasing characteristics of GAA NW FG (dashed line), and GAA NW SONOS (solid line) memory devices with same NW channel dimensions.

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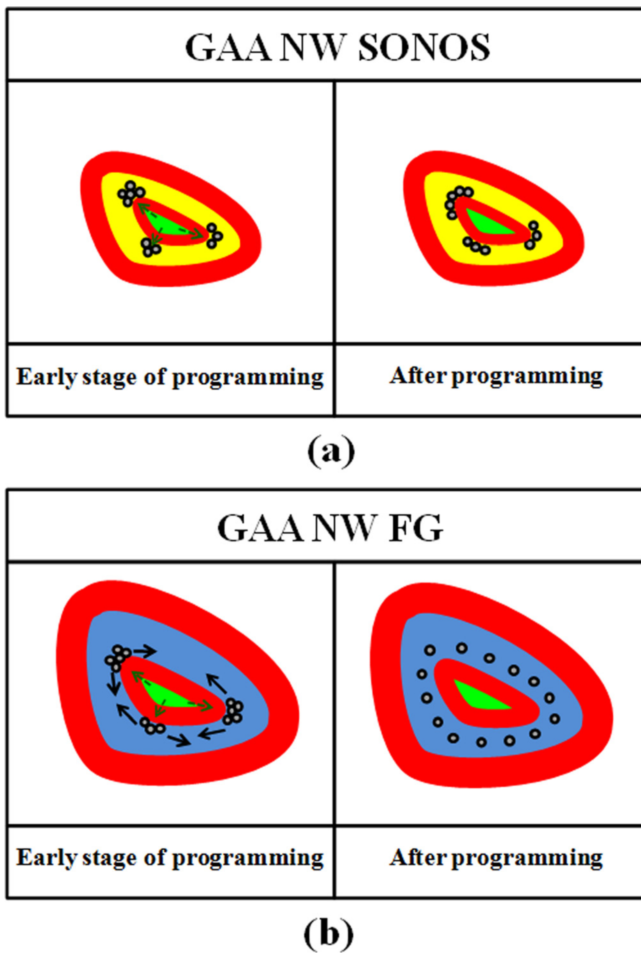

FIG. 4. Schematic illustrations of electron trapping events during programming process for (a) the SONOS devices. The injection electrons are trapped in discrete sites in the nitride and impede further injection of electrons from the channel. (b) The FG memory devices. The injection electrons redistribute themselves in the n^+ poly-Si FG and thus would not significantly affect the subsequent injection of electrons from the channel.

shifts (ΔV_{th}) of GAA NW FG memory device is 3 V at the programming voltage of +10 V (programming time of 10^{-3} s) and at the erasing voltage of −8 V (erasing time of 10^{-3} s). In contrast, the SONOS devices only achieve around 0.5 V shift under the same P/E operations. The high efficiencies under the low P/E voltages for the FG split are ascribed to the strong electric field across the tunnel oxide around the sharp corners of NW channels. Nonetheless, despite the same NW channels, the above benefits are realized only on the FG devices, but not observed in the SONOS split. The different outcomes of the two splits of devices are attributed to the natures of the charge storage medium, *e.g.*, n^+ poly-Si and silicon nitride. The strength of the electric field around the NW corners is much stronger than that around the remaining regions of the NW channel, and thus a greatly enhanced injection current density is expected to occur around the corners. As the schematic illustrations of the SONOS device shown in Fig. 4(a), the electrons will first tunnel into the silicon nitride CT layer through the corners of the NW channel. Since most of the trapping sites in the nitride are discrete, the spreading-out and re-distribution of the stored charges are limited. As a consequence, trapping of electrons in the CT layer is limited in the corner regions. In contrast, as shown in Fig. 4(b), the use of an n^+ poly-Si as floating gate can eliminate this concern by effectively redistributing the stored electrons and thus the carrier injection in and out through the channel corners can be sustained during the P/E operations.

Figure 5 shows the electric field distributions of poly-Si NW devices along the XY direction indicated in the figures simulated by the Sentaurus TCAD simulator[11] at the programming voltage of +10 V with times of 10^{-6} s and 10^{-2} s. The electric field profile in the NW device suggests that, at the beginning of the programming, the maximum electric field occurs at the two sharp corners of NW channels. Owing to the low programming voltage and localization of the

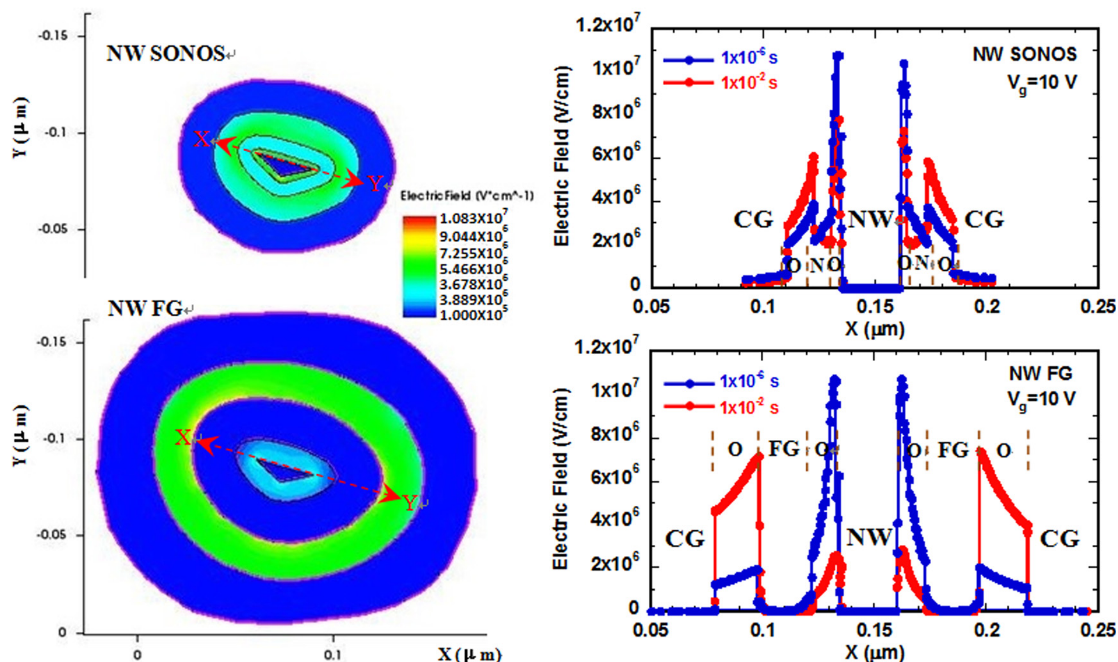

FIG. 5. The simulated electric field distributions in the n^+ poly-Si FG and nitride CT layers by Sentaurus TCAD simulator with the programming voltage of 10 V at programming times of 10^{-6} and 10^{-2} s.

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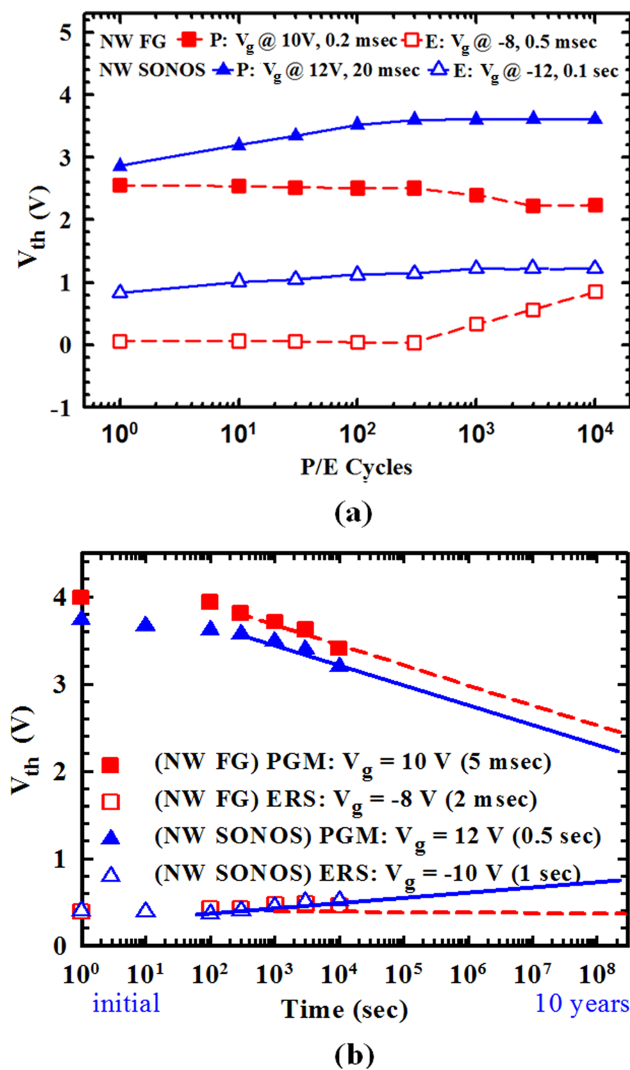

FIG. 6. Comparison of (a) Endurance characteristics and (b) retention characteristics of GAA NW FG (dashed line) and GAA NW SONOS (solid line) memory devices.

trapping events, the electric filed at the tunneling oxide/NW interface is still higher than that at nitride CT/blocking oxide interface, an indication of slow programming process. In contrast, owing to the redistribution of the trapped charges in the n^+ poly-Si FG, location of the maximum electric field in the NW FG device shifts from the tunneling oxide/NW interface at 10^{-6} s to the blocking oxide/FG interface at 10^{-2} s.

The endurance characteristics of FG and SONOS devices are shown in Fig. 6(a). Note that, in order to acquire comparable window sizes between the two splits, the P/E conditions executed on the SONOS devices are with higher stress voltages and longer times. It is seen in this figure that the window of the FG device begins to shrink after 10^3 P/E cycles. This is owing to the cumulative damage resulted in the tunnel oxide around the corners after a number of P/E cycles. This concern can be alleviated by promoting the quality of the tunnel oxide (for example, nitridation.[12]). Figure 6(b) shows the retention characteristics of the FG and SONOS devices. Obviously, the FG device shows better data retention than the SONOS counterpart due to the thicker tunnel oxide. Memory window of 2 V can be retained after ten years from the extrapolation.

In summary, this paper studies the characteristics of FG memory devices built on poly-Si NW channels with GAA configuration. The FG devices exhibit excellent electrical characteristics owing to the superior gate controllability of GAA configuration on the NW channels. The triangular-shaped poly-Si NW channels are effective in promoting the injection efficiency of electrons from the corners of the channel. As compared with the SONOS counterparts, the GAA NW FG devices could further lower the P/E operation voltage. This is attributed to the use of the n^+ poly-Si FG which allows redistribution of the injected electrons.

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