Design Model and Guideline for n-Well Guard Ring in Epitaxial CMOS

Chih-Yao Huang, *Student Member, IEEE*, and Ming-Jer Chen, *Member, IEEE*

***Abstract*—This work reports the development of design model for n-well guard rings in a CMOS process utilizing a low-doped epitaxial layer on a highly doped substrate. The validity of the model has been judged by a wide range of experimental data measured from the fabricated n-well guard ring structures with guard ring width as parameter. From the model developed, guideline has been drawn to minimize the guard ring width while critically suppressing the amount of electrons escaping from guard ring.**

I. Introduction

MINORITY-carrier well-type guard ring has long been employed as one of the layout techniques in order to overcome the latch-up in CMOS circuits [1]. Such guard ring surrounds the parasitic emitter region to pre-collect the minority carriers injected into the substrate, and thus acts as the role of the pseudo collector. Especially for the CMOS process utilizing a low-doped epitaxial layer on a highly doped substrate, the potential of the minority-carrier well-type guard rings can be fully realized [2]. Recently, a study of this guard ring efficiency by solving the two-dimensional carrier diffusion equation has been reported [3]. Further two-dimensional numerical simulations of an n-well guard ring on p-epi/p^+-substrate have revealed that the minority-carrier current escaping from the guard ring is contributed by two components: 1) the minority carriers injected into a layer between the upper collecting plate and the bottom high/low junction reflecting plate; and 2) the minority carriers penetrating the high/low junction and spreading in the bulk [4]. The corresponding escape current components have been formulated analytically and have been verified by two-dimensional numerical simulations as well as by the experimental data [5]. However, the modeling of other currents such as that collected by guard ring itself, which is also of concern for practical design of guard ring, has not been established in [4], [5]. In this paper we present the work of establishing experimentally the complete model expressions for n-well guard rings in a CMOS process utilizing a low-doped epitaxial layer on a highly doped substrate. Design guideline will be drawn from the model in order to minimize the guard ring width while the escape electron current is suppressed below the specified critical value for triggering the latch-up.

Manuscript received February 16, 1994; revised May 9, 1994. The review of this paper was arranged by Associate Editor K. Tada. This work was supported by the National Science Council under Contract NSC 82-0404-E-009-232/246.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsin-Chu 300, Taiwan, Republic of China.

IEEE Log Number 9404376.

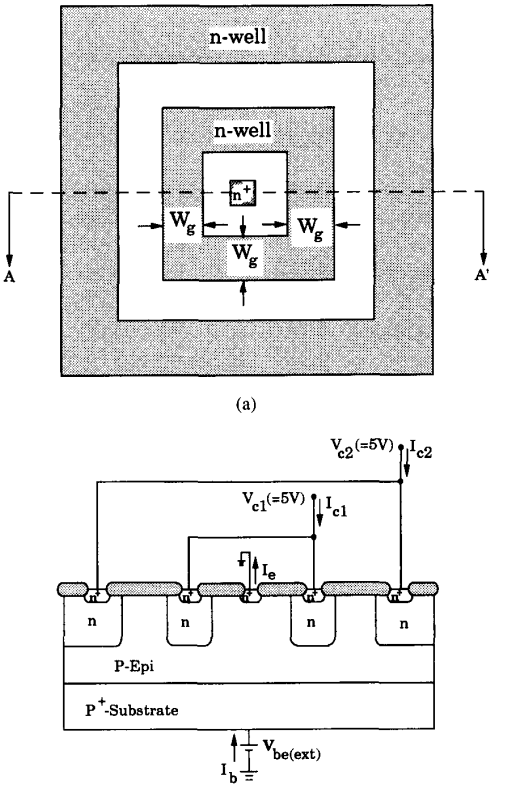


Fig. 1. (a) The schematic top view and (b) cross section along the line AA′ of the n-well guard ring structure on the p-epi/p^+-substrate where n^+ emitter and inner and outer n-well collectors are shown.

II. Experiment

Fig. 1 shows schematically an n-well guard ring structure on the p-epi/p^+-substrate. The inner guard ring surrounds the parasitic n^+ emitter and the outer guard ring surrounds the inner guard ring. The inner guard ring acts as a pseudo collector and the outer guard ring considerably represents the internal circuitry. As the parasitic n^+ emitter is forward biased, the electrons are injected into the substrate, some of which are pre-collected by the inner guard ring and constitute the collector current I_{c1}. The electrons escaping from the inner guard ring, as collected by the outer guard ring, contribute to the collector current I_{c2}. The rest of the electrons recombines with the holes in the substrate and contributes in part to the base current I_b. To demonstrate the development of the model,

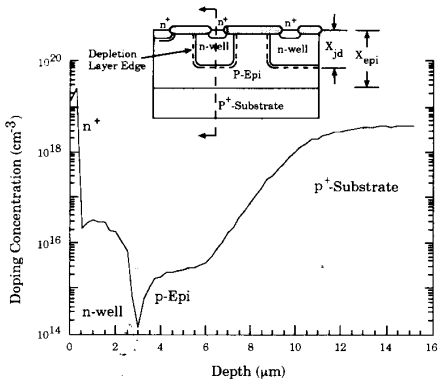


Fig. 2. The measured doping profile along the depth direction as illustrated in the upper part of the figure.

it is needed to measure the data such as the currents I_{c1}, I_{c2}, and I_b as functions of both the forward bias $V_{\rm be}$ and the inner guard ring width W_g.

The n-well guard ring structures with the inner guard ring width as parameter were fabricated by a 1.0 μm n-well standard CMOS process. The starting material was a 12 μm, 12 Ω•cm low-doped p-type epitaxial layer on a highly doped p-type substrate. The post-process vertical doping profile measured by using an auto-spreading resistance probe is shown in Fig. 2. The four different inner guard ring widths of 6, 20, 40, and 60 μm have been considered. The other structure parameters are fixed: the distance between the n^+ emitter and the inner guard ring is 7.5 μm; and the distance between the inner guard ring and the outer collector is 10 μm. Fig. 3 depicts the photograph of the patterns of these structures. The layouts from the left to the right represent the 6, 40, 60, and 20 μm wide guard ring structures. Note that the 60 μm layout case has four contact rings on the inner guard ring specially designed to monitor the three-dimensional potential distribution, which is not addressed in the present study; and any combination of these four contact rings does not at all affect the measurement results reported here. To establish the experimental data, the two n-well guard rings are biased at 5 V; the n^+ emitter is grounded; and the external base-to-emitter bias $V_{\rm be(ext)}$ ranges widely from 0 to 3 V. The corresponding measurement results are shown in Fig. 4 and 5.

From the Gummel plot in Fig. 4 we can observe that the measured collector current I_{c1} and base current I_b are considerably independent of the inner guard ring width. However, Fig. 5 exhibits that the escape electron collection current I_{c2} strongly depends on the inner guard ring width, in agreement with those reported in [4], [5]. From Fig. 4 and 5 it can also be seen that at high-level injection as the $V_{\rm be(ext)}$ bias increases both I_{c1} and I_b tend to saturate while the I_{c2} gradually increases. The measured maximum emitter current I_c, occurring at $V_{\rm be(ext)} = 3$ V, is about 93, 100, 96, and 67 mA corresponding to $W_g = 6$, 20, 40, and 60 μm, respectively.

III. Modeling

To model the above experimental data with considerable accuracy, several published explicit expressions [4]–[7] for the currents I_{c1}, I_{c2}, and I_b as functions of both the forward bias $V_{\rm be(ext)}$ and the inner guard ring width W_g have been considered. According to the work [4], [5], the inner guard ring collection current I_{c1} can be interpreted by the electron collection at the sidewall of the inner guard ring. Therefore, the model expression for the collector current of a lateral n-p-n bipolar transistor as cited in [6] has been employed for I_{c1}:

$$I_{c1} = \left(\sqrt{a_1 + a_2 \exp\left(\frac{qV_{\rm be}}{KT}\right)} - a_3\right) \tag{1}$$

where a_1, a_2, and a_3 are the coefficients to be determined empirically. Note that the expression (1) has taken into account both the low- and high-level injection conditions. The base current I_b follows the empirical formula [7]:

$$I_b = I_{c1} \Big/ \left(\frac{\beta_{\max}}{(1 + I_{c1}/I_k)}\right) \tag{2}$$

where $\beta_{\max}$ is the maximum current gain; and I_k is the knee current of I_{c1}, which is the corner point for current gain roll-off at high current level as usually defined in the Gummel–Poon model [7]. Note that the $V_{\rm be}$ in (1) is the intrinsic forward bias of the base-to-emitter junction, i.e., $V_{\rm be(ext)} = V_{\rm be} + (I_{c1} + I_{c2} + I_b)R_e + I_bR_b$, where R_e is the emitter series resistance and R_b is the lumped base resistance. Initially the values of the parameters such as $\beta_{\max}$ and a_2 can be adequately extracted at the low-level injection condition and the others can be adjusted such as to match the I-V data up to $V_{\rm be(ext)} = 3$ V. The resulting fitted coefficient values are: $R_e = 0.3\ \ \Omega$, $R_b = 60\ \ \Omega$, $\beta_{\max} = 150$, $I_k = 0.9$ mA, $a_1 = 3.73 \times 10^{-8}\text{A}^2$, $a_2 = 7.88\times10^{-21}$ A^2, and $a_3 = 1.93 \times 10^{-4}$ A. The corresponding calculated results using (1) and (2) are demonstrated in Fig. 4. From Fig. 4 it can be observed that the calculated results agree closely with the experimental data. Both (1) and (2) are essential for determination of the intrinsic forward bias $V_{\rm be}$ in order to evaluate the escape electron collection current I_{c2} as demonstrated below.

According to the work [4], [5], the escape electron collection current I_{c2} is made up of two components: 1) the component $I_{\rm epi}$ due to electrons injected into the quasi-neutral epitaxial layer between the upper collecting plate and the bottom reflecting plate; and 2) the component $I_{\rm sub}$ due to electrons penetrating the high/low junction and spreading in the bulk. These two components can be modeled explicitly by [5]:

$$I_{\rm epi} = I_{\rm eff}1(V_{\rm be}) \exp\left(-\frac{W_g}{L_{\rm eff1}}\right) \tag{3}$$

and

$$I_{\rm sub} = I_{\rm eff2}(V_{\rm be}) \exp\left(-\frac{W_g}{L_{\rm eff2}}\right) \tag{4}$$

where both $I_{\rm eff1}(V_{\rm be})$ and $I_{\rm eff2}(V_{\rm be})$ are the pre-exponential factors depending on the intrinsic base-to-emitter bias; and $L_{\rm eff1}(= 2(X_{\rm epi} - X_{\rm jd})/\pi)$ and $L_{\rm eff2}$ are two coefficients to be determined. $X_{\rm epi}$ represents the effective epitaxial layer thickness and $X_{\rm jd}$ represents the distance from the surface to the bottom junction depletion layer edge as depicted in Fig. 2. Since there is a considerable thickness for the quasi-neutral epitaxial layer as can be observed in Fig. 2, we have

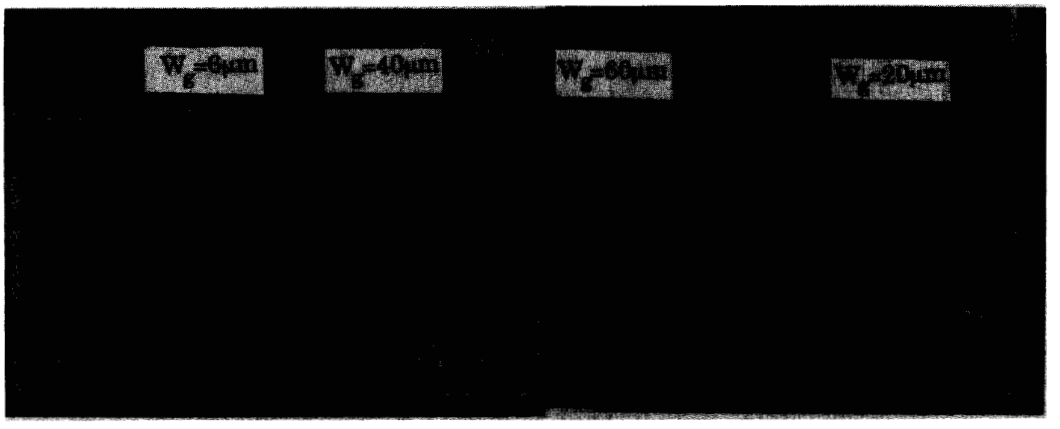


Fig. 3. The photomicrograph of the guard ring structure layout.

$I_{\rm epi} > I_{\rm sub}$ for small W_g as explained experimentally and theoretically in [5], i.e., for a narrow $W_g(< 30\ \mu\text{m})$ the $I_{\rm epi}$ component is greater than the $I_{\rm sub}$ component by several orders of magnitude while as the W_g becomes wider the $I_{\rm epi}$ is reduced more rapidly due to the strong width dependence of $I_{\rm epi}$. For larger $W_g(> 30\ \mu\text{m})$ the $I_{\rm sub}$ becomes dominant. As a result, the whole I_{c2} versus W_g relationship is the superposition of the $I_{\rm epi}$ and $I_{\rm sub}$ components; that is, the $I_{\rm sub}$ parameters can be extracted easily in the range of $W_g > 30$ μm and the $I_{\rm epi}$ parameters can also be extracted in the range of $W_g < 30\ \mu$m. Therefore, the values of two parameters $L_{\rm eff1}$ and $L_{\rm eff2}$ can be separated from the single I_{c2} versus W_g relationship. The validity of this parameter extraction process will be judged later. Fig. 6 shows the measured outer guard ring collection current I_{c2} versus the inner guard ring width W_g with the external forward bias $V_{\rm be(ext)}$ as parameter. By fitting the measured results in Fig. 6 utilizing (3) and (4), we obtain $L_{\rm eff1} = 3.118\ \mu$m and $L_{\rm eff2} = 8.474\ \mu$m. The simultaneously extracted $I_{\rm eff1}$ and $I_{\rm eff2}$ values as functions of the $V_{\rm be(ext)}$ are demonstrated in Fig. 7. Note that the extracted value of $L_{\rm eff1} = 3.118\ \mu$m agrees closely with the calculated one of $L_{\rm eff1} = 3.5\ \mu$m from $L_{\rm eff1} = 2(X_{\rm epi} - X_{\rm jd})/\pi$ [4], [5]. However, the extracted value of $L_{\rm eff2} = 8.474\ \mu$m appears to be considerably different from $L_{\rm eff2} = 33\ \mu$m reported in [5]. This inconsistency can be satisfactorily interpreted by noting that there is a considerable thickness of the high/low junction transition region (see Fig. 2) and the $I_{\rm sub}$ component in the present work has recently been judged to flow laterally across the high-low junction transition region itself [8]. Further we have found that the $I_{\rm eff1}$ and $I_{\rm eff2}$ versus $V_{\rm be(ext)}$ curves in Fig. 7 can be satisfactorily reproduced by using the low- and high-level injection formulation [6]:

$$I_{\rm eff1}(V_{\rm be}) = \left(\sqrt{b_1 + b_2 \exp\left(\frac{qV_{\rm be}}{KT}\right)} - b_3\right) \tag{5}$$

$$I_{\rm eff2}(V_{\rm be}) = \left(\sqrt{c_1 + c_2 \exp\left(\frac{qV_{\rm be}}{KT}\right)} - c_3\right). \tag{6}$$

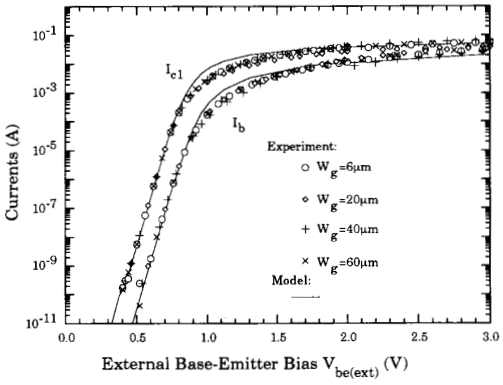


Fig. 4. The measured and calculated Gummel plots for test structures with four different guard ring widths.

The fitting parameter values of $b_1 = 8.465 \times 10^{-13}\text{A}^2$, $b_2 = 2.268 \times 10^{-28}\ \text{A}^2$, $b_3 = 9.2 \times 10^{-7}$ A, $c_1 = 3.733 \times 10^{-18}\ \text{A}^2$, $c_2 = 8.08_x\ 10^{-32}\ \text{A}^2$, and $c_3 = 1.93 \times 10^{-9}$ A have led to good agreements as demonstrated in Fig. 7. Therefore for the epi CMOS process mentioned above, the escape electron collection current I_{c2} can be modeled quantitatively by

$$I_{c2} = \left[\left(\sqrt{b_1 + b_2 \exp\left(\frac{qV_{\rm be}}{KT}\right)} - b_3\right) \exp\left(-\frac{W_g}{3.118\ \ \mu\text{m}}\right)\right] + \left[\left(\sqrt{c_1 + c_2 \exp\left(\frac{qV_{\rm be}}{KT}\right)} - c_3\right) \exp\left(-\frac{W_g}{8.474\ \ \mu\text{m}}\right)\right]. \tag{7}$$

By substituting the above fitting parameter values into (7), the calculated results are shown in Fig. 5. It can be observed from Fig. 5 that the agreement with the experimental data for four different guard ring widths is very good. This supports the validity of the forward-mentioned parameter extraction process and thus the established analytical model expressions in combination with the empirical approach is useful for further applications as demonstrated below.

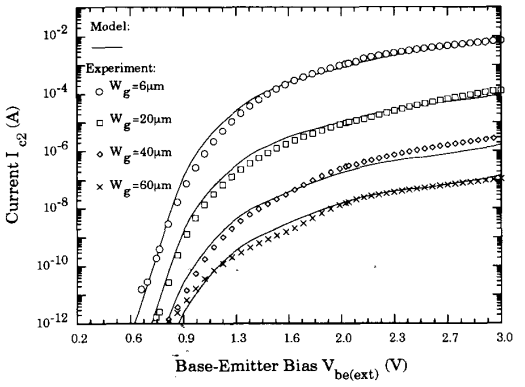


Fig. 5. The measured and calculated results of the escape currents I_{c2} versus external base-emitter bias $V_{\mathrm{be(ext)}}$ for four different guard ring widths.

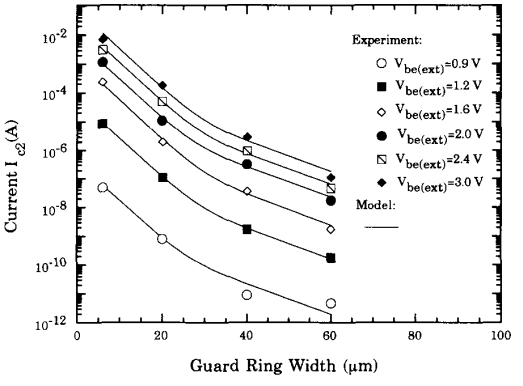


Fig. 6. The measured and calculated escape currents I_{c2} as function of guard ring width for six different $V_{\mathrm{be(ext)}}$ biases.

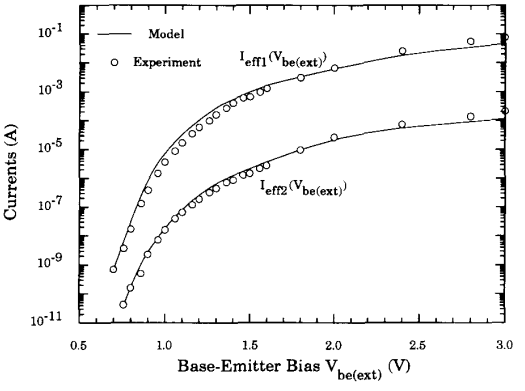


Fig. 7. The data of current factors I_{eff1} and I_{eff2} versus $V_{\mathrm{be(ext)}}$ extracted from Fig. 6. Also shown are the calculated results from (5) and (6).

IV. Design Guideline

Here we demonstrate the application of the above model expressions in order to establish the design guideline for n-well guard rings in a given epi CMOS process. One such guideline in terms of guard ring width versus external base-emitter bias with the specified escape collection current as

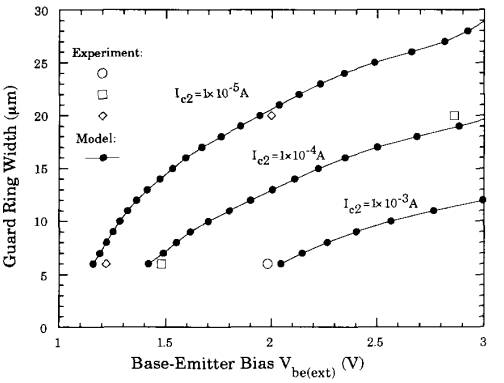


Fig. 8. The calculated guard ring width versus external base-emitter bias with the escape electron collection current as parameter. Some experimental data from Fig. 5 are also shown for comparison.

parameter is plotted in Fig. 8. This figure has been established by employing (7), as given the values of both the W_g and the specified I_{c2}, to find the corresponding value of the intrinsic bias V_{be}. Then the currents I_{c1} and I_b have been calculated using (1) and (2), respectively, in order to yield the associated resistance potential drops, and thus the corresponding external bias $V_{\mathrm{be(ext)}}$ has been obtained. Also shown in Fig. 8 are some experimental data from Fig. 5. From Fig. 8 it can be observed that the calculated results agree closely with the experimental data, which confirms the validity of the design guideline.

If we consider the I_{c2} value labeled in Fig. 8 as the critical current for triggering the latch-up, it can be drawn from Fig. 8 that as the critical current value for triggering the latch-up decreases, the n-well guard ring width needed for latch-up suppression must be increased. For example, latch-up free design with $W_g = 5$ μm can be obtained with the allowable external base-emitter bias of less than 2.0 V if the triggering current I_{c2} for the internal circuitry is 1 mA; however, if the triggering current I_{c2} is lowered for poor layout design in the internal circuitry, the corresponding external base-emitter bias should be respecified by a relatively small value. Note that based on the above design guideline, a 6 μm n-well guard ring width has yielded the results: $I_c \geq 100$ mA for $I_{c2} \cong 10$ mA, which meet the specification of $I_c \geq 100$ mA as usually considered as a measure of evaluating the immunity against the latch-up in the input/output pad of a CMOS chip. Therefore a 6 μm wide n-well guard ring based on the epi CMOS process as described above is enough to completely eliminate the latch-up due to the action of an n^+ emitter in the substrate.

Obviously, the above empirically based analytical escape current model is able to be extended appropriately to the cases of different structural parameters such as epitaxial layer thickness, well junction depth, and guard ring width, by simply recalculating the exponential terms in (7) without any further fitting process. Moreover, the other detailed experimental results [8] have exhibited that the escape current I_{c2} is essentially independent of not only the distance between the inner guard ring and the outer collector but also the distance between the n^+ emitter and the inner guard ring. Therefore

the our design guideline can offer the ability of accurately specifying both the triggering currents characterizing the latch-up susceptibility of the internal circuitry and the external forward bias value in order to design an appropriate n-well guard ring width.

V. Conclusion

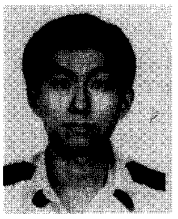
The complete model expressions concerning the design of n-well guard rings in a given epitaxial CMOS process have been established and have been judged experimentally. Design guideline has been drawn from the model and has been addressed. Based on our design guideline, not only the triggering currents characterizing the latch-up susceptibility of the internal circuitry but also the external forward bias applied have been specified in order to maintain a small value of n-well guard ring width.

Acknowledgment

The authors would like to thank Mr. Ping-Nan Tseng, Taiwan Semiconductor Manufacturing Company, for fabricating the our designed guard ring structures, and Mr. Jeng-Kuo Jeng, ERSO/ITRI, for doping profile measurement. The authors also would like to thank the reviewers for their helpful comments and suggestions.

References

[1] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Cures*. Boston: Kluwer, 1986.
[2] R. R. Troutman, "Epitaxial layer enhancement of N-well guard rings for CMOS circuits," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 438–440, Dec. 1983.
[3] M. J. Chen and C. Y. Wu, "A simplified computer analysis for N-well guard ring efficiency in CMOS circuits," *Solid-State Electron.*, vol. 30, pp. 879–882, Aug. 1987.
[4] M. J. Chen, C. Y. Huang, P. N. Tseng, N. S. Tsai, and C. Y. Wu, "Design model for minority-carrier well-type guard rings in CMOS circuits," *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 4.5.1–4.5.4, 1991.
[5] M. J. Chen, C. Y. Huang, and P. N. Tseng, "Design formulation for minority-carrier well-type guard rings in CMOS circuits," *IEE Proc.—G Circuits, Devices and Syst.*, vol. 140, pp. 182–186, June 1993.
[6] S. Chou, "An investigation of lateral transistors—D.C. characteristics," *Solid-State Electron.*, vol. 14, pp. 811–826, Sept. 1971.
[7] I. E. Getreu, *Modeling the Bipolar Transistor*. New York: Elsevier, chap. 2, 1984.
[8] C. Y. Huang and M. J. Chen, "Optimization of well-type guard rings in epi-CMOS," 1993 *Symp. on Semicond. Modeling and Simulation*, pp. 2.6–2.7, 1993.



Chih-Yao Huang (S'87) was born in Taiwan, Republic of China, on May 31, 1963. He received the B.S. degree in electrical engineering from the National Tsing-Hua University in 1985, and the M.S. degree in electronics engineering from the National Chiao-Tung University in 1987.

During 1987–1989 he served in the Chinese Air Force. From 1991 to 1993 he was a part-time Lecturer at the Institute of Electronics, National Chiao-Tung University. He is now working toward the Ph.D. degree at the same university. His research interest is in characterization and modeling of submicron VLSI devices and circuits concerning enhanced reliability.

Ming-Jer Chen (S'77–M'86) was born in Taiwan, Republic of China, on April 1, 1954. He received the B.S. degree (highest honors) from the National Cheng-Kung University in 1977, and the M.S. and Ph.D. degrees from the National Chiao-Tung University in 1979 and 1985, respectively. His doctoral dissertation covered the modeling and prediction of CMOS latch-up.

During 1979–1980, he worked for the Telecommunication Laboratories, Taiwan, where he was responsible for the design and implementation of a multiprocessor distributed system. From 1985 to 1986 he conducted postdoctoral research on CMOS latch-up at the National Chiao-Tung University. From 1986 to 1992, he was an Associate Professor at the same university, and in 1993 became a Professor. His present research interests include submicron device reliability, subthreshold CMOS circuits, and special BiCMOS structures. Since 1985 he served as a reviewer for international journals such as *IEEE Electron Device Letters*, *IEEE Transactions on Electron Devices*, *Solid-State Electronics*, and *Journal of the Chinese Institute of Engineers*.

Dr. Chen is a member of Phi Tau Phi.