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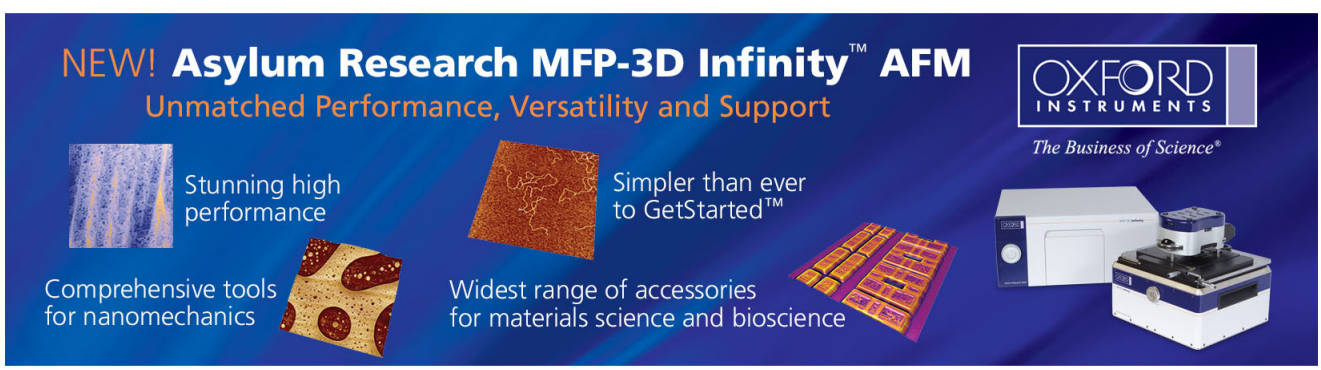

Memory device application of wide-channel in-plane gate transistors with type-II GaAsSb-capped InAs quantum dots

Yu-An Liao,[1] Yi-Kai Chao,[2] Shu-Wei Chang,[3,4,a)] Wen-Hao Chang,[1] Jen-Inn Chyi,[3,5] and Shih-Yen Lin[2,3,4,a)]
[1]*Department of Electrophysics, National Chiao Tung University, Hsinchu 300, Taiwan*
[2]*Institute of Optoelectronic Sciences, National Taiwan Ocean University, Keelung 202, Taiwan*
[3]*Research Center for Applied Sciences, Academia Sinica, Taipei 115, Taiwan*
[4]*Department of Photonics, National Chiao Tung University, Hsinchu 300, Taiwan*
[5]*Department of Electrical Engineering, National Central University, Jhongli 320, Taiwan*

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We demonstrate room-temperature electron charging/discharging phenomena of InAs quantum dots using wide-channel in-plane gate transistors. The device based on type-II GaAsSb-capped InAs quantum dots exhibits both the longer charging and discharging times than those of the type-I counterpart with GaAs capping layers. The slow charge relaxation of GaAsSb-capped InAs quantum dots and simple architecture of in-plane gate transistors reveal the potential of this device architecture for practical memory applications. © *2013 AIP Publishing LLC*.
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Self-assembled InAs/GaAs quantum dots (QDs) have been widely investigated in the last decade.[1] Their applications in optoelectronic and photovoltaic devices such as 1.3 μm laser diodes,[2] infrared photodetectors,[3] and single photon emitters[4] have been demonstrated. In addition to these applications, other advantages of the nanostructures such as the high read/write speed, enhanced capacity for carrier storage, and decent endurance make them a promising candidate for applications of nonvolatile memory devices.[5,6] In previous works, memory characteristics of InAs/GaAs QDs based on optical[7,8] and electrical[9–14] carrier injections were extensively explored. Room-temperature (RT) memory operations have been demonstrated with multi-stacked QD layers,[8,9] and the optimized positioning of a single InAs QD layer in a local conduction-band minimum has also been investigated.[11] However, with the type-I nature of InAs/GaAs heterostructures, the fast carrier recombination, which relaxes the charge storage radiatively, may limit the applications of InAs QDs to memory devices. On the other hand, it has been shown that the band alignment of GaAsSb-capped InAs QDs becomes type-II as the Sb composition exceeds 14%,[15–18] which reduces the unwanted inter-band carrier recombination. Therefore, by changing the capping layer (CL) from GaAs to GaAsSb, we may further improve the charge-storing capability of InAs QDs.

In previous publications, InAs QDs usually act as floating gates above a nearby channel of two-dimensional electron gas (2DEG) based on conventional architectures of high-electron mobility transistors (HEMTs).[8–10,13] In that case, the charging/discharging of electrons in InAs QDs influences the drain current of the device under different biases of the gate voltage. To further simplify the fabrication procedure, the architecture of in-plane gate transistors (IPGTs) with micrometer-sized channel widths is adopted in this work to demonstrate the memory effect of GaAsSb-capped InAs QDs.[19] The operation principle of wide-channel IPGTs is the density variation of 2DEG resulted from the electric fields built by different surface charge populations under different gate biases. This device architecture has also been utilized in the current modulation of a single n-type InGaAs sheet resistance which functions as a photodetector.[20] If the same architecture can be applied to InAs QD memory devices, the simplified fabrication procedure would greatly facilitate the feasibility of InAs QDs in memory applications.

The samples investigated in this work are prepared by a Riber C21 solid-source molecular beam epitaxy (MBE) system. The wafer structures are shown in Table I. After the growth of a 15 nm $Al_{0.3}Ga_{0.7}As$ spacer layer on the 300 nm undoped GaAs buffer layer/semi-insulating GaAs substrate, a QD-related region, 20 nm n-type $Al_{0.3}Ga_{0.7}As$ barrier (doping concentration $1.2 \times 10^{18}\,cm^{-3}$), and 30 nm n-type GaAs layer ($1.7 \times 10^{18}\,cm^{-3}$) are grown successively. A thin undoped 2 nm GaAs layer is grown before the QD layer to maintain the same InAs dot morphology for different samples. The QD layer is formed by depositing 2.7 monolayers (MLs) of InAs at 500 °C and subsequently capped by a 5 nm $GaAs_{1-x}Sb_x$ layer. Two samples with nominal Sb compositions x of 0% and 20% are prepared, which are referred as samples A and B, respectively. For sample B, due to a Sb composition exceeding 14%, the band alignment of InAs/GaAsSb interface is transformed from type-I to type-II. In addition to the two QD samples, a reference sample with an identical structure except for the QD-related region, which is replaced with GaAs, is prepared for further comparisons. The IPGTs are then implemented on these samples under the standard procedures including photolithography, wet etching, and metal evaporation using a thermal coater. The channel lengths and widths of these IPGTs are 5 and 20 μm, respectively. Trenches of 7 μm in width are fabricated to separate the drain/source/channel regions from gate terminals. They are 750 nm in depth and penetrate through the 2DEG layers of the three devices. For transient-current measurements, the Keithley 2400 source meter and 6487 picoammeter/voltage source are adopted for the three-terminal

a)Electronic addresses: swchang@sinica.edu.tw and shihyen@gate.sinica.edu.tw

TABLE I. The wafer structures of the reference sample and samples A and B.

Reference	Sample A	Sample B
	30 nm n-GaAs n = 1.7×10^{18} cm^{-3}	
	20 nm n-$Al_{0.3}Ga_{0.7}As$ n = 1.2×10^{18} cm^{-3}	
	10 nm GaAs	5 nm GaAs/5 nm $GaAs_{0.8}Sb_{0.2}$
	2.7 ML InAs QDs	
12 nm GaAs	2 nm undoped GaAs	
	15 nm undoped $Al_{0.3}Ga_{0.7}As$	
	200 nm undoped GaAs	
	350 μm (100) S-I GaAs Substrate	

device measurement. As the gate-source voltage V_{GS} is varied with the Keithley 2400, the drain currents I_D are recorded using the Keithley 6487 system at a constant drain-source voltage V_{DS} of 1 V. Due to the limit on the time duration between two datum counts of Keithley 6487, the best time resolution of transient-current measurements is about one millisecond. In experiment, the longer time duration of 8.8 ms is adopted to increase the signal-to-noise ratio.

Prior to the investigations of QD charging/discharging behaviors in the IPGTs, an issue to be resolved is whether the surface mobile electrons could follow variations of the gate bias in the millisecond timescale. The RT direct-current (DC) I_D-V_{GS} curve of the reference device is shown in Fig. 1(a). From the curve, a standard transistor behavior with clear current modulations as a function of V_{GS} ranging from −10 to 5 V is observed. The transistor behavior of wide-channel IPGTs originates from the mobile charge population induced by the gate bias.[19] In this case, the transport velocity of surface electrons would be the key factor determining whether (1) IPGTs alone introduce non-negligible dilations in time-dependent measurements, and (2) this architecture is suitable for memory devices under fast modulations of the gate bias or not. The RT time-resolved drain currents of the reference device are shown in Fig. 1(b). After biasing the reference device in the OFF state at $V_{GS} = -10$ V, the gate voltage is abruptly changed to ON state (5 V) at a time $t = 0.5$ s. As shown in the figure, the sudden change of the drain current with a delay-free trace in the millisecond range is observed. The result indicates that the response time of surface mobile electrons is at least below the resolution of 8.8 ms. In this way, the issue on the migration speed of surface mobile electrons can be excluded from the following measurements of QD devices. The result also demonstrates the applicability of this architecture in memory devices.

The hysteresis openings of I_D-V_{GS} curves under opposite sweeping directions of the gate bias would take place as the QD layer serves as a floating gate and influences the nearby 2DEG channel.[9–14] The effect has a twofold cause: (1) the carrier density responsible in 2DEG and (2) the QDs filled with electrons may not be identical at the same V_{GS} in the two opposite sweeping processes. The former is responsible for the current conduction while the latter may act as Coulomb scatters and slightly increase the scattering of nearby 2DEG in addition to the dominant polar scattering of longitudinal optical phonons at room temperature. If electron exchanges between 2DEG and QDs were fast, such hysteresis phenomena would disappear. In the experiment, due to

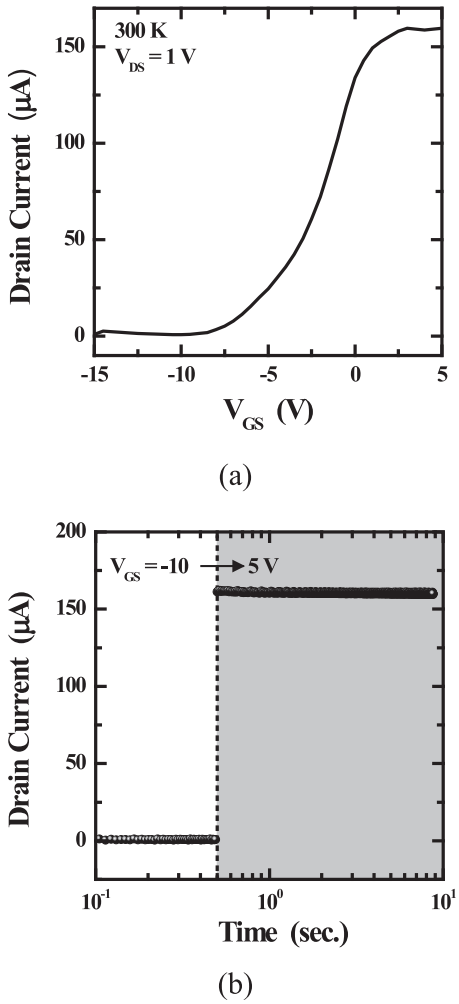

FIG. 1. The RT (a) I_D-V_{GS} curve and (b) time-resolved drain currents (V_{GS} jumps from −10 to 5 V at $t = 0.5$ s) of the reference device at $V_{DS} = 1$ V.

the long electron charging time of QDs, the higher drain current than the ideal one (no hindrance to electron exchanges) would be observed as V_{GS} gradually changes from negative to positive since there are more electrons in 2DEG but fewer ones in QDs than those at equilibrium (QDs slowly get charged). On the other hand, the lower drain current than the equilibrium one should be detected in the opposite sweeping process (QDs gradually turn discharged). The RT I_D-V_{GS} curves of devices A and B at $V_{DS} = 1$ V under different sweeping directions of the gate bias are shown in Fig. 2. The total sweep time of the figure is around 14 s. The significant clockwise hysteresis is observed in device B with GaAsSb-capped InAs QDs while such a phenomenon is undetected in device A with standard GaAs-capped QDs. The presence of hysteresis openings is the minimum requirement for the usage of these nanostructures to memory devices. The result suggests that applications of type-II InAs/GaAsSb heterostructures to memory devices are more promising than those based on the type-I counterparts.

Although the more significant hysteresis opening of device B than that of device A has indicated the longer electron storage times of type-II GaAsSb-capped InAs QDs than type-I counterparts, the magnitudes of these timescales are still important to practical applications. In Fig. 3, we show the RT time-resolved drain currents of devices A and B as

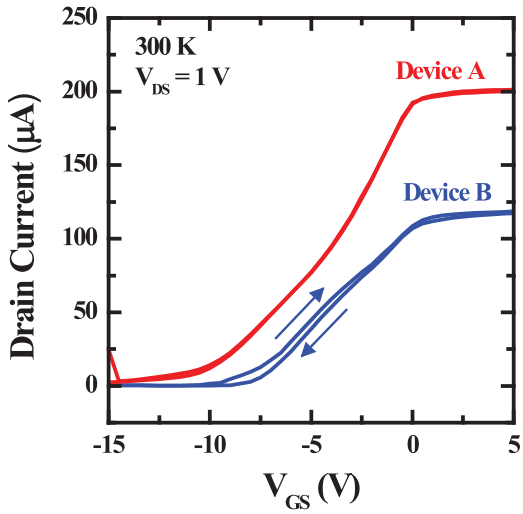

FIG. 2. The RT I_D-V_{GS} curves of devices A and B measured at $V_{DS} = 1$ V under different sweeping directions of the gate bias. The total sweep time of the figure is around 14 s.

V_{GS} jumps from 5 to −5 V at $V_{DS} = 1$ V. While device A exhibits the less prominent but faster current recovery after the sudden reduction, the counterpart of device B comes to the steady state in the much longer recovery time of about 0.5 s. For both of the IPGTs in devices A and B, switching V_{GS} from positive to negative results in accumulations of surface mobile electrons above the n-type AlGaAs barriers and dispels the electrons in 2DEGs of the corresponding channels. This operation accounts for step-like reductions in the drain currents of the two devices in responses to the bias switching. On the other hand, the distinct recovery times are closely related to the type-I/II nature of the nanostructures. In Figs. 4(a) and 4(b), we show the schematic diagrams of GaAs-capped QDs and 2DEG just before and after the switch of V_{GS}, respectively. Since the 2DEG responds to the bias switching (variation of the Fermi level) much faster than QDs do, the originally charged QDs release their excessive electrons at the relatively slower pace. These QDs may discharge through (1) tunneling injections of the electrons to the depleted 2DEG channel, which slightly increases I_D, or

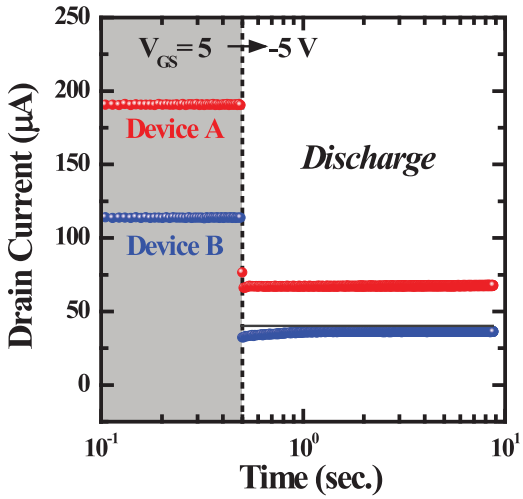

FIG. 3. The RT time-resolved drain currents of devices A and B measured at $V_{DS} = 1$ V. The gate bias V_{GS} changes from 5 to −5 V at $t = 0.5$ s.

(2) interband recombination with the minority holes in bound valence states of QDs. Both processes are not instantaneous and lead to the dilated current response of device A after the bias switching. The discharging process of GaAsSb-capped QDs in device B follows similar scenarios, as indicated in Figs. 4(c) and 4(d). However, the presence of the conduction barrier in the GaAsSb CL further diminishes the wave-function overlaps between QD and channel conduction states and therefore prolongs the tunneling duration. In addition, the type-II nature of the GaSbAs CL eliminates bound valence QD states and turns the interband recombination spatially indirect, which also slowdowns the discharging process. Since both discharging mechanisms are suppressed, the current recovery time becomes significantly longer in device B than in device A.

In addition to the electron discharging phenomena of InAs QDs, it is also important to look into the charging processes in the two devices. The RT time-resolved drain currents of devices A and B as V_{GS} jumps from −15 to 5 V at $V_{DS} = 1$ V are shown in Fig. 5. It takes about 1 and 10 s for devices A and B, respectively, to reach their steady states of current relaxations after the initial current jumps. In this situation, the mobile surface electrons leave the tops of n-type AlGaAs barriers in responses to the bias switching, and the 2DEGs in the originally emptied IPGT channels of the two devices are replenished. The electron charging then takes place from the 2DEG to unoccupied conduction states of InAs QDs, which slightly reduces I_D in both devices. The minority holes in QDs or the GaSbAs CL may be eliminated by the recombination with electrons in 2DEGs or the injected ones in QDs. Overall, the QD charging can be approximately thought of as the reversed processes of those shown in Fig. 4. Still, device B exhibits the longer current relaxation time (or QD charging time) than device A does due to the GaSbAs CL which plays the roles of conduction barriers and type-II hole separation layers. On the other hand, the charging times of QDs are significantly longer than the discharging counterparts. The further slowdown of the charging processes may have two origins. First, the charging phenomena occur in the bias conditions corresponding to Figs. 4(a) and 4(c). Compared to the discharging processes in Figs. 4(b) and 4(d), the steepened potential due to the positive bias V_{GS} in the charging counterparts further reduces the wave-function overlaps between the QD and channel conduction states. Hence, the tunneling injections from 2DEGs into QDs become even less efficient than the reversed ones in Figs. 4(b) and 4(d). Second, the charging process increases the local charge density in QDs, which in turn limits the successive injections of electrons into QDs, namely, the effect of Coulomb blockade.[21] These two additional mechanisms further impede carrier exchanges between QD and channel states in charging processes and may lead to the much slower current relaxations in Fig. 5 than the corresponding recoveries in Fig. 3.

In conclusion, the charging/discharging behaviors of InAs QDs are demonstrated using the architecture of wider-channel IPGTs at room temperature. The prompt response of drain currents to the gate bias for the reference device without QDs suggests that the migration speed of surface mobile electrons is sufficiently fast for memory applications. With the GaAsSb capping layer, the InAs QDs have shown the

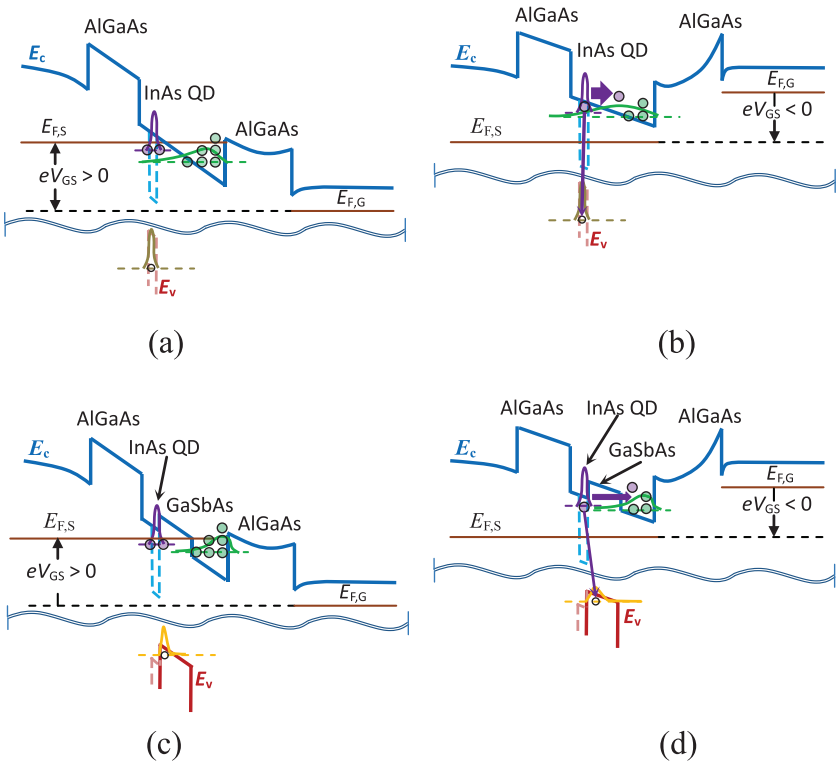

FIG. 4. The schematic band diagrams of device A (a) before and (b) after the bias switching. The counterparts of device B are shown in (c) and (d), respectively. The notations $E_{F,G}$ and $E_{F,S}$ represent the Fermi levels near the gate terminal and substrate side, respectively.

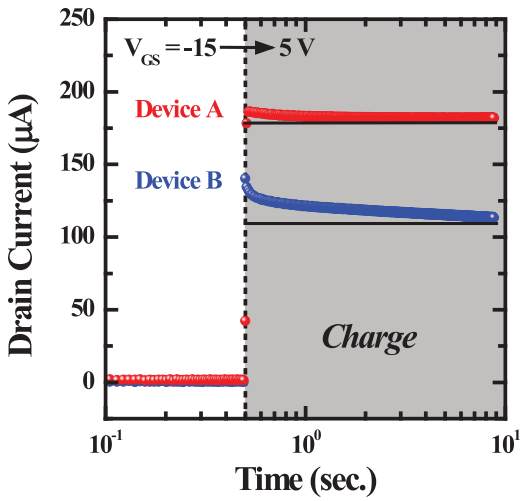

FIG. 5. The RT time-resolved drain currents of devices A and B measured at $V_{DS} = 1$ V. The gate bias V_{GS} changes from −15 to 5 V at $t = 0.5$ s.

longer electron discharging/charging times than their type-I counterparts. The results have indicated the potential of GaAsSb-capped InAs QDs based on the simple IPGT architecture for memory applications.

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