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Citation: Journal of Applied Physics **114**, 124505 (2013); doi: 10.1063/1.4822158
View online: http://dx.doi.org/10.1063/1.4822158
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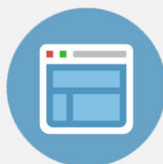
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Abnormal threshold voltage shift under hot carrier stress in $Ti_{1-x}N_x/HfO_2$ p-channel metal-oxide-semiconductor field-effect transistors

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(Received 29 July 2013; accepted 9 September 2013; published online 25 September 2013)

This work investigates the channel hot carrier (CHC) effect in $HfO_2/Ti_{1-x}N_x$ p-channel metal oxide semiconductor field effect transistors (p-MOSFETs). Generally, the subthreshold swing (S.S.) should increase during CHC stress (CHCS), since interface states will be generated near the drain side under high electric field due to drain voltage (V_d). However, our experimental data indicate that S.S. has no evident change under CHCS, but threshold voltage (V_{th}) shifts positively. This result can be attributed to hot carrier injected into high-k dielectric near the drain side. Meanwhile, it is surprising that such V_{th} degradation is not observed in the saturation region during stress. Therefore, drain-induced-barrier-lowering (DIBL) as a result of CHC-induced electron trapping is proposed to explain the different V_{th} behaviors in the linear and saturation regions. Additionally, the influence of different nitrogen concentrations in $HfO_2/Ti_{1-x}N_x$ p-MOSFETs on CHCS is also investigated in this work. Since nitrogen diffuses to SiO_2/Si interface induced pre-N_{it} occurring to degrades channel mobility during the annealing process, a device with more nitrogen shows slightly less impact ionization, leading to insignificant charge trapping-induced DIBL behavior. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4822158]

Consumer electronic products, which are combined display design,[1,2] memory circuits,[3–5] and IC circuits, have become considerably more popular in the last few years. To achieve high speed and light weight, the continuous scaling down of metal oxide semiconductor field electrical field transistors (MOSFETs) is driving conventional SiO_2-based dielectric to be only a few atomic layers thick, leading to excessive gate leakage current and reliability issues.[6–8] To solve the leakage current problem, it is necessary to increase the physical thickness of the gate dielectric. One of the drawbacks of increasing the physical thickness, however, is that drive current will be decreased. Therefore, high-k material is highly recommended over a SiO_2 gate insulator to reduce both tunneling gate leakage and power consumption in CMOS circuits.[9,10] Furthermore, the high-k/metal gate can be integrated with silicon on insulator techniques.[11–13] Additionally, charge trapping in high-k gate stacks remains a key reliability issue, since it causes V_{th} shift and drive current degradation[14–17] due to the filling of pre-existing traps in the high-k dielectric layer.[18–20] With the scaling down of MOSFETs, the issue of charge trapping effect is found to have great impact on channel hot carrier stress (CHCS)-induced device instability, since carriers tend to be injected into the high-k layer.[21,22] However, these studies have mainly focused on characteristics of high-k/metal gate n-MOSFETs under CHCS. There are only a few studies on p-MOSFETs even though p-MOSFETs are as important as n-MOSFETs in CMOS circuits. In this work, we therefore focus on the V_{th} shift characteristics during CHCS on p-MOSFETs. It was found that the behavior of V_{th} shift is toward the positive direction in the linear region, but does not change in the saturation region. Using capacitance-voltage (C-V) technique and observing the gate-induced drain leakage (GIDL) current demonstrate that the charge trapping region under CHCS is mainly localized near the drain overlap region, rather than throughout the overall high-k dielectric layer. In addition, we further investigated the impact of different $Ti_{1-x}N_x$ metal gate electrode compositions on CHCS and found that the interface traps play an important role in V_{th} shift. A device with more interface traps has a smaller V_{th} shift after CHCS.

HfO_2/TiN p-MOSFETs with different concentrations of $Ti_{1-x}N_x$ were studied in this paper as an element of high-performance 28 nm CMOS technology. These devices were fabricated using a conventional self-aligned transistor which progressed via the gate-first process. For gate-first process devices, high quality thermal oxides with thicknesses of 10 Å were grown on a (100) Si substrate as an interfacial oxide layer. After standard cleaning procedures, 30 Å of HfO_2 film was sequentially deposited by atomic layer deposition. Next, 10 nm of TiN film was deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The source/drain activation and poly-Si gate deposition were performed at 1025 °C. The channel and source/drain doping concentrations were about

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$1 \times 10^{18}\,cm^{-3}$ and $1 \times 10^{21}\,cm^{-3}$, respectively. In this study, the dimensions of the selected devices were 1 and 10 μm in length with both 1μm in width. Identical devices with different concentrations and thicknesses of $Ti_{1-x}N_x$ were also investigated. These devices were subjected to the maximum substrate current $I_{b,max}$ during CHCS conditions while at -3.6 V/-4.5 V(L = 1/10 μm) drain voltages (V_d). The stress was briefly interrupted to measure the drain current-gate voltage (I_d-V_g) and substrate current-gate voltage (I_b-V_g) transfer characteristics. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

Figure 1 shows the effects of CHCS on the characteristics of linear I_d-V_g and corresponding Gm-V_g at $V_d = -100$ mV for high-k/metal gate p-MOSFETs. The stress condition V_g was selected at the maximum substrate current $I_{b,max}$ of CHCS conditions while $V_d = -3.6$ V. Results show that there are degradations in the device during CHCS, which show a decrease in transconductance (G_m) and positively shift in threshold voltage (V_{th}), drain current (I_d), however, seems to be invariant at $V_g = -1.6$ V.

Generally, according to the behavior of CHC effect on MOSFETs, there is a serious degradation at the drain side due to the creation of N_{it}, causing decrease in S.S, I_d, and G_m and increase in V_{th}.

However, a positive V_{th} shift (V_{th} became small) is obtained under CHCS for high-k/metal gate p-MOSFETs. This suggests that the positive V_{th} shift results from electron trapping in high-k layer during stress. When electron-hole pairs are produced by impact ionization, the stress voltage difference between gate and drain (V_{gd}) causes electron to tend to inject into the gate side, as shown in the lower left inset of Fig. 1, resulting in the V_{th} shift. Further, CHC-induced electrons flowing below the channel forms substrate current (I_b). The top right inset of Fig. 1 shows the I_d-V_g curve under semi-logarithmic scale before and after CHCS. It can be observed that the subthreshold swing (S.S.) was not affected, illustrating that N_{it} generation was insignificant. Therefore, this result supports our assertion that the positive shift in V_{th} is indeed induced by electron-trapping in the high-k layer located at the drain side rather than CHC-induced N_{it}.

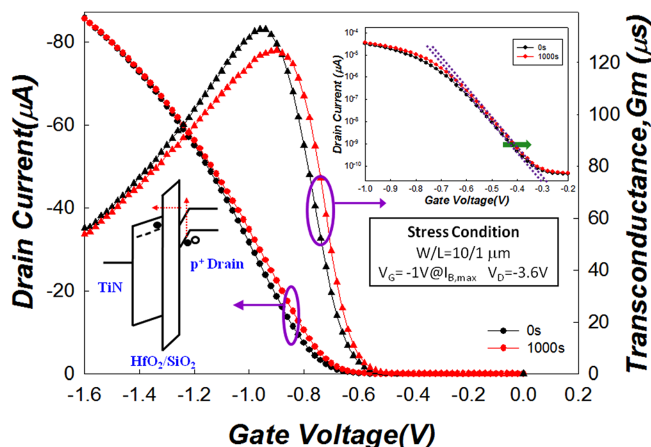

FIG. 1. The characteristics of linear I_d-V_g and corresponding Gm-V_g at $V_d = -100$ mV for high-k/metal gate p-MOSFETs. The inset shows S.S. of log I_d-V_g curve.

In addition, it is likely that the injection carrier in the high-k dielectric is electrons. Fig. 2(a) shows the effect of CHCS on the GIDL characteristics by measurement of saturation I_d-V_g and corresponding I_b-V_g from $V_g = 0.5$ V to $V_g = -1.6$ V with Vd = -2.4 V. The GIDL current decreases with stress time, because the electrons trap in the high-k dielectric, which lead to a longer band-to-band tunneling path, in turn, reducing GIDL current, shown by the corresponding energy diagram in the inset of Fig. 2(a). Capacitance-voltage (C-V) measurement techniques indicate the location of electron trapping before and after CHCS. The gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}) characteristics under initial and after CHCS are measured and shown in Fig. 2(b) and its inset, respectively. Note that the C_{gd}-V_g curve shifts in the positive direction after CHCS, but the C_{gs}-V_g curve has no significant change before and after CHCS. This result supplies evidence that electron injection induced by CHCS is mainly trapped near the drain side of the high-k dielectric.

The correlation between the stress time and the V_{th} shift is extracted from I_d-V_g in linear and saturation region and is shown in Fig. 3(a). It can be seen that the V_{th} shifts in the linear region under CHCS, however, the V_{th} shift in the

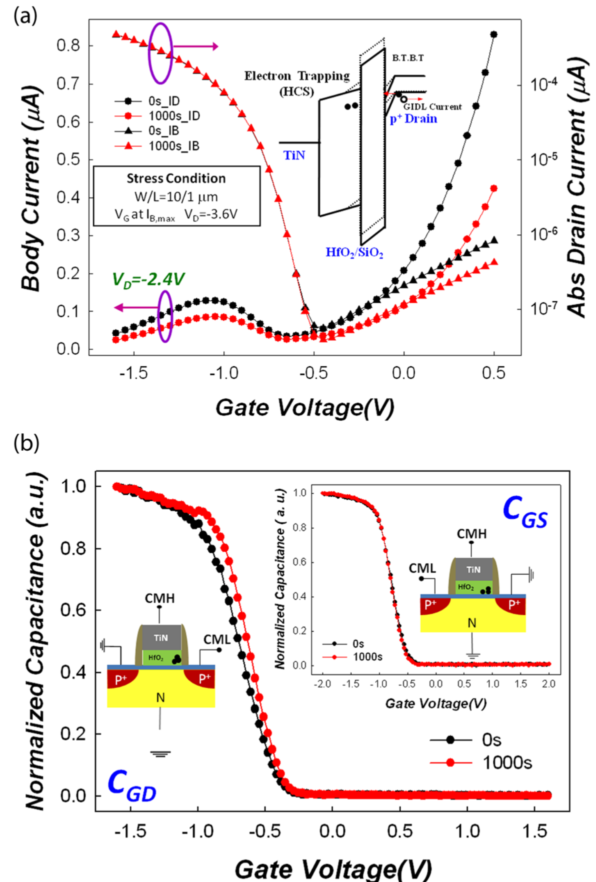

FIG. 2. (a) The saturation I_d-V_g and corresponding I_b-V_g from OFF-state to ON-state at $V_d = -2.4$ V. The inset shows the energy-band diagram cutting from drain overlap region during CHCS. (b) Cgd-Vg and (inset) Cgs-Vg transfer characteristics under initial and after CHCS. Diagrams indicate their respective measurement methods.

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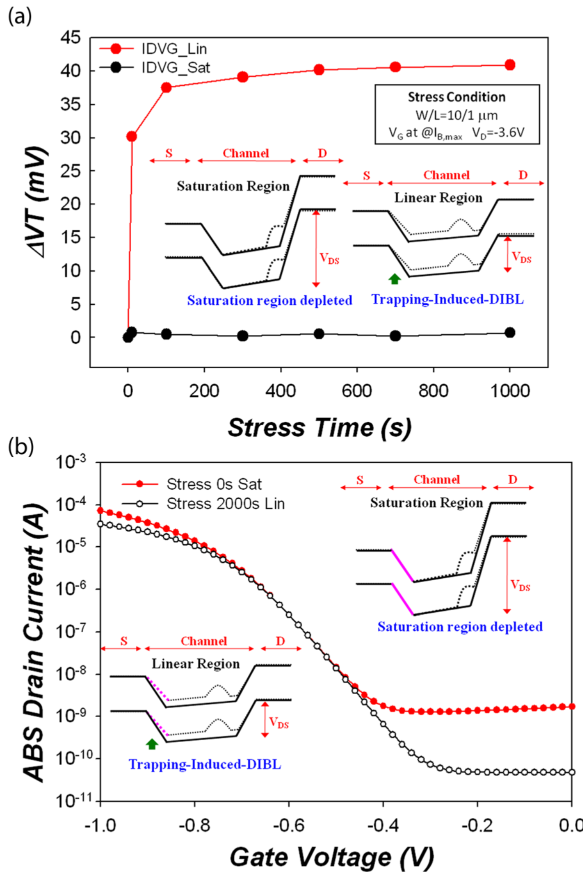

FIG. 3. (a) The degradation of ΔV_{th} versus stress time in linear and saturation regions during CHCS. The inset shows the energy-band diagram to illustrate charge trapping-induced-DIBL effect. (b) The characteristics of I_d-V_g curves in saturation before CHCS and linear region after CHCS. The inset shows the energy-band diagram in linear and saturation regions at initial and after CHCS.

saturation region is almost uninfluenced during stress. According to this, we suggest that the behavior can be attributed to charge trapping-induced DIBL (drain-induced-barrier-lowering) effect. The electrons coming from impact ionization are trapped into the high-k layer at the drain side and result in DIBL behavior, lowering V_{th}. However, in the saturation region, the source barrier height is dominated by higher V_d. According to the inset of Fig. 2(b), C_{gs} shows no significant change, illustrating no damage at the source, corresponding to no V_{th} shift.

Furthermore, Figure 3(b) shows a comparison of the I_d-V_g curves in the linear region after CHCS and saturation region before CHCS. It can be seen that the influence of trapping does not extend to the source during saturation operation. This is because saturation V_d depletes the trapping and dominates channel potential.

To clearly illustrate that this phenomenon of electron trapping during CHCS being mainly trapped near the drain side, leading to the trapping-induced DIBL effect, channels of different lengths were examined. For the longer channel device, the stress condition was also selected at $I_{b,max}$. In order to achieve the same amount of electrons, an I_b current of 10 μA, similar to the shorter channel device was selected, as shown in the inset of Fig. 4. Based on the results in Fig. 4, which shows a comparison of V_{th} as function of stress time

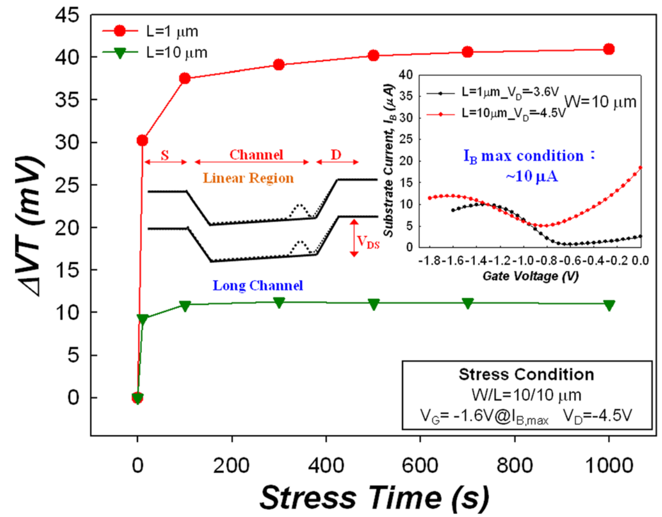

FIG. 4. The degradation of ΔV_{th} versus stress time for L = 1 and 10 μm. The inset shows I_b-V_g, indicating identical I_b stress condition for both devices.

for short and longer channels, it can be seen that the V_{th} shift for the long channel device has less degradation than the short one. This is because it is sufficiently long to endure the influence of drain voltage and trapping in the linear region, thereby suppressing the trapping-induced DIBL effect.

The impact of different composition $Ti_{1-x}N_x/HfO_2$ p-MOSFETs under CHCS was also investigated. Devices were fabricated with different metal gate stack concentrations: $Ti_{1-a}N_a$ has less nitrogen (N), while $Ti_{1-b}N_b$ has more nitrogen (N). As has been previously shown, the nitrogen of the metal gate can diffuse to the SiO_2/Si interface during the annealing process, causing additional defects.[23] Therefore, the $Ti_{1-b}N_b$ device exhibits more interface states (pre-N_{it}) by the charge pumping measurement,[24] corresponding to more N, as shown in Figure 5(a). Figure 5(b) shows the charge trapping-induced V_{th} shift for $Ti_{1-x}N_x/HfO_2$ p-MOSFETs under CHCS. It can be observed that a smaller V_{th} shift under stress corresponds to a metal gate with higher N concentration. This is due to channel mobility degradation from pre-N_{it}. The mobility degradation leads to a decrease in impact ionization, causing fewer trapping carriers. Hence, fewer electron-hole pairs are generated, further reducing the probability of trapping behavior.

To further confirm that the pre-N_{it} results in this phenomenon, a device with thinner high-k layer was utilized. Generally, N can diffuse to the SiO_2/Si interface and easily generate pre-N_{it} with a thinner high-k layer. Therefore, the device with thinner HfO_2 should exhibit the least degradation due to more pre-N_{it}. Charge pumping current versus gate voltage for $Ti_{1-b}N_b/HfO_2$ p-MOSFETs with thinner and thicker HfO_2 are shown in the inset of Figure 6. Clearly, the device with $Ti_{1-b}N_b$ and thinner HfO_2 shows more insignificant V_{th} shift than that with thicker HfO_2. The V_{th} shift for the $Ti_{1-a}N_a/HfO_2$ device is also shown for comparison in Fig. 6 to confirm that less charge trapping-induced DIBL behavior is due to more pre-N_{it}, reducing V_{th} shift.

This paper investigates the effect of channel hot carrier stress on $Ti_{1-x}N_x/HfO_2$ p-MOSFETs. The positive V_{th} shift can be observed in the linear region but no shift in the

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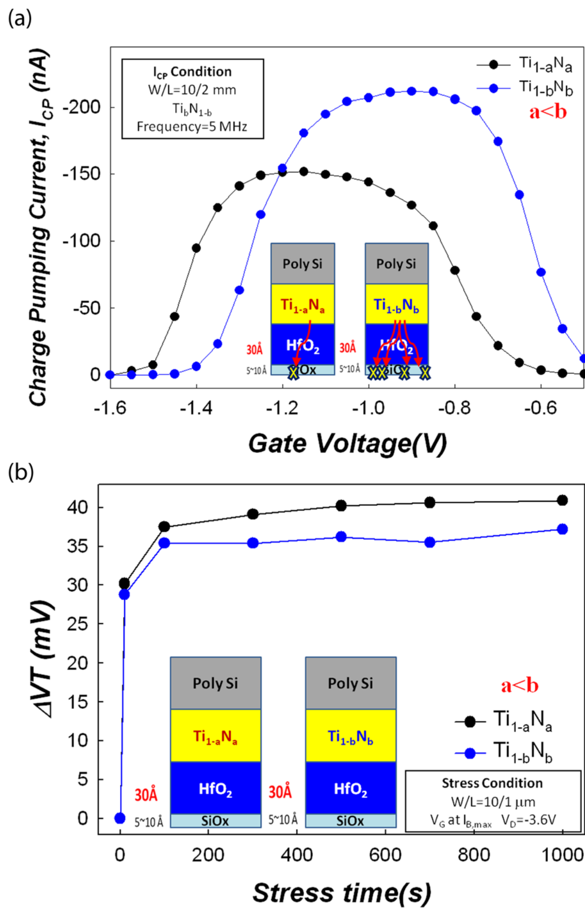

FIG. 5. (a) The characteristics of I_{cp}-V_g curves for devices with different metal gate stacks. The inset shows the Si/SiO_2 interface of both devices with interface states. (b) The degradation of ΔV_{th} versus stress time for two different metal gate stacks.

saturation region under CHCS is due to trapping-induced DIBL effect. Electron trapping during CHCS being mainly trapped near the drain side, leading to the trapping-induced DIBL effect was also confirmed, which has been verified by modifying channel length. Investigation of charge trapping-induced DIBL behavior under CHCS for different metal gate stack compositions showed that pre-N_{it} dominates the amount of trapping carrier, since decreasing mobility reduces the impact ionization.

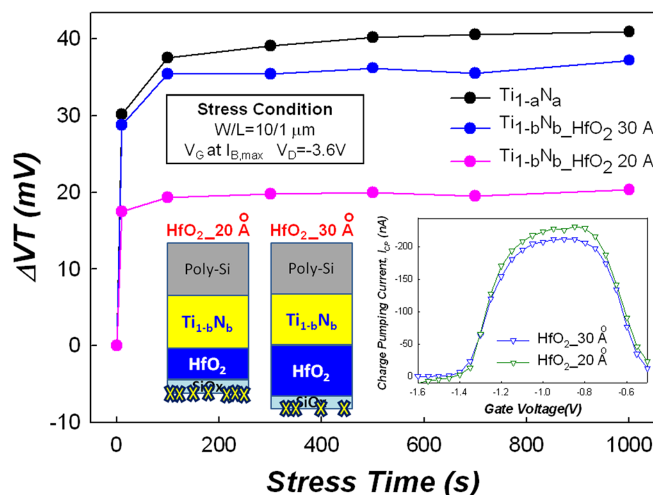

FIG. 6. The degradation of ΔV_{th} versus stress time during CHCS for different metal gate stacks of different HfO_2 thicknesses. The inset shows the I_{cp}-V_g curves for different HfO_2 thicknesses.

Part of this work was performed at United Microelectronics Corporation. The work was supported by the National Science Council under Contract No. NSC-102-2120-M-110-001.

[1] T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, "Developments in nanocrystal memory," Mater. Today **14**, 608 (2011).
[2] M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, "Influence of electrode material on the resistive memory switching property of indium gallium zinc oxide thin films," Appl. Phys. Lett. **96**, 262110 (2010).
[3] Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, "Redox reaction switching mechanism in RRAM device with Pt/CoSiOX/TiN structure," IEEE Electron Device Lett. **32**, 545 (2011).
[4] C. T. Tsai, T. C. Chang, S. C. Chen, I. Lo, S. W. Tsao, M. C. Hung, J. J. Chang, C. Y. Wu, and C. Y. Huang, "Influence of positive bias stress on N_2O plasma improved InGaZnO thin film transistor," Appl. Phys. Lett. **96**, 242105 (2010).
[5] T. C. Chen, T. C. Chang, C. T. Tsai, T. Y. Hsieh, S. C. Chen, C. S. Lin, M. C. Hung, C. H. Tu, J. J. Chang, and P. L. Chen, "Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress," Appl. Phys. Lett. **97**, 112104 (2010).
[6] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, IEEE Electron Device Lett. **18**, 209 (1997).
[7] C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, F. Y. Jian, W. H. Lo, S. H. Ho, C. E. Chen, W. L. Chung, J. M. Shih, G. Xia, O. Cheng, and C. T. Huang, Appl. Phys. Lett. **98**, 092112 (2011).
[8] C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. C. Tsai, S. H. Ho, W. H. Lo, G. Xia, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **31**, 540 (2010).
[9] Y. Kim, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres, J. E. Lim, B. Foran, F. Shaapur, A. Agarwal, P. Lysaght, G. A. Brown, C. Young, S. Borthakur, H. J. Li, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R. W. Murto, H. Alex, H. R. Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanec, and C. Werkhoven, Tech. Dig. - Int. Electron Devices Meet. **2001**, 20.2.1.
[10] C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. H. Ho, T. Y. Hsieh, W. H. Lo, C. E. Chen, J. M. Shih, W. L. Chung, B. S. Dai, H. M. Chen, G. Xia, O. Cheng, and C. T. Huang, Appl. Phys. Lett. **99**, 012106 (2011).
[11] W. H. Lo, T. C. Chang, C. H. Dai, W. L. Chung, C. E. Chen, S. H. Ho, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **33**, 303 (2012).
[12] C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. T. Tsai, W. H. Lo, S. H. Ho, G. Xia, O. Cheng, and C. T. Huang, Surf. Coat. Technol. **205**, 1470 (2010).
[13] C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, F. Y. Jian, W. H. Lo, S. H. Ho, C. E. Chen, W. L. Chung, J. M. Shih, G. Xia, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **32**, 847 (2011).
[14] S. H. Ho, T. C. Chang, C. W. Wu, W. H. Lo, C. E. Chen, J.-Y. Tsai, G. R. Liu, H. M. Chen, Y. S. Lu, B. W. Wang, T. Y. Tseng, O. Cheng, C. T. Huang, and S. M. Sze, Appl. Phys. Lett. **102**, 012103 (2013).
[15] M. Casse, L. Thevenod, B. Guillaumot, L. Tosti, F. Martin, J. Mitard, O. Weber, F. Andrieu, T. Ernst, G. Reimbold, T. Billon, M. Mouis, and F. Boulanger, IEEE Trans. Electron Devices **53**, 759 (2006).
[16] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, IEEE Trans. Device Mater. Reliab. **5**, 5 (2005).
[17] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, J. Appl. Phys. **93**, 9298 (2003).
[18] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, P. M. Zeitzoff, G. A. Brown, B. H. Lee, and R. W. Murto, Microelectron. Reliab. **44**, 1509 (2004).
[19] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, IEEE Electron Device Lett. **24**, 87 (2003).
[20] H. R. Harris, R. Choi, J. H. Sim, C. D. Young, P. Majhi, B. H. Lee, and G. Bersuker, IEEE Electron Device Lett. **26**, 839 (2005).

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[21]E. Amat, T. Kauerauf, R. Degraeve, R. Rodríguez, M. Nafría, X. Aymerich, and G. Groeseneken, IEEE Trans. Device Mater. Reliab. **9**, 425 (2009).
[22]G. Zhang, C. Yang, H. M. Li, T. Z. Shen, and W. J. Yoo, in *IEEE 12th International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* (2010), p. 894.
[23]X. Garros, M. Cassé, G. Reimbold, F. Martin, C. Leroux, A. Fanton, O. Renault, V. Cosnier, and F. Boulanger, Dig. Tech. Pap. - Symp. VLSI Technol. **2008**, 68.
[24]G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, IEEE Trans. Electron Devices **31**, 42 (1984).

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