

The integration of Ge and III-V materials on GaAs and Si for Post CMOS applications

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In the study, the growth of InAs on Si is demonstrated using “interface blocking” technique with SiGe layers as buffer layer. And the growth of high quality Ge film on GaAs is demonstrated using ultra high vacuum chemical vapor deposition (UHVCVD). Both Ge film grown on GaAs and InAs film grown on Si substrate demonstrate high crystallinity and good surface morphology as observed by XRD and AFM. Furthermore, the fabrication process and electric characteristics of Ge/GaAs and InAs/Si is discussed in the study. The developed epitaxial materials systems and device fabrication including InAs on Si, Ge on GaAs are useful for future III-V and Ge integration on Si substrate for next generation high speed low power CMOS as well as for RF/digital mixed signal circuit applications in the future.

1. Introduction

Recently, the semiconductor industry community faces challenges from the continued reduction of device feature sizes for silicon devices. Meanwhile, the III-V compound semiconductor materials such as InSb, $\text{In}_x\text{Ga}_{1-x}\text{As}$ attract a lot of attentions for post CMOS applications, because these materials have significantly higher carrier mobility than silicon. For example, InAs has an electron mobility of $20000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. High-speed devices such as quantum-well field-effect transistors (QWFETs) made from these III-V materials have demonstrated very low gate delay time. Meanwhile, for the post CMOS applications, Ge is considered as a good candidate for p-channel material because of its high hole mobility ($1,900\text{cm}^2\text{V}^{-1}\text{s}^{-1}$). The Ge epitaxial film grown on GaAs is of immense interest due to the lattice mismatch is practically zero ($\sim 0.08\%$) which ensures large critical thickness and low dislocation density, strain-free Ge epitaxial film. As a result, they have the great potential as the transistor-channel materials for quantum-well field-effect transistors (QWFETs) and show very attractive and tangible merits over scaled Si MOSFETs. In addition, these devices are well established on GaAs and InP substrates with high cost. These problems can be solved by growing the SiGe buffer layer on Si substrate as the templates for high-hole-mobility Ge for p-channel and high-electron-mobility III-V materials, such as $\text{In}_x\text{Ga}_{1-x}\text{As}$ or InAs, for n-channel with the complementary circuitry architecture. A seamless, robust heterogeneous integration

scheme of III-V nFETs and Ge pFETs on silicon will allow high-speed, low-voltage transistors to couple with the mainstream Si CMOS platform, while avoiding the need for developing large diameter III-V substrates with a substantial reduction in cost, reduced brittleness and increased size.

2. Experimental Process

InAs on Si material growth

For the SiGe/Si template for the further $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ structure growth, the epitaxial SiGe and Ge layers were grown by UHVCVD equipment using silane (SiH_4) and germane (GeH_4) as the Si and Ge sources. The 4" Si substrates were cleaned by immersing in deionized water (DI water) for 3 mins and dipped in 10% hydrofluoric acid (HF) for 5 seconds to remove silicon oxide away. The oxide-free surface and surface passivated by the dangling bonds terminated with hydrogen are obtained by the HF dipping process.

In the growth of 1st SiGe buffer layer at 350°C, the composition of Si and Ge are 0.1 and 0.9. Then the 2nd SiGe buffer layer where the composition of Si and Ge are 0.05 and 0.95 was grown on the top of the 1st SiGe buffer layer at 350°C and finally the pure Ge layer was grown on this structure. Between the processes of each epitaxial layer, annealing step is introduced for 10 minutes at 600 °C to improve the crystal quality of the epitaxial layers. Finally, annealing was performed again at 600 °C for 10 min in order to remove defects that are possibly generated in the growth of Ge layer. And the structure can be the SiGe/Si template for further integration with $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT structure.

The Fig. 1(a) demonstrates the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ structure grown on SiGe/Si template. Three epitaxial growth systems were used to grow this structure. First, an ultrahigh vacuum chemical vapor deposition (UHVCVD) system was used to grow the SiGe/Si template as mentioned above. Then, a commercial metal organic chemical vapor deposition (MOCVD) was utilized to grow a thin GaAs film on the top of the Ge film(1). Finally, the high quality $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT structure was grown by a molecular beam epitaxy (MBE) system.

During the MOCVD growth, the growth pressure of the GaAs film is 40 torr, and V/III ratio is 100 (1). Finally, the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT was grown on top of the Ge layer by MBE system and the wafer was baked at 630 °C for 1 min before the growth. And the buffer layer were grown at 560°C including a GaAs layer, an AlSb layer, two GaSb/AlSb superlattice, and two $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}$ layers to accommodate the 7% lattice mismatch between the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT structure and the Ge layer. Then InAs channel layer including a 50 nm $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}$ layer, a 15 nm InAs layer, a 13 nm $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}$ layer (Schottky layer), and a 3 nm GaSb layer (cap layer) were grown on the top of the buffer layer to form the AlGaSb/InAs HEMT structure. The growth temperature of InAs layer and $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}$ layer was set at 520 °C to obtain good quality InAs channel layer.

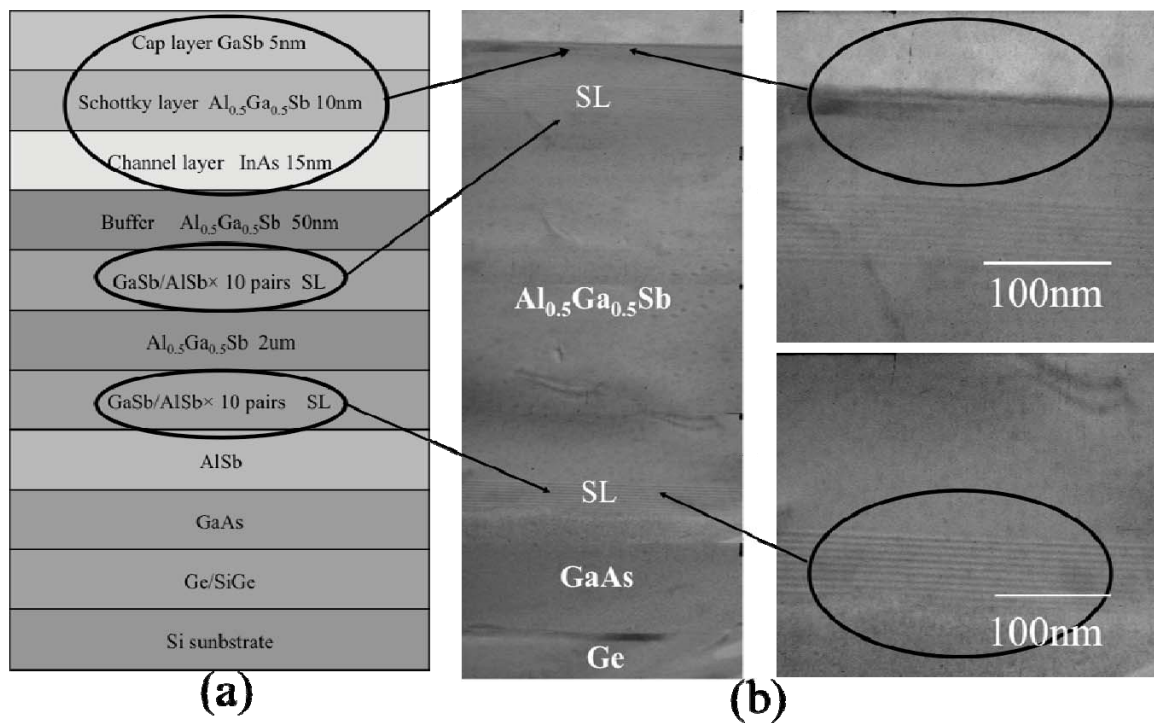


Figure 1. The illustration of $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT on Si substrate and the cross section of the TEM images

Ge/GaAs material growth

In the Ge epitaxial growth, epi-ready GaAs 2-inch (100) wafers were used as substrates for Ge deposition. GeH_4 was used as the Ge source when Ge deposition by UHV-CVD system. The as-received GaAs wafer was loaded into the load-lock chamber without any pre-cleaning step after breaking the N_2 filled package. The native oxide (As_2O_3 and Ga_2O_3) on the GaAs surface could be removed by a prebake step in the growth chamber at 600°C , because the native oxide of GaAs would be decomposed at high temperature. Due to the sensitive nature of GaAs substrate surface, the prebake time should be controlled carefully to prevent the decomposition and overpressure of GaAs. During the growth of 250nm Ge film growth at 600°C , the GeH_4 flow rate and the growth pressure was fixed at 10 sccm and 20 mTorr.

Ge/GaAs MOSCAPs

For the Ge/GaAs MOSCAPs fabrication, the Ge/GaAs wafer was degreased in acetone and isopropanol followed by the removal of native oxide using HF (49%): $\text{H}_2\text{O}=1:100$ solution and finally rise with deionized (DI) water. After the HF treatment, one sample went through rapid thermal oxidation (RTO) to grow a thin GeO_2 film prior to the deposition of Al_2O_3 . The RTO was performed at 450°C for 5 minutes in oxygen atmosphere. After that, $\sim 10\text{nm}$ atomic layer deposition (ALD) Al_2O_3 was deposited at 250°C as the MOSCAP dielectric. Post deposition annealing (PDA) was carried out at 400°C for 5 minutes in forming gas (2) followed by e-beam evaporated Pt/Au

(500Å/1000Å) gate metal and Ti/Au (500Å/1000Å) ohmic contact, respectively. Finally, post metal annealing was performed at 250 °C for 30 seconds in forming gas.

3. Results and Discussion

InAs on Si material growth

The TEM analysis of SiGe/Si template reveals that propagated dislocations were bent sideward and terminated very effectively at the $\text{Si}_{0.05}\text{Ge}_{0.95}/\text{Si}_{0.1}\text{Ge}_{0.9}$ and $\text{Ge}/\text{Si}_{0.05}\text{Ge}_{0.95}$ interfaces, so the threading dislocation density of Ge film is $8.3 \times 10^6 \text{ cm}^{-2}$ measured by etching pit method. Through the AFM tapping mode measurement as shown in fig. 2, the root mean square (RMS) of the Ge surface is 32 Å.

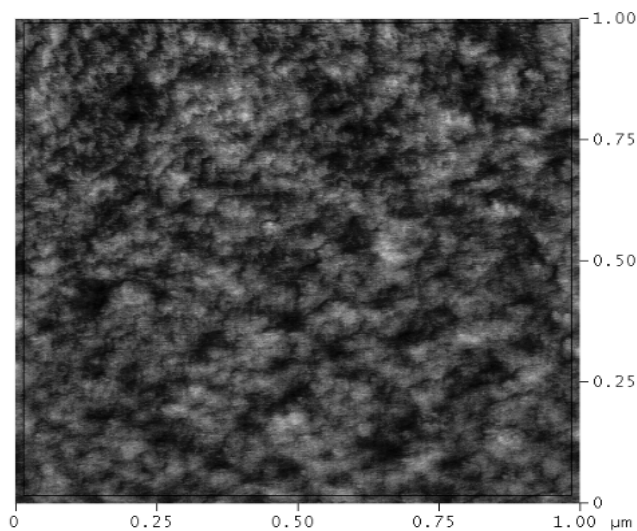


Figure 2. The the root mean square (RMS) of the Ge surface is 32 Å by AFM measurement.

It is obvious from the cross-sectional TEM images (Fig. 1b) of the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT on Ge with SiGe buffer layer that the interfaces of buffers were quite smooth, and the defect density in InAs channel is pretty low. And the root mean square (rms) of the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT on Si wafer surface was 19.1 Å. From the high resolution x-ray diffraction (HRXRD) analysis, these major peaks is very clear, and it indicates that the crystalline quality of the HEMT structure was very good. The room-temperature electron mobility of $27300 \text{ cm}^2/\text{Vs}$ was achieved for the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT grown on SiGe/Si template. This is the highest mobility for a HEMT structure grown on Si substrate reported so far and that a very-high mobility $\text{Al}_{0.5}\text{Ga}_{0.5}\text{Sb}/\text{InAs}$ HEMT structure has been demonstrated with well designed buffer layer.

"Ge/GaAs" MOSCAPs: A C-V curve

The crystal quality of 250nm Ge film deposited at 600°C was checked by HRXRD measurement (Bede D1 XRD system). The double axis scanned result is Fig. 3 with the GaAs substrate peak at zero, the HRXRD result is in black line and the simulated curve is

in gray line. The HRXRD result and the simulated curve match closely with each other, it represents that the quality of Ge film grown on GaAs is very closed to the optimized condition. The appearance of fringes on both sides of Ge and GaAs peaks implies a parallel and very good interface existed in this Ge/GaAs heterojunction structure (3). The root mean square roughness (rms) of Ge film was only 0.132 nm by AFM measurement. Figure 4 shows the cross sectional TEM micrograph of 2.75 μm thick Ge film deposited on GaAs substrate grown at 600 $^{\circ}\text{C}$. A few misfit dislocations are detected at the interface, but there is no appearance of any threading dislocation.

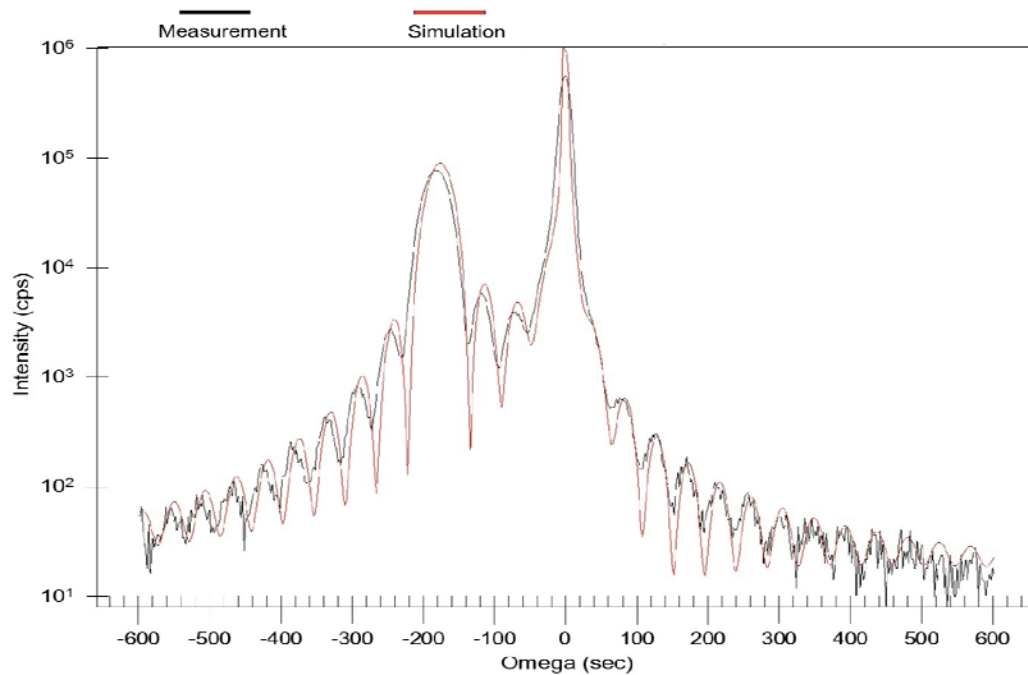


Figure 3. XRD measurement of 200 nm Ge film on GaAs substrate. The fringes on both sides imply a sharp Ge/GaAs interface

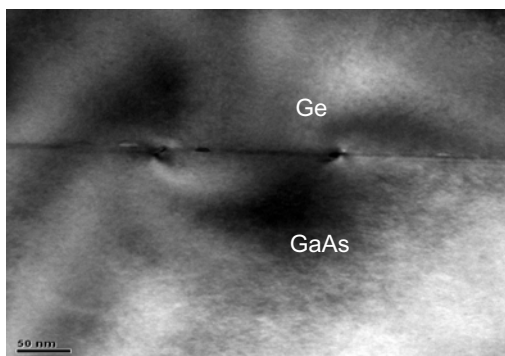


Figure 4. Cross-sectional TEM image of Ge on GaAs. A few misfit dislocations are seen at the interface but no threading dislocation is detected.

The multi-frequencies C-V behaviors of $\text{Al}_2\text{O}_3/\text{Ge}/\text{GaAs}$ MOSCAPs with HF treatments measured at the frequencies from 100 Hz to 100 kHz shows p-type behavior, it

represents that the Ge epitaxial layer exhibits n-type doping which is in agreement with the previous study and is related from the arsenic auto-doping effect during the growth of Ge epitaxial film on GaAs (4). Excellent C-V curves with good inversion behaviors were observed for both the samples, and the sample shows smaller frequency dispersion in accumulation region and depletion region as compared with the sample with HF treatment.

For high performance MOSFET, the interface quality of the MOS capacitor is very important, and the lower D_{it} is needed. The higher D_{it} value has a significant effect on the transistor performance by increasing the transistor sub-threshold slope, drain-induced barrier lowering, etc. The values of D_{it} of these samples were extracted by conductance method (5).

At different gate voltages in the depletion region, the D_{it} values estimated at near Ge mid-gap by conductance method are $1.2 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ for samples with HF treatment. The D_{it} estimation was took into consideration of the weak inversion response, resulting in the overestimation of the D_{it} (6). For more accurate estimation of D_{it} , full conductance method needs to be applied and the true values should be one order lower than these above values, i.e. about mid $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ for the case treated by HF (6).

4. Conclusion

Both Ge film grown on GaAs and InAs film grown on Si substrate demonstrate high crystallinity and good surface morphology as observed by XRD and AFM. Furthermore, the fabrication process and electric characteristics of Ge/GaAs MOSCAP were discussed in the study. The developed epitaxial materials systems and device fabrication including InAs on Si, Ge on GaAs are useful for future III-V and Ge integration on Si substrate for next generation high speed low power CMOS as well as for RF/digital mixed signal circuit applications in the future.

Reference

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