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Study of Conduction Modes of Time to Dielectric Breakdown Reliability in Cu Damascene Structures

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Low k time-dependent dielectric breakdown is increasingly becoming a major issue at the 45 nm technology node and beyond. Although TDDB models, such as the E model, the $\sqrt{E}$ model and the 1/E model, have been extensively explored, determining the back end of line processing direction for TDDB warrants further study. This study attempts to determine whether the thickness of the etching stop layer film influences the electron conduction mechanism. Cu damascene structures were designed following three approaches with various thickness of the etching stop layer : Co/ESL = 0 A-550 A (low-k: SiCO k = 3.1), Cu/ESL = 0 A-275 A (low-k: SiCO k = 2.5) and Co/ESL = 0 A-275 A (low-k: SiCO k = 2.5). The application of capping material Co is warranted for electron emission suppression, but the oxygen attacking from subsequent low-k deposition is a concern. In addition, greater ESL thickness offers paths for electron conduction which worsens TDDB; i.e., less ESL thickness is better. Therefore, the combination of Co with SiH_4 treatment addresses optimized conditions to achieve an ESL-less application for TDDB enhancement.
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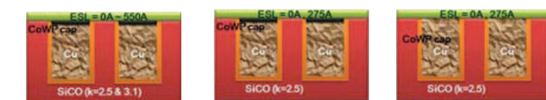
Currently, low-k dielectrics are applied to reduce back end of line (BEOL) interconnect RC delay.[1–5] Low-k dielectrics in the interconnect system reduce the power dissipation and signal propagation delay. To further reduce the BEOL dielectric constant, an etching stop layer (ESL) with a lower dielectric constant is sought. In addition, the use of a Co cap in the parallel approach has been investigated because of its etch stop capability as well as considerable EM resistance.[6–10] The increased interconnect density with tightening design rules represents a reliability concern, especially in the TDDB. Therefore, the provision of BEOL and low capacitance without detrimentally affecting reliability is an important subject. The work develops ESL and Co cap engineering in the Cu damascene structure.[11,12] The effect of the ESL thickness on breakdown field is systematically investigated using 32 nm technology nodes. The conduction mechanisms are also elucidated. The TDDB performance of Cu/ESL is compared with that of Co/ESL.

Table I. Structures used in this study.

	Scheme A	Scheme B	Scheme C
Metal	Cu/75 A Co SiH_4 treatment	Cu/50 A Co SiH4 treatment	Cu
ESL	SiCN in 0 A ∼ 550 A	SiCN in 0 A and 275 A	SiCN in 0 A and 275 A
LK	LKA, k = 3.1 LKB, k = 2.5	LKB, k = 2.5	LKB, k = 2.5
Node	32 nm	32 nm	32 nm



Experimental

Table I presents three approaches that were applied in this investigation. A self-aligned cobalt tungsten phosphide (Co) cap deposited on top of interconnect was used. Porous low-k dielectric which lies between the lines was made of plasma chemical vapor deposition. In addition, SiCN etching stop layer (ESL) was chosen material with high etch selectivity compared with low-k to form Cu damascene structure. The technology used in this study was 32 nm technology node in 12 inch Si wafers. In scheme A, low-k with k = 2.5 and 3.1/ESL = 0 A ∼ 550 A/Co cap was fabricated. SiH_4 treatment after Co deposition was applied to improve oxygen resistance of Co, where SiH_4 treatment condition was 275°C, 30 sec. In schemes B and C, low-k with k = 2.5/ESL = 0 A and 275 A were fabricated. A Co cap was also implemented in scheme B. Room-temperature breakdown voltage tests (VBD) and Time to Dielectric Breakdown (TDDB) tests were performed using a temperature of 125°C in an applied electrical field of 3.0 MV/cm.

Results and Discussion

Fundamental study of interface integrity.— Figures 1a and 1b schematically depicts the Cu silicide/low-k scheme and the Co silicide/low-k scheme. Correspondingly, Figs. 1c and 1d present TEM images of Cu/ESL = 0 A and Co/ESL = 0 A, respectively. The smooth via-bottom surface is obtained by optimized SiH_4 post- Cu or post-Co surface treatment. Fig. 1e further shows TEM image of Co/ESL = 0 A

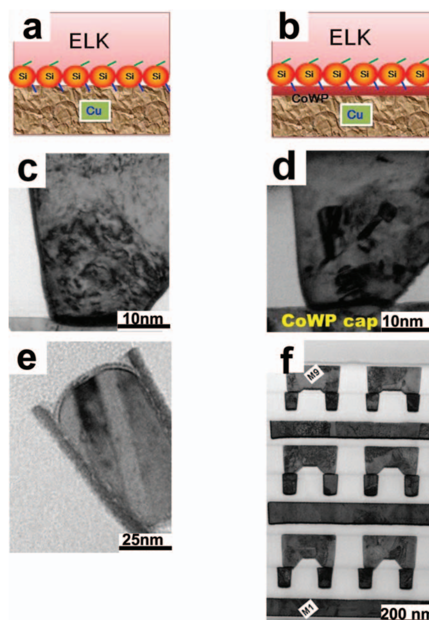


Figure 1. (a) Schematic diagram of Cu silicide/low-k scheme. (b) Schematic diagram of Co silicide/low-k scheme. (c) TEM image of damascene structure with Cu/silicide/low-k scheme. (d) TEM image of damascene structure with Co/silicide/low-k scheme. (e) TEM image of trench structure with Co/silicide/low-k scheme. (f) TEM image of 9 metal layers with Co/silicide/low-k scheme.

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trench profile. The full run of Co/ESL = 0 A including 9 metal layers is shown in Fig. 1f.

To determine the interfacial integrity of Co silicide, X-ray photoelectron spectroscopy (XPS) is used to identify the bonding structure. The results reveal the presence of Co silicide for Co after treatment with an amorphous phase, which corresponds to the Co_2Si structure that is formed by SiH_4 treatment. XPS revealed a superior oxygen barrier, such that no additional Co-O bonds formed when this Co silicide underwent CO_2 plasma attacking. Figure 2a and 2b present samples A, B, C and D which are Co, Co that underwent CO_2 plasma attacking, Co with SiH_4 treatment and Co with SiH_4 treatment that underwent CO_2 plasma attacking. For sample A, the XPS core level spectra of Co(2p) and Co(3p) are observed at 781.6 eV and 100.5 eV respectively. An significant increase in Co(2p)-O and Co(3p)-O at 780.0 eV and 100.5 eV are investigated for Co that underwent CO_2 attack shown in sample B. For sample C, XPS core level spectra of Co(2p)-Si and Co(3p)-Si at 778.2 eV and 101.5 eV can be observed for Co after SiH_4 treatment samples. In contrast to the Co sample,

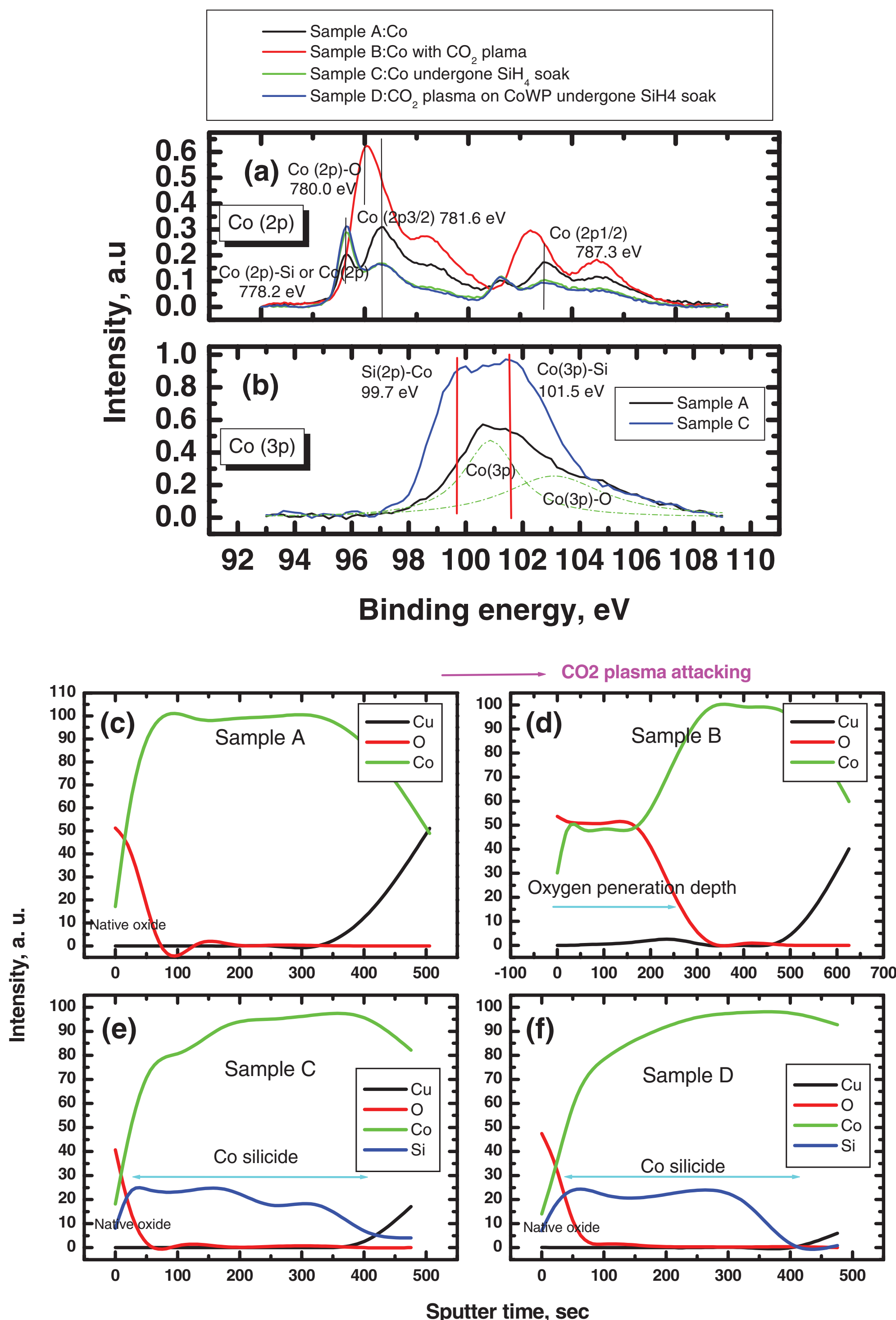

Figure 2. (a)–(b) Co silicide identification by XPS analysis of core level (a) Co(2p)Si (b) Co(3p)Si. (c)–(f) Oxygen resistance: (c) as deposited Co (d) Co-O formed for Co underwent CO_2 plasma treatment (e) as formed Co silicide (f) Negligible Co-O formed for Co silicide underwent CO_2 plasma treatment.

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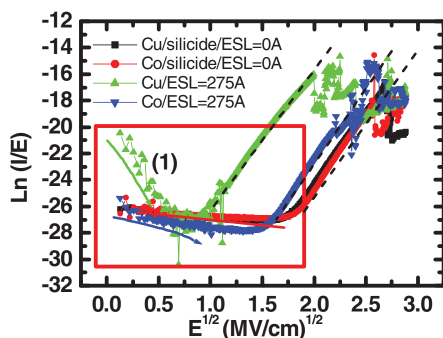

Figure 3. Frenkel-Poole plot, schemes B and C.

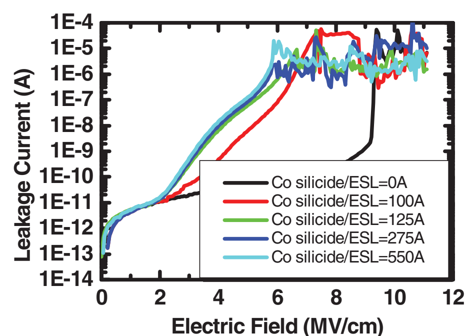

Figure 4. Leakage current vs. electric field, scheme A.

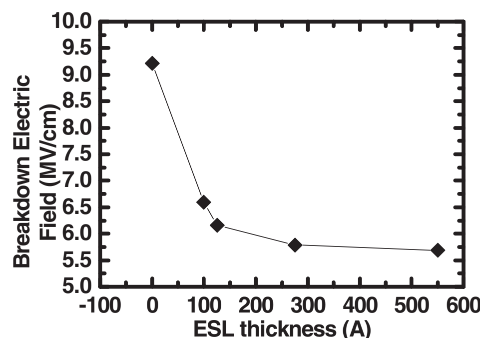

Figure 5. Breakdown electric field vs. ESL thickness.

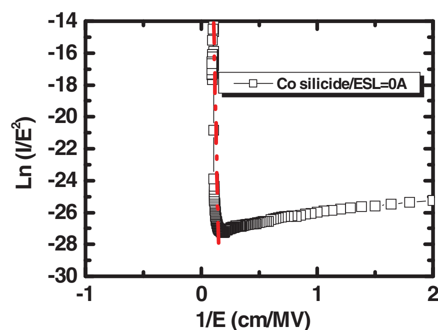

Figure 6. Frenkel-Poole plot, scheme A.

negligible change of Co(2p)-Si and Co(3p)-Si samples that underwent CO_2 attack are investigated. Co following SiH_4 treatment can withstand attack by CO_2 because of an increased oxygen resistance. However, significant Co-O bonding is observed in the Co cap after attack by CO_2. Figures 2c–2f present the XPS depth profiles of samples A, B, C, and D, respectively. Figure 2c shows as-deposited Co cap and Fig. 2d shows Co after attack by CO_2. Significant Co oxidation displays as-deposited Co cap after attack by CO_2 as shown in Fig. 2d. Co silicide demonstrates oxygen resistance because a comparison of Figs. 2e and 2f reveal negligible surface oxidation. With this understanding, a proper SiH_4 treatment has been developed for Cu or Cu/Co materials before dielectric materials deposition to ensure interfacial quality, which explains the reasons that smooth surfaces are achieved for silicide-made interfaces as shown in Figs. 1c and 1d.

The effects of schemes on conduction modes.— Figure 3 plots ln(I/E) against $E^{1/2}$ based on the Frenkel-Poole emission. A linear relationship exists ln(I/E) and $E^{1/2}$ for Cu silicide/ESL = 0 A, Co silicide/ESL = 0 A, Cu/ESL = 275 A and Co/ESL = 275 A at electric field >3.2 MV/cm, >3.2 MV/cm, >0.7 MV/cm and 2.3 MV/cm, respectively. With the application of SiH_4 treatment on Cu or Co metal, the current is confined in the silicide layer because of the higher resistivity compared with pure metal. Therefore, silicide materials efficiently block interfacial conduction and breakdown voltage improves. In the Cu/ESL and Co/ESL schemes at the lower electric field shown in Fig. 3 mark "1", the leakage current declines as when an electric field is applied. The number of trapped Cu ions per unit volume is referred to as defect density. The level of the trapped Cu ions is deeper than the level of trapped electrons, inhibiting the emission of new electrons from traps formed by Cu ions, such that the leakage current drops.[13] The extended low-leakage current of Cu/ESL or Co/ESL in the low electric field is evidence of the presence of more defect sites than generated in the ESL = 0 A scheme. The chemical bonding mismatch between low-k and ESL can produce more defect sites, which are beneficial for subsequent electron or Cu ion generation, contributing to subsequent leakage current. Hence, a lower breakdown field is associated with the addition of ESL.

Figures 4 and 5 with W/S = 0.07/0.07 μm line-line I-E curves and their corresponding electric breakdown fields are obtained to further examine scheme's effects. The dielectric constant k of ILD is 3.1 in this test (low-k, scheme A). The breakdown field decreases monotonically as the ESL thickness increases. The quick breakdown is a factor of 0.7 worse for thin ESL 100 A (VBD = 6.5 MV/cm) than for ESL = 0 A (VBD = 8.5 MV/cm). I-E curves reveal different electric-field-dependent behaviors and show that the conduction mechanisms of samples without ESL and with added ESL differ. It is therefore interesting to note the ESL role on the conduction mode. Figure 6 shows the plot of ln(I/E)-$E^{1/2}$ based on the Frenkel-Poole emission: the current is given by Eq. 1. Two distinct I-E behaviors are observed in a low/high electric field. The low field yields the ohmic characteristic. The ESL in films of 100 A ∼ 500 A thickness are exponentially related to the square root of the field at high electrical field, indicating that the trapped electrons dominate the conduction process. Those trapped electrons can further be conducted in ESL bulk film or along the low-k/ESL interface because ESL with SiCN composition has a lower energy gap (2.5 - 3 eV) than the low-k material (>5 eV). Therefore, SiCN ESL inherently offers an effective path for electrons, which is considered the reasoning for ohmic conduction domination. In contrast, the paradigm of ESL role shifts to Frenkel-Poole emission as thickness decreases. Figure 7 shows the plot of ln(I/E^2) against I/E based on I-E curves. The field emission and the current can be expressed by Eq. 2 to further investigate the conduction mode of ESL = 0 A.[14,15] The negative gradient of the F-N plot confirms that electron emission is attributed to electron tunneling through a positive work function barrier. The high breakdown field for ESL = 0 A (greater than the SiCOH intrinsic breakdown field 8 MV/cm) is considered be negligible electron path conduction from ESL, Co silicide implantation with higher electrical potential is achieved and is responsible for negligible interfacial Co silicide /low-k surface defects.

$$\text{Frenkel}-\text{Poole} \quad \sim V\exp(+2a\sqrt{V}/T - q\phi_B/KT) \qquad [1]$$

$$\text{Fowler}-\text{Nordhiem} \quad \sim V^2\exp(-b/V) \qquad [2]$$

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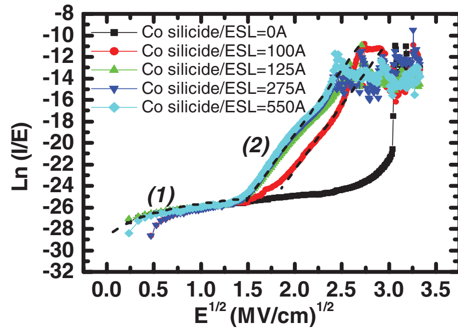

Figure 7. Fowler-Nordheim plot of Co/ESL = 0 A.

Weibull VBD and TDDB analysis.— Among parameters such as ESL thickness, the k value of low-k materials, and the capping materials, it is interesting to note the mutual interaction among final TDDB performance. To ensure fewer interfacial defects to act as additional defect sites for electron transportation, Co or Cu with post- SiH_4 treatment was used. The T63.2% VBD and TDDB Weibull intrinsic performance improved as the ESL thickness decreased. However, less low-k materials dependency is confirmed from VBD comparisons of low-k A/B using the same technology node. The T63.2% of time to failure shows approximately 10 X/100 X improvement when comparing ESL = 0 A to the ESL = 125 A/550 A. Figures 8a and 8b compare T63.2% of time to failure Weibull breakdown voltage (VBD) and time-to-dielectric-breakdown (TDDB) (scheme A). The ESL correlation to VBD and TDDB is seen as well as the schemes A. The T63.2% of time to failure shows approximately 10X/25X improvement when comparing ESL = 0 A to ESL = 100 A/275 A. Cu/ESL is more ESL-thickness-sensitive than Cu/Co/ESL when considering electron barrier modification with Co cap application. Figures 8c and 8d compare the T63.2% of time to failure Weibull VBD and TDDB (schemes B and C), respectively. It is interesting to note the failure mode Co cap for ESL or ESL free processes because the TDDB failure mode application was widely discussed with ESL but insufficient researched for the ESL-free scheme. The first earlier failures for Co/ESL and Co silicide/low-k at 1.5MV/cm and 3MV/cm are shown in Figs. 9a and 9b. The sample without ESL application is able to withstand higher breakdown voltage compared to ESL application one, which is consistent with the TDDB result. Lower electric field in the earlier failure observed for CoWP/ESL proves ESL appearance favoring the electron conduction. The failure modes of both samples are similar showing Cu extrusion at corner sites due to the highly

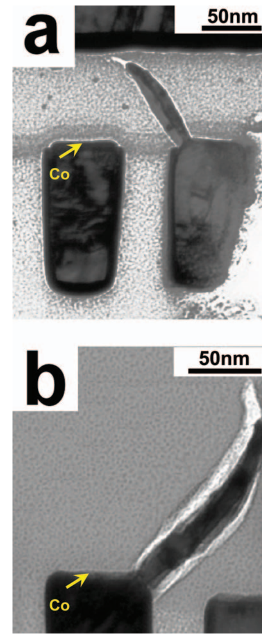

Figure 9. (a) TEM sample of Co/ESL/low-k stressed at 1.5 MV/cm. (b) TEM sample of Co/low-k stressed at 3 MV/cm.

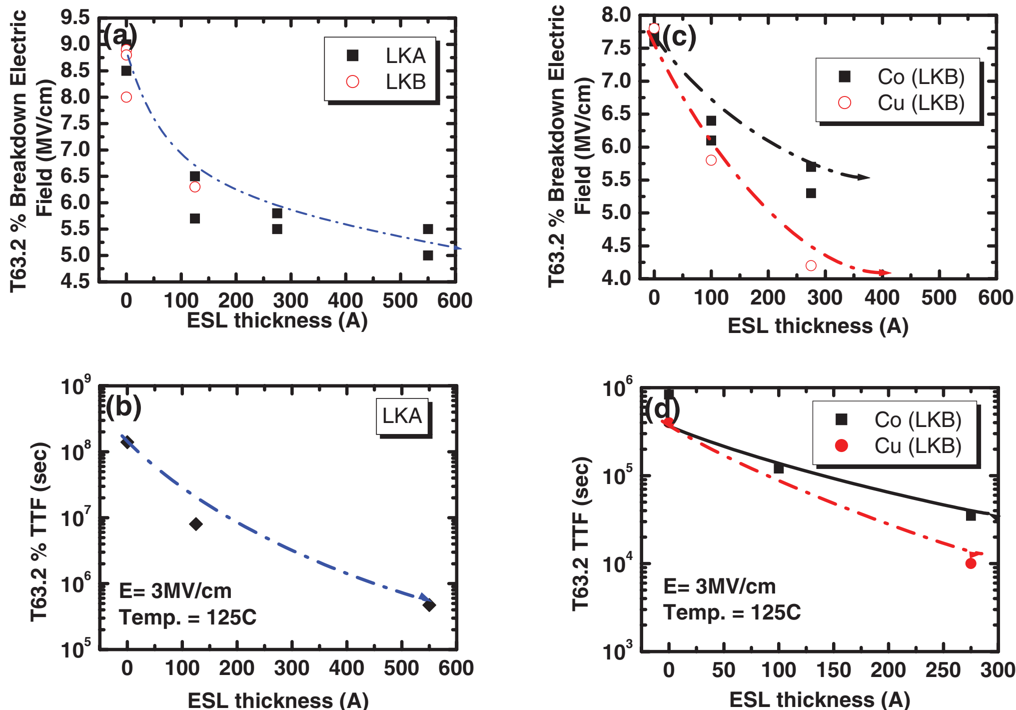

Figure 8. (a) T63.2% VBD vs. ESL film in varied thickness, scheme A. (b) T63.2% TTF vs. ESL film in varied thickness, scheme A. (c) T63 VBD vs. ESL film in varied thickness, schemes B and C. (d) T63 TTF vs. ESL film in varied thickness, schemes B and C.

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effective stress field. The effectiveness of the ESL-less scheme for TDDB improvement is concluded.

Conclusions

The leakage current and breakdown field depend on thickness of ESL. The lower energy gap of ESL than that of low-k materials provides a path for transportation of electrons. Both low-k/ESL interface and reduction of the conductivity of ESL bulk film are critical to improving the lifetime of TDDB. The mechanism of TDDB improvement is considered to involve modification of the metal/low-k electrical potential, negligibility of interfacial low-k/low-k surface defects and ESL-less application.

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