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Investigation on amorphous InGaZnO based resistive switching memory with low-power, high-speed, high reliability

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ABSTRACT

Recently, non-volatile memory (NVM) has been widely used in electronic devices. Nowadays, the prevailing NVM is Flash memory. However, it is generally believed that the conventional Flash memory will approach its scaling limit within about a decade. The resistive random access memory (RRAM) is emerging as one of the potential candidates for future memory replacement because of its high storage density, low power consumption as well as simple structure.

The purpose of this work is to develop a reliable a-InGaZnO based resistive switching memory. We investigate the resistive switching characteristics of TiN/Ti/IGZO/Pt structure and TiN/IGZO/Pt structure. The device with TiN/Ti/IGZO/Pt structure exhibits stable bipolar resistive switching. The impact of inserting a Ti interlayer is studied by material analyses. The device shows excellent resistive switching properties. For example, the DC sweep endurance can achieve over 1000 times; and the pulse induced switching cycles can reach at least 10,000 times. Furthermore, the impact of different sputtering ambience, the variable temperature measurement, and the conduction mechanisms are also investigated. According to our experiments, we propose a model to explain the resistive switching phenomenon observed in our devices.

1. Introduction

Non-volatile memory (NVM) can retain stored data even when not powered. NVMs are extensively used in electronic products, such as MP3 players, cell phones, and laptops. Nowadays, most commercially available NVM is Flash memory. However, as transistors have continued to be scaled down into the nano-scale region, Flash memory is widely believed to have reached its physical limit: the continuous shrinking of the tunneling oxide results in a larger leakage current, making the storage of charge in the floating gate increasingly difficult. Additionally, Flash lacks several of the required features of ideal universal memory — especially a low power consumption and a short programming/erasing time. Therefore, various novel non-volatile memory devices, such as magnetoresistive random-access memory (MRAM), ferroelectric RAM (FeRAM), phase change memory (PCM) and resistive random-access memory (RRAM), have been proposed as alternatives with increased capacity. Among all potential replacements, RRAM is the most promising owing to its small size (4 F^2), low programming voltage (~1 V), high operating speed (~ns) and a potential for 3D stacking. Recently, some research has demonstrated that adding a Ti interlayer between the top electrode and the dielectric improves the electrical performance of RRAM devices [1,2]. Owing to the ability of Ti to get oxygen ions, the oxygen concentration of the dielectric may be reduced, resulting in the formation of TiO_x at the interface and very many oxygen vacancies in the dielectric. This work proposes a device with the structure TiN/Ti/InGaZnO/Pt and compares its electrical properties with that of a device without a thin Ti layer. InGaZnO (IGZO) was chosen as the resistive switching layer because the materials can serve as both the switching medium for the memory and the active material in thin film transistors (TFTs), attracted substantial interest. IGZO has the key features of high carrier mobility, ability to be deposited at low temperature and high optical transparency. Furthermore, this material is emerging as the favored candidate material for active channel layers in next-generation TFTs in AMLCDs and AMOLEDs [3]. The IGZO RRAM has the potential to be integrated with IGZO TFT periphery circuits in flat panel displays to realize systems-on-panels (SoP).

2. Experimental details

First, a 20 nm titanium dioxide (TiO_2) adhesion layer and a 60 nm platinum layer were deposited on a SiO_2/Si substrate by e-gun evaporation to form a Pt/TiO2/SiO2/Si structure. After the Pt bottom electrode had been deposited, a 50 nm-thick IGZO film was deposited using a magnetron sputtering system and patterned by shadow masks with a diameter of 200 μm. The IGZO target was sputtered in ambient Ar at room temperature. Finally, a thing 10 nm-thick titanium (Ti) oxygen-gettering layer and a 70 nm-thick TiN layer were also deposited using

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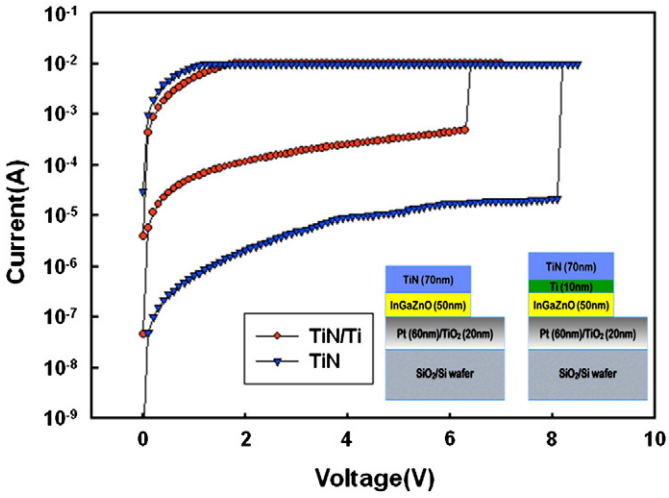

Fig. 1. Comparison between the TiN/Ti/IGZO/Pt structure and the TiN/IGZO/Pt structure.

a sputtering system. The process flow for the fabrication of the TiN/IGZO/Pt structure was almost the same as that for the TiN/Ti/IGZO/Pt structure, but without the deposition of the Ti layer. After the device had been fabricated, electrical measurements were made using a Keithley 4200 semiconductor parameter analyzer, a probe station with a temperature controller and a dual-channel pulse generator card, to examine its electric-pulse-induced resistance (EPIR) switching behaviors. Microstructural investigations were performed using a transmission electron microscope (TEM). X-ray photoelectron spectroscopy (XPS) was utilized to analyze the compositions of the films.

3. Results and discussion

Fig. 1 shows the process of formation of the TiN/Ti/IGZO/Pt structure and the TiN/IGZO/Pt structure. As can be seen, the structure with the Ti interlayer has a smaller initial resistance because the Ti forms oxygen vacancies. Additionally, TiN/Ti/IGZO/Pt structure exhibits stable resistive switching properties with a lower forming voltage and a higher yield than the TiN/IGZO/Pt structure.

To further analyze resistive switching, a cross-sectional transmission electron microscopic (TEM) image of the TiN/Ti/IGZO/Pt structure was obtained and shown in Fig. 2(a). According to the TEM image, the thickness of IGZO was approximately 40 nm and an interfacial layer (~2 nm) was formed between Ti and IGZO, perhaps because of a reaction between the easily oxidizable Ti and the IGZO thin film. As suggested elsewhere [4], the resistance switching is believed to be related to this interfacial layer. To identify this layer, XPS analysis was carried out. Fig. 2(b) displays the O 1s core level spectra, including a lattice peak (530.8 eV) and an additional peak (531.5 eV), which indicate a high content of non-lattice oxygen ions in the Ti/IGZO interface [5–7].

After the forming process, the resistive switching phenomenon of the device was observed. Fig. 3(a) presents the typical bipolar switching behavior of the TiN/Ti/IGZO/Pt device under dc sweeping. When a swept voltage from 0 to 2.5 V was applied to the TiN top electrode (indicated by arrow "1" in the figure), the device changed from the high-resistance state (HRS) to the low-resistance state (LRS) with a compliance current (I_{CC}) of 10 mA at around 1 V (V_{SET}). I_{CC} prevents the abrupt jump in the current from becoming an irrecoverable breakdown. As the applied voltage is swept from 2.5 to 0 V (indicated by arrow "2" in the figure), the device remained in the LRS. Then, the applied voltage was swept to −2.5 V (indicated by arrow "3" in the figure), and device changed from the LRS to the HRS at about −1.5 V (V_{RESET}). The HRS was maintained as the applied voltage was swept from −2.5 to 0 (indicated by arrow "4" in the figure). The endurance of the device was tested by sweeping the DC voltage to switch the RRAM, by repeating the aforementioned cycle (arrow numbers 1 to 4). Fig. 3(b) plots the read-out resistance at 0.3 V versus voltage sweeping cycle. The resistance ratio (R_{HRS}/R_{LRS}) exceeds 10, and the resistance remains stable even after 1000 switchings. To determine whether the device can endure more uses, a dynamic pulse operation is performed: "set" and "reset" pulses are used separately to find the width and amplitude of pulses that effectively change the resistance states. The pulses used to switch the device to LRS and HRS were 100 ns, 3.4 V and 100 μs, −2.5 V, respectively. Fig. 3(c) shows the AC endurance. Reversible resistive switching is conducted up to 10,000 times and the R_{HRS}/R_{LRS} ratio is approximately 10.

Oxygen vacancies are known importantly to affect the electrical performance of the IGZO film. According to some investigations [8–10], oxygen vacancies influence the leakage current of device. If the HRS current can be reduced, then the resistive ratio of the device can be improved. Hence, TiN/Ti/IGZO/Pt RRAMs were fabricated using various partial pressures of oxygen in the Ar + O_2 ambient to sputter the IGZO target. The fabrication process flows were otherwise identical. The proportions of oxygen in the Ar + O_2 ambient were 0%, 20% and 33%. The results in Fig. 4(a) reveal that as the oxygen partial pressure was increased, the HRS becomes less conductive, so the memory window became larger. As the oxygen concentrations were increased, the R_{HRS}/R_{LRS} ratios were 24, 48 and 161, respectively. However, the SET voltage increased with the oxygen concentration. Therefore, the use of a stronger electric field to switch the device causes the device to become unstable after fewer switchings (Fig. 4(b)), causing it to fail. In 0% oxygen, the device retains stable resistive switching for at least 50 cycles

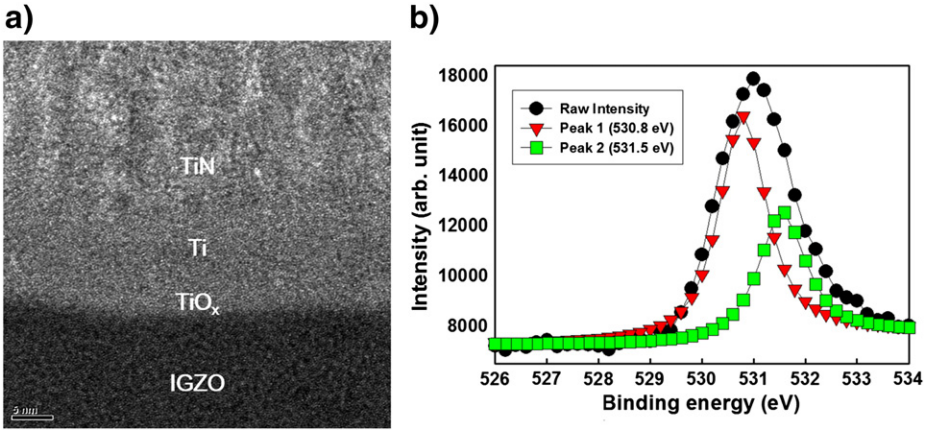

Fig. 2. (a) The cross-section TEM image of the TiN/Ti/IGZO/Pt device. (b) XPS O 1 s core level spectra of the Ti/IGZO interface.

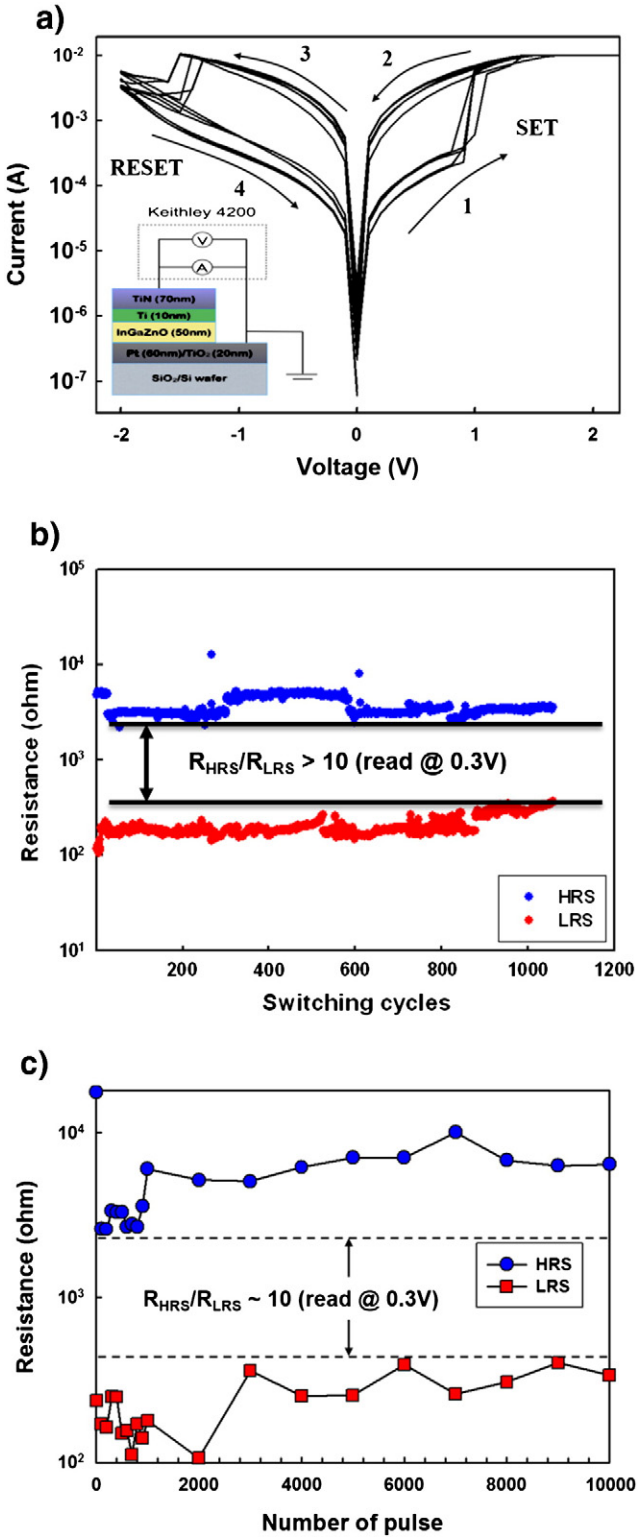

Fig. 3. (a) 1000 I–V curves from the TiN/Ti/IGZO/Pt device, which show typical bipolar resistance switching characteristics. The inset shows a schematic diagram of the memory device. (b) The DC endurance at room temperature. (c) Endurance test of the device by continuous pulses operation.

(Fig. 4(c)). A trade-off must be made between the R_{HRS}/R_{LRS} ratio and stability.

Current fitting is performed to give and to provide insight into the mechanisms of conduction. Fig. 5 plots the current versus voltage for the SET process on a double logarithmic scale. In the low-voltage region, the slope is close to one in both the HRS and the LRS so the conduction mechanism in the low-field region is believed to be Ohmic behavior. In the higher electric field, the I–V data obtained in the LRS yield a strong linear relationship. However, the I–V relationship is nonlinear in the high electric field in the HRS. This nonlinear I–V characteristic passes through various regimes, from $I \propto V$ (slope = 1.16, Ohmic behavior), through $I \propto V^2$ (slope = 2.04, trap-filled-limited region), followed by a steep increase in current, to a $I \propto V^2$ again (slope = 2.07, trap-filled region). This behavior indicates that the conduction mechanism was trap-controlled SCLC [11]. At a low applied voltage, the density of the thermally generated free carriers in the IGZO films exceeded that of the injected carriers, leading to Ohmic conduction. When the density of injected carriers became dominant, $I \propto V^2$. In this regime, shallow traps were gradually filled. In the second $I \propto V^2$ regime, all traps had been occupied; most the injected carriers were free carriers, and the device switched to the LRS.

The thermal dependence of the measurements was also discussed. The resistive switching properties of the device at different temperatures – 25 °C, 40 °C, 55 °C, 70 °C, 85 °C, 100 °C and 120 °C – were also measured. Fig. 6 shows the statistical data concerning the HRS and the LRS at these temperatures. The LRS current depended on temperature, while the HRS current shows indecently on temperature. The LRS current increased with temperature. A positive resistance temperature coefficient of $4.67 \times 10^{-3}\ K^{-1}$ was obtained, confirming conduction behavior like that of a metallic filament in the IGZO-based RRAM, revealing that these conductive filaments may have been composed of metal atoms. Based on the above experimental results, the resistive switching model of the TiN/Ti/IGZO/Pt structure that is presented in Fig. 7, was proposed. Some oxygen vacancies are initially present in the IGZO film. After the forming process, more oxygen vacancies in IGZO were produced, activating resistance switching. The inset in Fig. 7 shows the "SET" process in which a positive bias is applied to the TiN top electrode, producing a downward electric field, causing the O^{2-} ions move into the Ti layer, and oxidize at the anode. The Ti layer serves as an oxygen reservoir. Meanwhile, the metal ions (oxygen vacancies) drift or diffuse to the bottom electrode Pt, and are reduced at the cathode. The metal atoms may accumulate from the cathode to the anode, forming conducting filaments (such that the device is in the LRS). The inset in Fig. 7 also shows the RESET process. The application of a negative bias to the top electrode generates an upward electric field and the reverse redox process occurs. The oxygen ions migrate back to the IGZO film and recombine with the metal ions, which are oxidized, causing the conducting filaments partially to rupture near the Ti layer, switching the resistance state of the device from the LRS to the HRS.

4. Conclusion

A reliable a-InGaZnO-based resistive switching memory was fabricated, with a Ti interlayer inserted both to improve the stability of the resistive switching properties and the yield, owing to the formation of a TiO_x interlayer, according to material analysis. The device exhibits excellent resistive switching properties, including stable DC sweep endurance, long data retention, and fast pulse switching. The effects of sputtering ambient, the temperature, and conduction mechanisms of current transport were investigated. Based on the experimental results, a resistive switching model was proposed.

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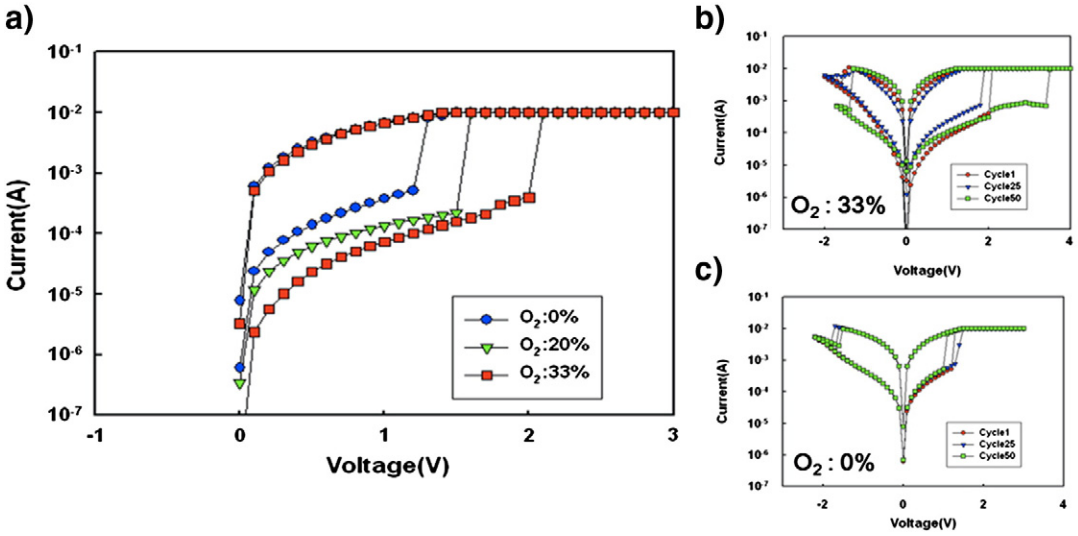

Fig. 4. (a) The SET process I–V curves of IGZO films deposited in 0%, 20% and 33% oxygen partial pressure ratios. The resistance switching I–V curves with multiple cycles of the IGZO films deposited in (b) 33% oxygen partial pressure ratios and (c) 0% oxygen partial pressure ratios.

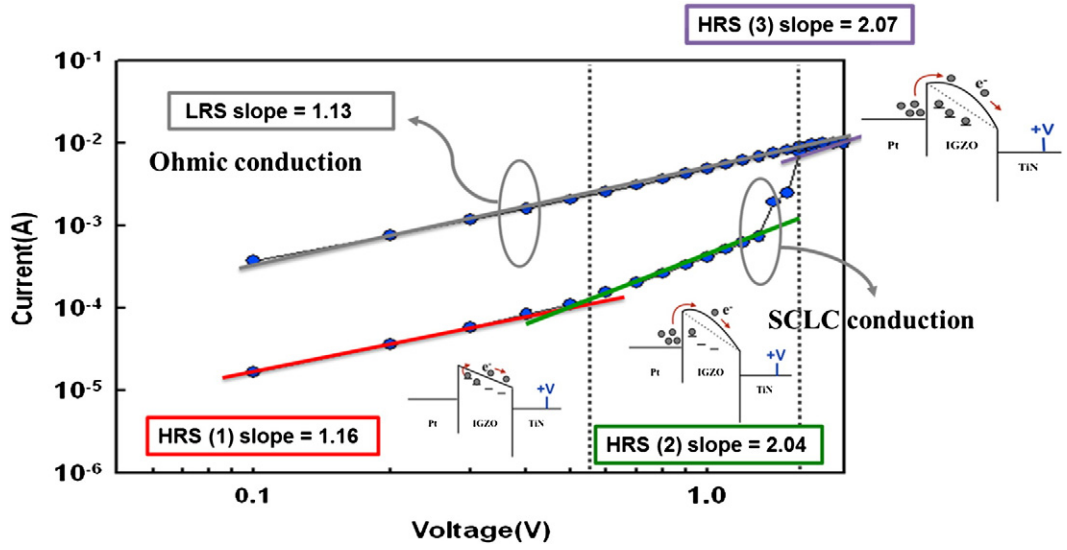

Fig. 5. The I–V characteristics of the TiN/Ti/IGZO/Pt device in log-log scale, indicating the Ohmic conduction in the LRS, while SCLC conduction fitting in the HRS.

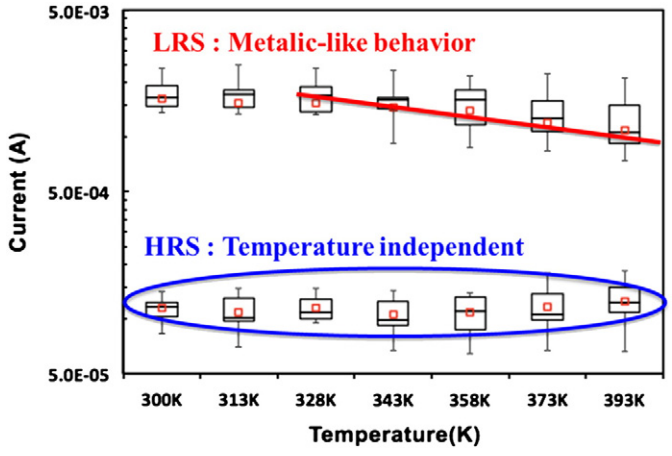

Fig. 6. The resistance read at 0.3 V in both LRS and HRS with different temperatures.

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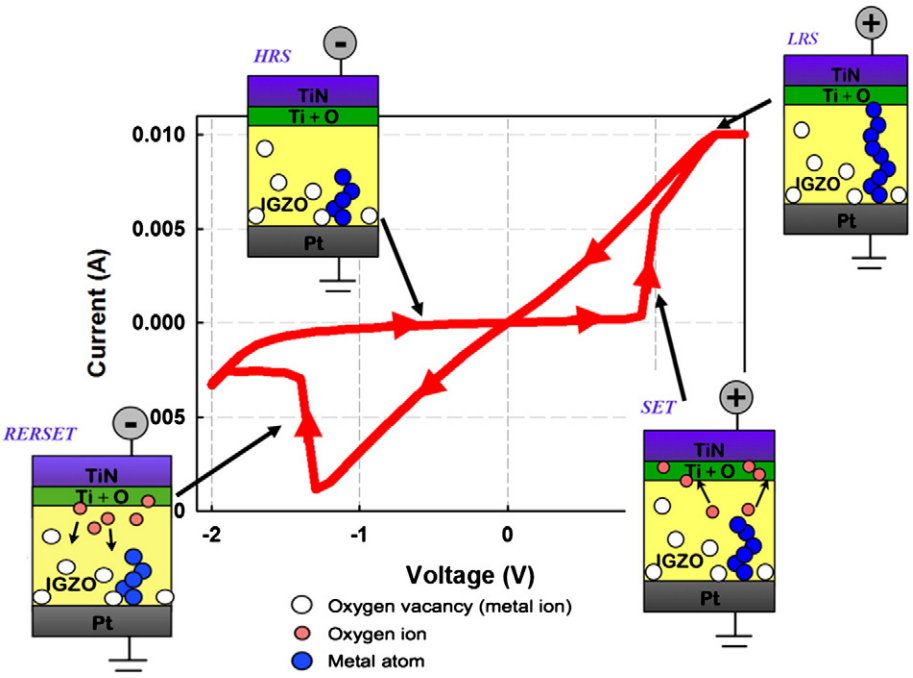

Fig. 7. Schematic diagram of proposed resistive switching mechanism. Including the LRS, HRS, SET process, and RESET process.