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Assessment of Thermal Impact on Performance of Metamorphic High-Electron-Mobility Transistors on Polymer Substrates Using Flip-Chip-on-Board Technology

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In this study, we have fabricated and characterized an $In_{0.6}Ga_{0.4}As$ metamorphic high-electron-mobility transistor (mHEMT) device packaged using flip-chip-on-board (FCOB) technology. A low-cost polymer substrate was adopted as the carrier for cost-effective purposes. The impact of bonding temperature on the device performance was also experimentally investigated. While the DC performance was not as sensitive, serious degradation in RF performance was observed at high bonding temperature. Such degradation was mainly due to the thermal-mechanical stress resulting from the mismatch in the coefficient of thermal expansion (CTE) between the GaAs chip and the polymer substrate. Quantitative assessment was also performed through equivalent circuit extraction from *S*-parameter measurements.

The rapidly growing demands on the data bandwidth and transmission speed of modern wireless communication systems have pushed the operating frequencies to millimeter-wave range or beyond.[1–3] Such trend has also accelerated the development of device fabrication as well as packaging technologies to meet the stringent requirements for high-frequency operations. On the device side, metamorphic high-electron-mobility transistor (mHEMT) technology with indium-rich channels has been attractive due to the very high electron mobility and saturation velocity of InGaAs materials.[4–7]

The development of packaging configuration and interconnect technologies has become critical since both high performance and cost effectiveness are the main focuses of modern applications. Instead of the conventional wire-bonding technology, flip-chip interconnection is considered favorable at high frequencies due to its features of shorter interconnection length, better thermal management, better mechanical stability, and smaller packaging size.[8–16] Additionally, the flip-chip-on-board (FCOB) technology is a very cost-effective solution for high-frequency applications because it bypasses chip-level assembly, which makes it easier for further integration with other components in the system.[17–21] Therefore, such technology not only reduces RF loss but also saves material cost from the elimination of the chip level package. Table I lists the material properties of some conventional substrates for millimeter-wave applications. Clearly, the commercial RO 3210 organic substrate from Rogers Corporation™ is a good candidate due to its very low cost with comparable material properties at high frequencies. Giesler et al. and O'Malley et al. had successfully demonstrated the flip-chip structure on FR4 organic substrate by using 97Pb/3Sn solder bump interconnection and the reliability improvement of the flip-chip interconnect with encapsulation.[17,18] Hsu et al. demonstrated the flip-chip structure on the RO 3210 organic substrate with epoxy-based underfill to work up to 50 GHz and pass the 600-cycle thermal-cycling test.[19] The characteristic of the flip-chip-packaged HEMT device on the RO 3210 organic substrate with epoxy-based underfill injection has been reported up to W band in our previous work.[20] While previous research effort was devoted mostly to the electrical performance of the FCOB technology, the impact of the bonding temperature on the device performance after packaging has not been investigated.

Table I. Material properties of the substrates commonly used for flip-chip packaging.

Material	Dielectric constant (at 10 GHz)	Loss tangent (at 10 GHz)	CTE (ppm/K)	Cost in USD ($2'' \times 2''$)
Si	11.9	0.001	2.5	2.3
GaAs	12.9	0.0005	5.4	88
Al_2O_3	9.8	0.0002	6.3	25
RO3210	10.2	0.0027	13	2.5

In this study, a flip-chip-packaged 150 nm $In_{0.6}Ga_{0.4}As$ mHEMT on low-cost RO 3210 polymer substrate using FCOB technology is demonstrated. We have characterized the packaged device under different bonding temperatures through the DC and RF measurements up to 110 GHz. Degradations in RF performance were observed due to the stress from the coefficient of thermal expansion (CTE) mismatch between the materials during the bonding process. Further assessment of the thermal effect during the bonding process was performed through equivalent circuit extraction of the solder bumps at different temperatures. Results revealed that minimum degradations in RF performance up to 100 GHz could be achieved with the appropriate bonding temperature.

We adopted the in-house-fabricated 150 nm $In_{0.6}Ga_{0.4}As$ mHEMT as the primary device in this study. The HEMT structure was grown on a 3″ semi-insulating GaAs substrate by molecular beam epitaxy (MBE). The high indium content in the $In_xGa_{1-x}As$ channel layer will improve the RF performance of the device. A Pt-based buried gate was adopted to minimize the gate-to-channel distance without increasing the access resistance and, in the meantime, to suppress the short-channel effect. The fabrication process of the $In_{0.6}Ga_{0.4}As$ mHMET device has been described in a previous publication.[22]

Figure 1 shows the in-house fabrication process of the FCOB structure on the RO 3210 polymer substrate. The commercial RO3210™ PCB of 0.635 mm thickness from Rogers Corporation was used as the substrate material. Compared with the conventional Al_2O_3 substrate commonly used for the flip-chip process, the RO3210 substrate exhibits great competitiveness in terms of the very low cost. For both electrical and mechanical performance improvements, chemical mechanical polishing (CMP) was first applied to reduce the

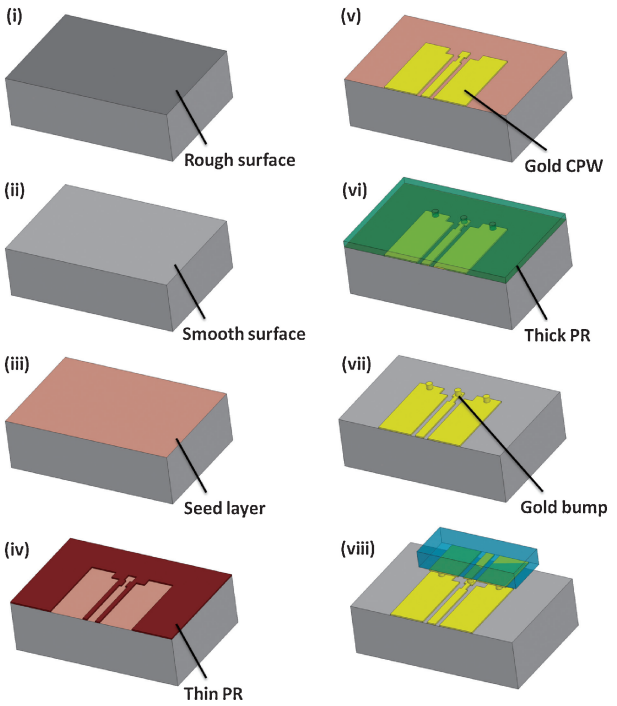

Fig. 1. In-house fabrication of FCOB structure on RO 3210 polymer substrate.

Table II. Bonding conditions at high and low substrate bonding temperatures.

Condition	Chip temp. (°C)	Substrate temp. (°C)	Bonding force (g)	Duration (s)
High temp.	200	200	80	200
Low temp.	200	100	100	240

surface roughness of the polymer substrate. After the CMP process, the surface roughness of the polymer substrate was improved from 3 to less than 1 μm by using a P-10 Surface Profiler. In the beginning of the RO 3210 substrate process, the Ti/Au seed layer was firstly evaporated on the RO 3210 substrate. The CPW transmission line of 3 μm thickness was patterned by Au electroplating. To obtain good RF performance of the FCOB structure, the CPW transmission line with compensation design has been considered in Ref. 20. Then, the thick photoresist from TOK Company was patterned for the Au microbump electroplating. The height and diameter of the Au microbumps are 20 and 50 μm, respectively. Finally, the mHEMT device was flip-chip packaged onto the RO 3210 polymer substrate by using an M9 flip-chip bonder.

During the bonding process, both the device and substrate were heated before adhesion to establish a solid contact with the interconnection, and then cooled to room temperature. Thus, the existence of the mechanical stress due to the mismatch in CTE between the materials is unavoidable. To investigate the thermal impact on the device during the bonding process, two different flip-chip bonding conditions were applied as summarized in Table II. For the case of high bonding temperature, the optimized bonding force and bonding time were 80 g and 200 s, respectively. A higher bonding force of 100 g and a longer bonding time of 240 s

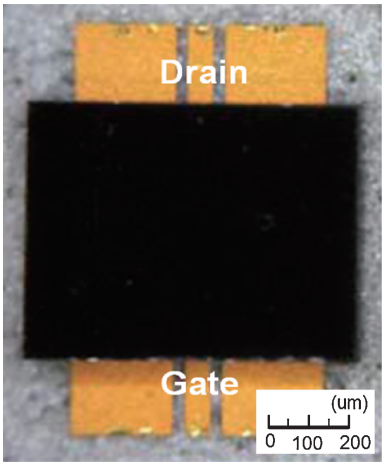

Fig. 2. Photograph of the device flip-chip bonded onto RO3210 substrate.

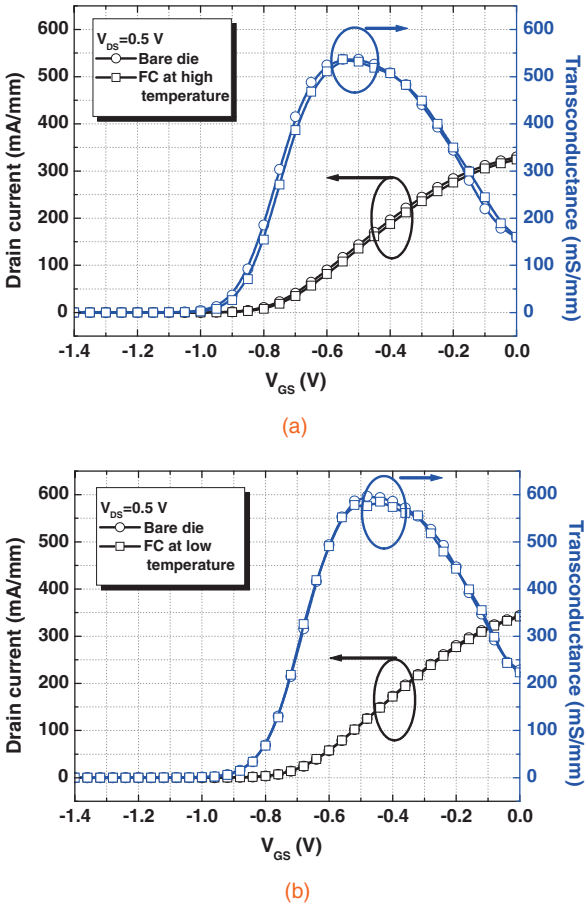

Fig. 3. Measured drain current and DC transconductance as functions of gate bias at $V_{DS} = 0.5$ V of the flip-chip-packaged device under different bonding conditions, (a) with high bonding temperature and (b) with low bonding temperature, with those of bare dies included for comparison.

were applied to maintain good connection between the Au bumps and Au pads in the case of low bonding temperature. Figure 2 shows the photograph of the device flip-chip bonded onto the RO3210 substrate.

Figures 3(a) and 3(b) show the measured drain current and DC transconductance as functions of gate bias at $V_{DS} = 0.5$ V of the flip-chip-packaged device under different bonding conditions with those of bare dies included for com-

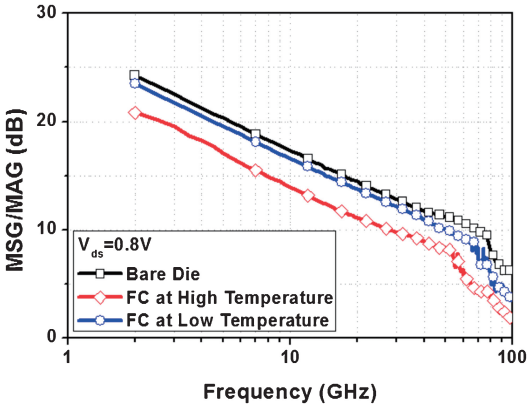

Fig. 4. Measured MSG/MAG as a function of frequency for the cases of bare die, flip-chip-packaged device with high bonding temperature, and flip-chip-packaged device with low bonding temperature.

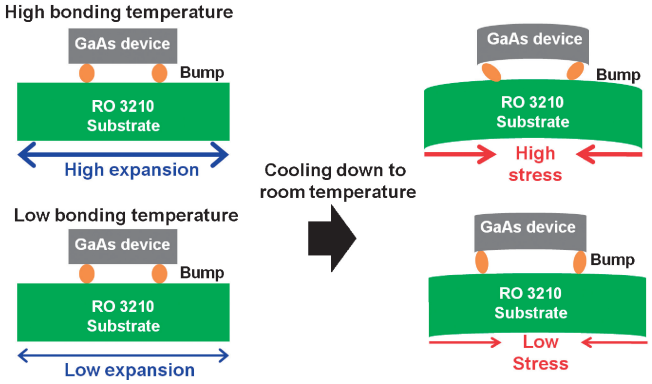

Fig. 5. Illustration of induced mechanical stress during bonding process with different bonding temperatures.

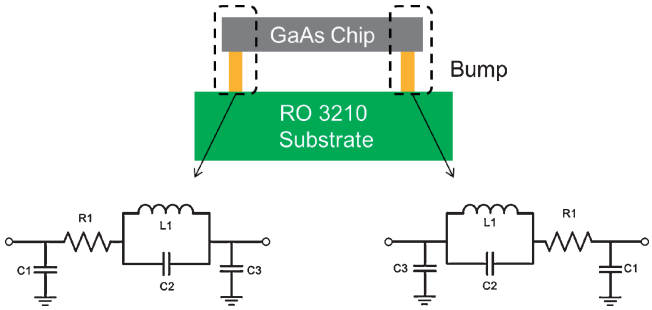

Fig. 6. The corresponding equivalent circuit model of the bump interconnect.

parison. It is clear that the DC characteristics for both cases are identical to those of bare dies without any degradation. The RF performance was characterized from 2 to 110 GHz by using an HP 8510XF network analyzer with E7352 test heads calibrated by using a standard load-reflection-reflection-match method. Figure 4 plots the maximum stable gain/maximum available gain (MSG/MAG) as a function of frequency for the cases of bare die, flip-chip-packaged device with high bonding temperature, and flip-chip-packaged device with low bonding temperature. Note that the input and output terminations were set to 50 Ω during the measurement. As is observed, a 5 dB drop in the low-frequency regime occurs for the case with high bonding temperature. In contrast, a very slight degradation of only 0.5 dB at 50 GHz is observed for the case of low bonding temperature. We believe that such degradation should be related to the CTE mismatch between RO 3210 (13 ppm/K) and GaAs (5.4 ppm/K). An intuitive interpretation is shown in Fig. 5. Apparently, the RO3210 substrate undergoes higher expansion during the heating process, leading to higher stress level once cooled to room temperature.

To further assess the mechanism causing the RF degradation, we patterned 50 Ω transmission lines on GaAs and flip-chip bonded onto the RO3210 substrate using exactly the same conditions listed in Table II. Procedures outlined in Ref. 23 were adopted to extract the equivalent circuit of the bump interconnection through *S*-parameter measurement. Figure 6 shows the corresponding equivalent circuit model of the bump interconnect. In the equivalent circuit model, C1 and C3 represent the discontinuity capacitances at the RO3210 substrate and the GaAs chip, respectively. R1, L1, and C2 represent the parasitics along the signal path. To determine the *S*-parameters of the bump interconnect, we first patterned 50 Ω CPW transmission lines on GaAs substrate and measured the *S*-parameters. Then, the transmission line was flip-chip bonded onto RO3210 polymer substrate using the conditions outlined in Table II. Finally, the *S*-parameters of the complete structure were measured. The *S*-parameters of the overall structure in Fig. 6 can be obtained by cascading the individual *S*-matrices as

$$[S^{\mathrm{Total}}] = \begin{bmatrix} S^{\mathrm{b}}_{11} & S^{\mathrm{b}}_{12} \\ S^{\mathrm{b}}_{12} & S^{\mathrm{b}}_{22} \end{bmatrix} [S^{\mathrm{CPW}}] \begin{bmatrix} S^{\mathrm{b}}_{22} & S^{\mathrm{b}}_{12} \\ S^{\mathrm{b}}_{12} & S^{\mathrm{b}}_{11} \end{bmatrix}, \quad (1)$$

where $[S^{\mathrm{Total}}]$ and $[S^{\mathrm{CPW}}]$ are obtained through direct measurement with proper reference plane defined. The remaining unknown matrix elements in the above equation can be solved by the following set of equations:

$$S^{\mathrm{T}}_{11} = (S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{22} + S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{12})S^{\mathrm{C}}_{11} + (S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{22} + S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{12})S^{\mathrm{C}}_{12}, \quad (2)$$

$$S^{\mathrm{T}}_{12} = (S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{12} + S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{12})S^{\mathrm{C}}_{11} + (S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{12} + S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{11})S^{\mathrm{C}}_{12}, \quad (3)$$

$$2S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{12}S^{\mathrm{C}}_{11} + (S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{12} + S^{\mathrm{b}}_{11}S^{\mathrm{b}}_{11})S^{\mathrm{C}}_{12} = 2S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{22}S^{\mathrm{C}}_{11} + (S^{\mathrm{b}}_{12}S^{\mathrm{b}}_{12} + S^{\mathrm{b}}_{22}S^{\mathrm{b}}_{22})S^{\mathrm{C}}_{12}. \quad (4)$$

In the above equations, elements with superscript "C" are related to the CPW transmission line on GaAs chip while those with superscript "T" are related to the overall structure. Conversion of the *S*-parameters of the bump interconnect to the *Y*-parameters was then performed to extract the component values as outlined in Ref. 23. Figure 7 shows the modeled and measured *S*-parameters at high bonding temperature. Good agreement over the entire frequency range was achieved. Table III lists the extracted component values corresponding to the two bonding conditions. As observed, the case with higher bonding temperature yields to higher parasitic levels which is related to the larger mechanical stress induced during the bonding process. Such increase in the parasitic levels should be the main reason to result in the degradation in RF performance.

We have investigated the impact of bonding temperature on the performance of a 150 nm $In_{0.6}Ga_{0.4}As$ mHEMT device packaged onto RO3210 polymer substrate using FCOB technology. While the DC characteristics remained identical to those of bare dies for both cases, RF degradation was observed for the case of high bonding temperature.

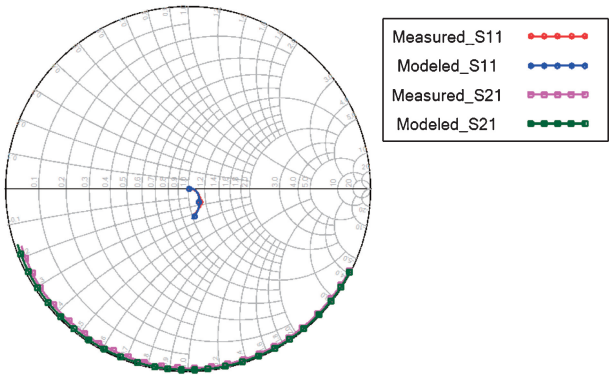

Fig. 7. Measured and modeled *S* parameters of the complete structure in Fig. 6 at high bonding temperature.

Table III. Extracted parasitic values at high and low bonding temperatures.

Condition	R1 (Ω)	L1 (pH)	C1 (fF)	C2 (fF)	C3 (fF)
High temp.	0.62	49	12	200	2.4
Low temp.	0.42	25	7.2	95	0.2

Higher parasitic levels of the bump interconnections have been observed through the extraction of the equivalent circuit for the case of higher bonding temperature. Such increase is related to the higher induced stress level during the bonding process, which leads to the degradation in RF performance.

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