A Low-Cost DC-to-84-GHz Broadband Bondwire Interconnect for SoP Heterogeneous System Integration

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***Abstract*—A low-cost broadband bondwire interconnect is proposed for heterogeneous system integration. Transmission lines are incorporated with bondwires to form a two-path structure, which can effectively reduce the bondwire effect. Theoretical analysis is provided using a graphical method and it shows that the interconnect can give widest operation bandwidth from dc up to a maximum frequency $f_{\max}$ if the length of the transmission lines is designed at an optimal electrical length $\theta_{\max}$. In particular, $\theta_{\max}$ only depends on the characteristic impedance of the transmission lines. The achievable $f_{\max}$ is limited by the bondwire inductance, i.e., smaller bondwire inductance is preferred to have wider operation bandwidth. An interconnect from a 0.18-μm CMOS chip to a glass-integrated-passive-device carrier is designed to verify the proposed concept. Measured results show that the insertion loss and the return loss can be better than 3.0 and 13.4 dB, respectively, from dc to 84 GHz. The proposed interconnect shows around 3.2 times bandwidth of a single bondwire alone. To the best of authors' knowledge, this work demonstrates the bondwire interconnect with the widest operation bandwidth for heterogeneous system integration by using system-on-package reported thus far.**

***Index Terms*—Bondwire, broadband, heterogeneous integration, interconnect, system-on-package (SoP), transmission lines.**

I. Introduction

APPLICATIONS at millimeter-wave frequencies, such as high-speed data communications, automobile radar systems, ultra-wideband personal area networks, and passive imaging, have ignited intensive research activities in recent years [1]–[7]. It is the trend to realize these systems entirely in CMOS technology for low cost and high integration. System-on-a-chip (SoC) is widely chosen for system integration. However, designing high-frequency circuits in CMOS technology is challenging because of lossy silicon substrate and low supply voltage. Besides, SoC may not be a good choice as bulky passive components, e.g., antennas, are to be integrated. The needed chip area is large and the cost is quite high.

On the other hand, system-on-package (SoP) is a good alternative. Instead of building everything in a single chip, modules of RF transceivers and bulky passive components can be designed and fabricated in different dies, and then fully integrated onto a single carrier as a multi-chip module. The technology of each module can be chosen appropriately to meet system requirements. To enable the success of SoP integration, an interconnect with good return loss and low insertion loss shall be provided. It behaves transparently to a signal and no additional matching networks are required. Broadband operation is also critical for high data-rate communications and the robustness to process variation. Flip-chip technology and wire bonding are widely employed for the interconnection [8]–[12]. The former has wider bandwidth because of its smaller parasitics. The latter is a popular choice since it is simple, low-cost, and well-established in consumer electronics. Yet its high-impedance property limits its operation bandwidth.

Some techniques were reported to improve the bandwidth of a bondwire interconnect. A bondwire with a shorter length exhibits wider bandwidth, but the minimum length is limited by the chip thickness. A cavity can be etched on the carrier to put a chip inside so that the top of the chip and the carrier can be near at the same horizontal level [13]. The bondwire length is shortened and the bandwidth is improved. Yet this inevitably needs an additional process and the cost is increased. Multiple bondwires can be shunt in parallel to reduce the bondwire inductance. However, the mutual inductance between bondwires sets a lower bound for the minimum achievable inductance. The operation bandwidth is still limited. A wideband bondwire interconnect is proposed by forming a five-stage low-pass filter [14]. It requires five elements for single interconnect realization. The occupied area is large and the cost is too high. The ground connection between the chip and the carrier is also unclear. Similar concepts are applied to narrowband applications by forming an L–C–L matching network [15]–[17]. Nevertheless, narrowband operation is sensitive to process and bonding variation. In addition, the network must be redesigned once the

Manuscript received July 05, 2013; revised August 29, 2013; accepted September 04, 2013. Date of publication September 19, 2013; date of current version December 02, 2013. This work was supported by the National Science Council, Taiwan, under Grant NSC 101-2220-E-009-013 and Grant 101-2220-E-009-053, by the Ministry of Education, Taiwan under the Aiming for the Top University (ATU) Program, and by MediaTek Inc. under a fellowship. This paper is an expanded paper from the IEEE MTT-S International Microwave Symposium, Seattle, WA, USA, June 2–7, 2013.

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Digital Object Identifier 10.1109/TMTT.2013.2281966

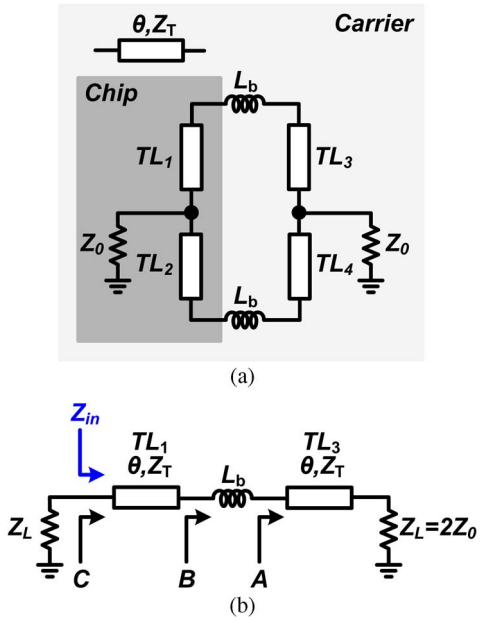


Fig. 1. (a) Proposed two-path broadband bondwire interconnect. (b) Equivalent circuit of (a) for the analysis.

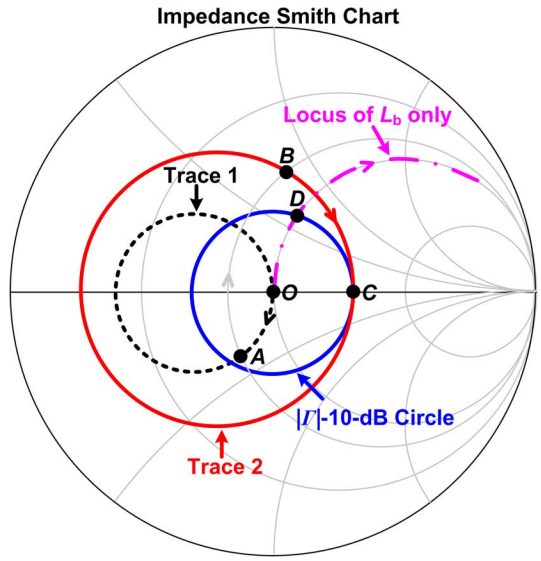


Fig. 2. Locus of optimal solution varied with the frequency on the Smith chart.

frequency of interest is changed. This increases the time spent on an interconnect design and delays products to markets.

In this paper, a low-cost bondwire interconnect is proposed to achieve broadband operation without any additional process. Transmission lines are incorporated with bondwires to form a multi-path structure. With properly designing the characteristic impedance and the length of transmission lines, the bondwire effect can be reduced. The technique can be applied to SoP for chip-to-carrier and chip-to-chip heterogeneous communications. Two- and three-path interconnects from a 90-nm CMOS chip to a glass-integrated-passive-device (GIPD) carrier have been demonstrated by the authors [18]. The measured return loss and insertion loss are better than 10.0 and 1.1 dB, respectively, from dc to 45.2 GHz. This paper focuses on the two-path design for chip-to-carrier communications, as shown in Fig. 1(a). The theory of the two-path interconnect is presented in this paper. Optimal solutions for the widest operation bandwidth are also provided with physical insights. A new interconnect from a 0.18-μm CMOS chip to a GIPD carrier is designed using the type of coplanar waveguides (CPWs) for the transmission line realization, instead of microstrip lines utilized in [18]. By doing this, parasitic effects caused by bonding pads can be minimized, and hence, the realized bandwidth is two times as wide as that reported in [18]. Moreover, the proposed interconnect has around 3.2 times bandwidth of a single bondwire alone. This paper is organized as follows. Section II explains the theory of the two-path broadband bondwire interconnect and design considerations. Section III illustrates the interconnect design using the proposed technique for heterogeneous communications between a CMOS chip and a GIPD carrier. Experimental results will be shown in Section IV. Finally, Section V concludes this work.

II. Analysis of Broadband Bondwire Interconnect

The proposed broadband bondwire interconnect is illustrated in Fig. 1(a). Signals are fed in from the center of the interconnect with source and load impedances Z_0, which is 50 Ω in this work. Transmission lines, $\mathrm{TL}_{1\text{-}2}$ and $\mathrm{TL}_{3\text{-}4}$, which have the same electrical length θ and characteristic impedance Z_T, are deployed on a chip and a carrier, respectively. Bondwires are assumed lossless and modeled by L_b. They are bonded from the chip to the carrier at the end of the transmission lines. It can be easily proven that the interconnect can be analyzed by its equivalent circuit, as depicted in Fig. 1(b), where the source and load impedances, Z_L, become $2Z_0$. By properly designing θ and Z_T, the proposed interconnect can work up to W-band with good return loss and low insertion loss.

A. Optimal Solution for Widest Bandwidth

The operation principle of the proposed interconnect can be understood graphically, as shown in Fig. 2, by observing the locus of its equivalent circuit on the Smith chart as a characteristic impedance of the transmission lines is given. Location of each node is designated as point A, B, C, D, and O on the Smith chart where the impedance is normalized to Z_L. By using this method, optimal solutions, which mean the widest operation bandwidth in this paper, can also be found easily. In the first place, the case of a single bondwire alone is considered. The locus goes directly out of a circle corresponding to the return loss of 10 dB, designated as a $|\Gamma|$–10-dB circle, along a constant-r circle. This explains why the bandwidth is quite limited. In contrast, for the proposed interconnect, the impedance becomes capacitive as it moves along Trace 1 to point A at a frequency f_0 after adding a transmission line $T_{\mathrm{L}3}$. Subsequently, the bondwire turns the impedance inductive by going along a constant-r circle to point B. Finally, $T_{\mathrm{L}1}$ brings the impedance back to inside, on, or outside the $|\Gamma|$–10-dB circle, along Trace 2. Note that Trace 1 and Trace 2 can be approximated as a circle. The widest bandwidth from dc to a maximum operation frequency, denoted as $f_{\max}$, occurs as Trace 2 and the $|\Gamma|$–10-dB circle intersect at only one point, i.e., point C. Other cases of either no intersection or two-point intersection are not the optimal solutions. The former gives the return loss worse than 10 dB at the present f_0, while the later implies that there must exist

a frequency higher than f_0, which can still provide the return loss better than 10 dB. Notice that the impedance at frequencies lower than $f_{\max}$ is within the $|\Gamma|$–10-dB circle. Thus, the distance along a constant-r circle on the Smith chart, which allows bondwire impedance to vary while keeping the return loss higher than 10 dB, is extended from point O to point D of a single bondwire alone to point A to point B of the proposed bondwire interconnect. Obviously, the proposed interconnect can reduce the bondwire effect and works at a much higher frequency. It is worth mentioning that $Z_{\rm T}$, which is smaller than $Z_{\rm L}$, is a better solution. If $Z_{\rm T}$ is larger than $Z_{\rm L}$, the impedance appears inductive as $T_{\rm L3}$ is added. Quite long transmission lines are then required to stay the locus within the $|\Gamma|$–10-dB circle. The occupied area will be large.

With the above observation, the optimal solutions can be obtained accordingly. To ease the analysis, the transmission lines are assumed lossless. Denote the normalized impedance with respect to $Z_{\rm L}$ at point B as $r + jx$. The impedance at point C, represented by normalized $r_{\max}$, can be found to be 1.92 by perceiving that it is real and on the $|\Gamma|$–10-dB circle. If other levels of the return loss are required, $r_{\max}$ can be found correspondingly. The first governing equation can be acquired by noting that the input impedance of $T_{\rm L1}$ loaded by the impedance at point B is equal to the one at point C, i.e.,

$$\widetilde{Z_{\rm T}}\frac{r+jx+j\widetilde{Z_{\rm T}}\tan\theta}{\widetilde{Z_{\rm T}}+j(r+jx)\tan\theta}=r_{\max} \tag{1}$$

where $\widetilde{Z_{\rm T}}$ is equal to $Z_{\rm T}/Z_{\rm L}$. The same reasoning can be applied to point A and another governing equation can then be acquired as

$$\widetilde{Z_{\rm T}}\frac{1+j\widetilde{Z_{\rm T}}\tan\theta}{\widetilde{Z_{\rm T}}+j\tan\theta}=r+jx-\frac{j2\pi f_{\max}L_{\rm b}}{Z_{\rm L}}=r+jx-jx_{\rm ind,max} \tag{2}$$

where $x_{\rm ind,max}$ is defined as the bondwire reactance at $f_{\max}$ normalized to $Z_{\rm L}$. By equating the real and the imaginary parts of the left- and right-hand sides of (1) and (2), simultaneous equations with a set of four can be found,

$$\frac{r\widetilde{Z_{\rm T}^2}\sec^2\theta}{(\widetilde{Z_{\rm T}}-x\tan\theta)^2+r^2\tan^2\theta}=r_{\max} \tag{3}$$

$$\frac{x\widetilde{Z_{\rm T}}-x^2\tan\theta+\widetilde{Z_{\rm T}^2}\tan\theta-r^2tan\theta-x\widetilde{Z_{\rm T}}\tan^2\theta}{(\widetilde{Z_{\rm T}}-x\tan\theta)^2+r^2\tan^2\theta}=0 \tag{4}$$

$$\frac{\widetilde{Z_{\rm T}^2}\sec^2\theta}{\widetilde{Z_{\rm T}^2}+\tan^2\theta}=r \tag{5}$$

$$\frac{\widetilde{Z_{\rm T}}\left(\widetilde{Z_{\rm T}^2}-1\right)\tan\theta}{\widetilde{Z_{\rm T}^2}+\tan^2\theta}=x-x_{\rm ind,max}. \tag{6}$$

There are four equations for four unknowns. The optimal solutions can be derived as

$$r=\frac{\widetilde{Z_{\rm T}^2}+r_{\max}}{r_{\max}+1} \tag{7}$$

$$x=\frac{\left(r_{\max}^2-\widetilde{Z_{\rm T}^2}\right)}{(r_{\max}+1)\sqrt{r_{\max}}} \tag{8}$$

$$f_{\max}=\frac{\left(r_{\max}-\widetilde{Z_{\rm T}^2}\right)}{2\pi L_{\rm b}\sqrt{r_{\max}}}Z_{\rm L} \tag{9}$$

$$\theta_{\max}=\sec^{-1}\sqrt{1+\frac{\widetilde{Z_{\rm T}^2}}{r_{\max}}} \tag{10}$$

where $\theta_{\max}$ represents the optimal electrical length of $T_{\rm L1}$ and $T_{\rm L3}$ for achieving $f_{\max}$. Once $\theta_{\max}$ is acquired, the physical length of the transmission lines can be obtained as

$$l_{\rm opt}=\frac{\theta_{\max}}{\beta_{\max}}=\frac{c}{2\pi\sqrt{\varepsilon_{\rm eff}}}\frac{\theta_{\max}}{f_{\max}} \tag{11}$$

where $\beta_{\max}$, c, and $\varepsilon_{\rm eff}$ are the propagation constant at $f_{\max}$, the speed of light in air, and the effective dielectric constant of dielectric materials in the transmission lines, respectively.

Equations (7)–(10) show that the optimal solutions only depend on $\widetilde{Z_{\rm T}}$, as a bondwire inductance and the required return loss level are given. In contrast, $\theta_{\max}$ is only determined by $\widetilde{Z_{\rm T}}$, no matter what the value of $L_{\rm b}$ is. It is also interesting to see that the magnitude of the bondwire impedance at $f_{\max}$, i.e., $2\pi f_{\max}L_{\rm b}$, is constant as $\widetilde{Z_{\rm T}}$ is given. This implies that as $L_{\rm b}$ is double, $f_{\max}$ will be half. In other words, the value of the bondwire inductance sets an upper bound of $f_{\max}$ for the proposed interconnect. Smaller bondwire inductance is still preferred to wider operation bandwidth.

The maximum operation frequency and the optimal electrical and physical length of the transmission lines can be acquired using (9)–(11), as illustrated in Fig. 3, where the bondwire inductance is varied. $\varepsilon_{\rm eff}$ is assumed as 3.5, an average value of effective dielectric constant of materials used in later realization. The maximum operation frequency that a single bondwire can achieve is also shown. Obviously, the proposed interconnect has great improvement on the bandwidth as compared with a single bondwire alone. The optimal solutions are more sensitive to $Z_{\rm T}$ variation as $Z_{\rm T}$ is larger. $f_{\max}$ also gets higher with a smaller $Z_{\rm T}$. This corresponds to a smaller required $\theta_{\max}$, i.e., shorter transmission lines. However, transmission lines with a small characteristic impedance have a large area. In addition, as indicated in Fig. 2, smaller $Z_{\rm T}$ represents that Trace 1 has a bigger radius on the Smith chart. This implies that the location of point A is sensitive to the electrical length of the transmission lines, resulting in that the interconnect performance becomes sensitive to θ. Besides, in practice, pads are required for the bonding of the bondwires, which inevitably contributes undesired parasitic capacitances, modeled as $C_{\rm p}$ in Fig. 4. It can be perceived that $C_{\rm p}$ reduces the realizable bandwidth since it will move point A out of the $|\Gamma|$–10-dB circle, as observed in Fig. 2. The interconnect with a smaller $Z_{\rm T}$ will not be immune to these parasitics because of its high sensitivity on θ. Hence,

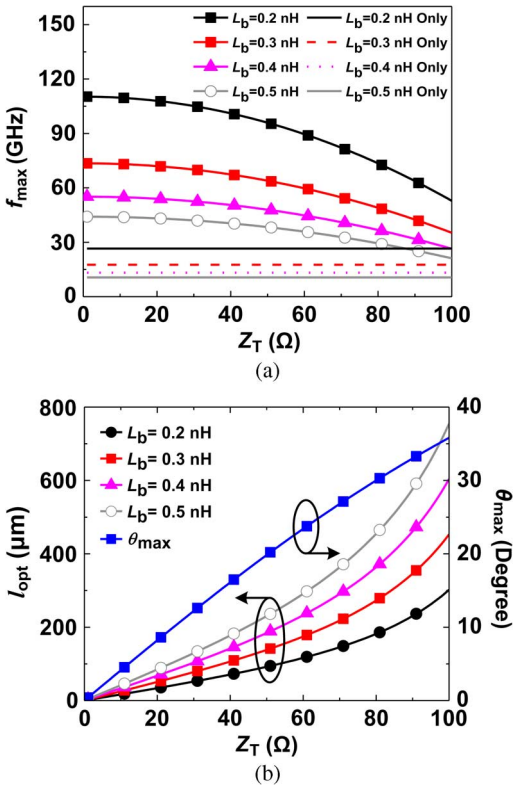


Fig. 3. Optimal solutions versus Z_T as the bondwire inductance is varied. (a) f_{max}. (b) l_{opt} and θ_{max}.

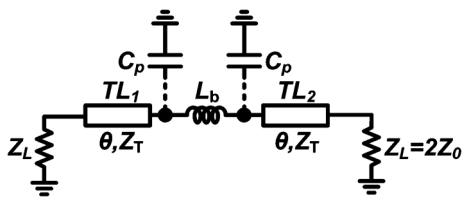


Fig. 4. Equivalent circuit of the proposed interconnect with parasitic capacitances of the bonding pads.

choosing a higher Z_T is a better choice, considering the practical realization.

Another advantage of choosing transmission lines with a higher Z_T is that the interconnect for heterogeneous system integration can be designed easily. In general, the effective dielectric constant of dielectrics in the chip and the carrier is not the same. The interconnect performance is not sensitive to the electrical length if the transmission lines have a higher characteristic impedance. Thus, the physical length of the transmission lines on the chip and the carrier can be selected the same without affecting the performance much. In the later

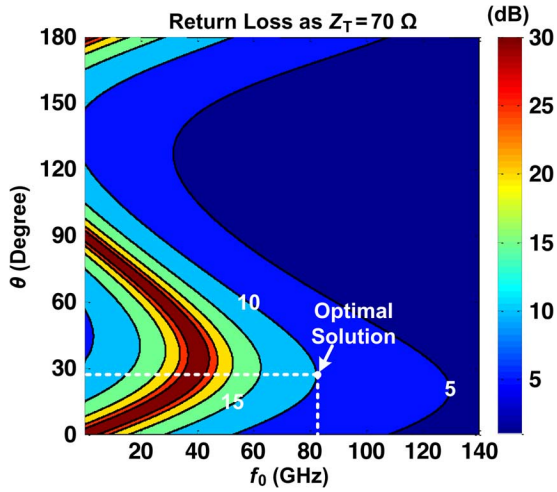


Fig. 5. Return loss of the proposed bondwire interconnect using (14).

realization of the interconnect, the difference of the electrical length of on-chip and on-carrier transmission lines is around 3.1°. In this work, Z_T of around 70 Ω is chosen to tolerate this difference and parasitics induced by bonding pads, which still provides 3.1 times bandwidth of a single bondwire alone.

B. Closed Form for the Return Loss

To verify the above graphical method for finding the optimal solutions, the closed form of the reflection coefficient is derived. The impedance at point B can be obtained as

$$\widetilde{Z_B} = \widetilde{Z_T}\frac{1 + j\widetilde{Z_T}\tan\theta}{\widetilde{Z_T} + j\tan\theta} + jx_{ind} \tag{12}$$

where $x_{ind} = 2\pi f L_b/Z_L$. Using (12), the input impedance $\widetilde{Z_{in}}$ and the reflection coefficient Γ of the interconnect can be acquired as (13) and (14), respectively, shown at the bottom of this page. Note that once the return loss is found, the insertion loss can be acquired easily by $(1-|\Gamma|^2)$, assuming the interconnect is lossless. As illustrated in Fig. 5, a contour plot is used to help understand the variation of the return loss versus θ and operation frequency as Z_T of 70 Ω and L_b of 0.2 nH are given. The optimal solutions for providing the widest bandwidth are found to be f_{max} of 82.1 GHz and θ_{max} of 26.8°, exactly the same as that obtained by (9) and (10). This verifies the graphical method for finding the optimal solutions discussed in Section II-A. Furthermore, the plot shows that the interconnect performance is not sensitive to the electrical length of the transmission lines. This explains why Z_T of 70 Ω is chosen in this work. The return loss and insertion loss of the interconnect at this optimal solution is

$$\widetilde{Z_{in}} = \frac{Z_{in}}{Z_L} = \frac{1 - \tan^2\theta - x_{ind}\tan\theta/\widetilde{Z_T} + j(x_{ind} + 2\widetilde{Z_T}\tan\theta)}{1 - \tan^2\theta - x_{ind}\tan\theta/\widetilde{Z_T} + j\left(2\tan\theta/\widetilde{Z_T} - x_{ind}\tan^2\theta/\widetilde{Z_T^2}\right)} \tag{13}$$

$$\frac{1}{\Gamma} = \frac{\widetilde{Z_{in}}+1}{\widetilde{Z_{in}}-1} = \frac{\left(x_{ind} + 2\widetilde{Z_T}\tan\theta + 2\tan\theta/\widetilde{Z_T} - x_{ind}\tan^2\theta/\widetilde{Z_T^2}\right) - j2\left(1 - \tan^2\theta - x_{ind}\tan\theta/\widetilde{Z_T}\right)}{x_{ind} + 2\widetilde{Z_T}\tan\theta - 2\tan\theta/\widetilde{Z_T} + x_{ind}\tan^2\theta/\widetilde{Z_T^2}} \tag{14}$$

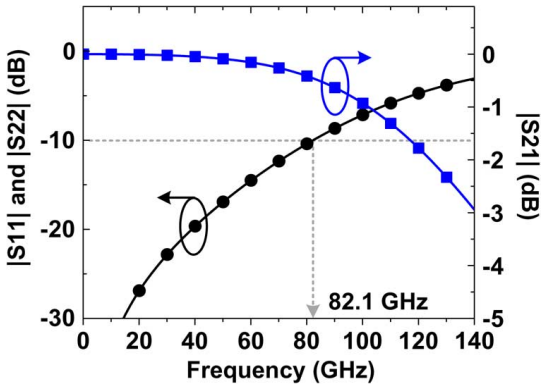


Fig. 6. Return loss and insertion loss of the proposed interconnect at the optimal solution of Fig. 5.

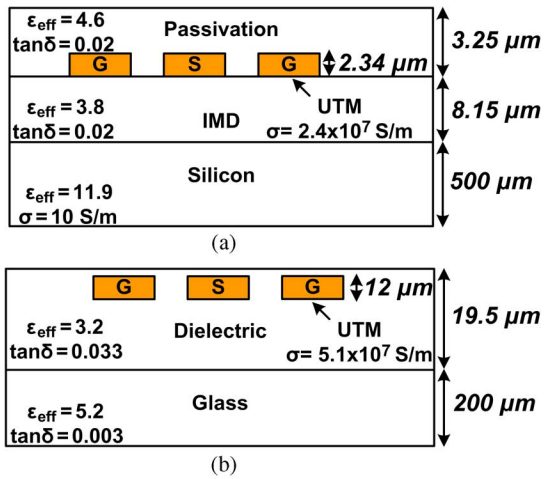


Fig. 7. Cross-section view of layers and material properties of: (a) 0.18-μm CMOS and (b) GIPD process.

also simulated using Agilent Advanced Design System (ADS), as depicted in Fig. 6. The operation bandwidth can be span from dc to 82.1 GHz, around 3.1 times bandwidth of 26.5 GHz obtained by a single bondwire alone.

III. Broadband Bondwire Interconnect Design

A transition from a 0.18-μm CMOS chip to a GIPD carrier for chip-to-carrier communications is designed to verify the proposed broadband interconnect. Material properties of the two technologies are shown in Fig. 7. Ultra-thick metal layers with a thickness of 2.4 and 12 μm are chosen to realize on-chip and on-carrier transmission lines, respectively. The chip has a substrate thickness of 500 μm while the carrier has that of 200 μm. The physical structure of the designed interconnect using the proposed technique is illustrated in Fig. 8 while detailed dimensions are summarized in Table I. The type of CPWs is chosen for the transmission line realization since the gap between the signal and the ground can be properly adjusted to mitigate parasitic effects induced by bonding pads. Another important consideration is the ground interconnection. Note that not only the signal needs to be transferred from the chip to the carrier smoothly, but the ground connection is also critical to ensure the same ground potential between the chip and the carrier. Hence, multiple bondwires are bonded between the chip ground and the carrier ground to minimize ground parasitics. If using a single bondwire

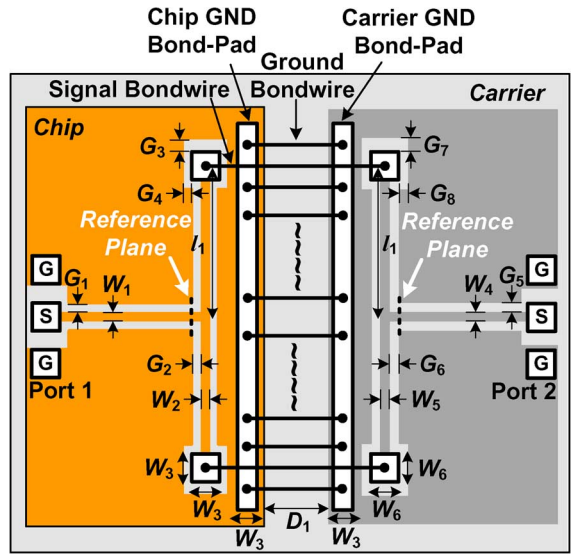


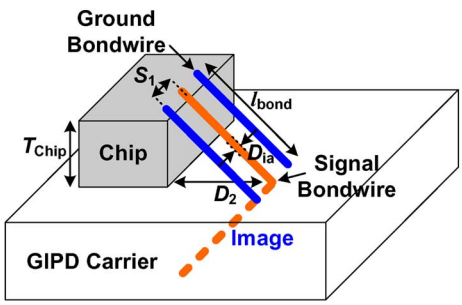
Fig. 8. Realized broadband interconnect for chip-to-carrier communications.

TABLE I
Physical Dimensions of the Proposed Interconnect

Parameter (μm)	Value (μm)
Bondwire Diameter	20 (0.8 mil)
G_1	5.5
G_2	35
G_3	50
G_4	25
G_5	13
G_6	25
G_7	50
G_8	25
W_1	10
W_2	10
W_3	50
W_4	10
W_5	10
W_6	70
l_1	150
D_1	310

for the ground connection, this bondwire will cause a peaking at the return loss and limit the achievable bandwidth. Moreover, as mentioned before, the bondwire inductance sets an upper bound of the maximum operation bandwidth. It is interesting to see that ground bondwires adjacent to signal bondwires can also be used to reduce the bondwire inductance by inducing negative mutual coupling to the signal bondwires. Hence, the operation bandwidth can be greatly improved. Indeed, the quality factor (Q) of signal bondwires is degraded. Fortunately, Q is still high since bondwires are very low loss intrinsically.

The analysis given in Section II can be used to find an initial design for the proposed interconnect. As mentioned before, $Z_{\rm T}$ of 70 Ω is chosen in this work to reduce the parasitic effect caused by bonding pads and to make the interconnect performance insensitive to the electrical length of transmission lines. The gaps between the signal and the ground, i.e., G_2 and G_6, and the line widths, i.e., W_2 and W_5, for the on-chip and on-carrier transmission lines are designed as 15 and 25 μm, and 10 and 10 μm, respectively, to have a characteristic impedance of 70 Ω.



	Value (μm)
D_{ia}	20
l_{bond}	707
D_2	500
T_{Chip}	500
S_1	100

	Value (nH)
L_{self}	0.57
$L_{m,image}$	0.09
$L_{m,GND}$	0.25
L_b	0.23

Fig. 9. Lateral view of wire bonding for bondwire inductance estimation.

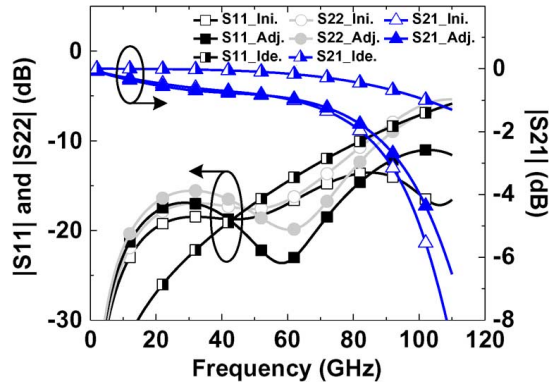


Fig. 10. Simulation results of the proposed broadband bondwire interconnect.

The optimal electrical length of transmission lines is determined as 26.8° using (10). To find $f_{\max}$ and the optimal physical length of the transmission lines, bondwire inductance needs to be acquired first. For two wires in parallel carrying the same current with center distance of S, the mutual inductance can be calculated as [19]

$$L_m = \frac{\mu_0}{2\pi} l \left\{ \ln \left[\frac{l}{S} + \sqrt{1+\left(\frac{l}{S}\right)^2} \right] - \sqrt{1+\left(\frac{S}{l}\right)^2} + \frac{S}{l} \right\} \tag{15}$$

where μ_0 is the permeability of air and l is the wire length. The effective bondwire inductance can be found as

$$L_b = L_{\text{self}} - L_{\text{m,GND}} - L_{\text{m,image}} \tag{16}$$

where $L_{\text{m,GND}}$ and $L_{\text{m,image}}$ are mutual inductance between a signal bondwire to adjacent ground bondwires and between a signal bondwire and its image, respectively. L_{self} is inductance of a wire of diameter d, which can be given as [20]

$$L_{\text{self}} = \frac{\mu_0}{2\pi} l \left\{ \ln \left[\frac{2l}{d} + \sqrt{1+\left(\frac{2l}{d}\right)^2} \right] + \frac{d}{2l} - \sqrt{1+\left(\frac{d}{2l}\right)^2} \right\}. \tag{17}$$

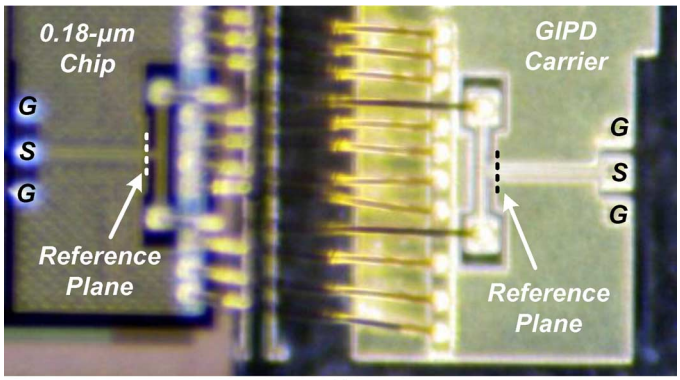
Assume that bondwires are bonded from the chip to the carrier with an angle of 45°. Since bondwires, in practice, are curved and nonhorizontal, a half value of the thickness of the chip substrate is used as the distance between the wire and the ground plane, i.e., 500 μm between the wire and its image. Given the dimension of the bondwires, as shown in Fig. 9, L_{self}, $L_{\text{m,image}}$, $L_{\text{m,GND}}$, and $L_{\text{m,image}}$ can be calculated as 0.57, 0.09, 0.25, and 0.23 nH, respectively, by (15)–(17). A round number of 0.2 nH is used for L_{b} in the following design. $f_{\max}$ and the optimal physical length are then calculated to be around 82.1 GHz and 145 μm, respectively, using (9) and (11). The difference of the electrical length of on-chip and on-carrier transmission lines is around 3.1°. As mentioned before, multi-bondwires in parallel can be used to reduce bondwire inductance. Assume two bondwires in parallel with length of 707 μm and spacing of 20 μm. The effective bondwire inductance can be calculated as $(L_{\text{self}} + L_{\text{m}})/2$, i.e., 0.52 nH. It is interesting to see that two bondwires in parallel only reduce bondwire inductance from 0.57 to 0.52 nH. The operation bandwidth is still quite limited.

3-D electromagnetic (EM) simulation using ANSYS HFSS is conducted for the interconnect characterization. Gold bondwires with a diameter of 0.8 mil, i.e., 20 μm, are used. As illustrated in Fig. 10, the simulation results of the initial design, denoted as $S11_{\text{Ini.}}$, $S22_{\text{Ini.}}$, and $S21_{\text{Ini.}}$, can be smaller than -13.6 and -10 dB, and greater than -3 dB, respectively, up to 84.5 GHz. The simulation results of the lossless interconnect shown in Fig. 1(a) using ADS, i.e., $S11_{\text{Ide.}}$ and $S21_{\text{Ide.}}$, are also shown. They have a similar response with each other. The difference is contributed by parasitics that are not considered in the simple model shown in Fig. 1(a). Input T-junctions, parasitic effects induced by the bonding pads, and the ground connection might cause the discrepancy. Yet the analysis given before indeed provides good initial design for the proposed interconnect. Finally, fine tuning is conducted and it is found that as G_2 is adjusted from 15 to 35 μm, the bandwidth can be improved. The characteristic impedance of on-chip transmission lines is changed from 70 to 90 Ω. The simulation results of the adjusted interconnect, denoted as $S11_{\text{Adj.}}$, $S22_{\text{Adj.}}$, and $S21_{\text{Adj.}}$, can be smaller than -12.8 and -10 dB, and greater than -2.3 dB, respectively, from dc to 88.5 GHz, around 4-GHz improvement to that of the initial design. Detailed dimensions of the final interconnect are summarized in Table I.

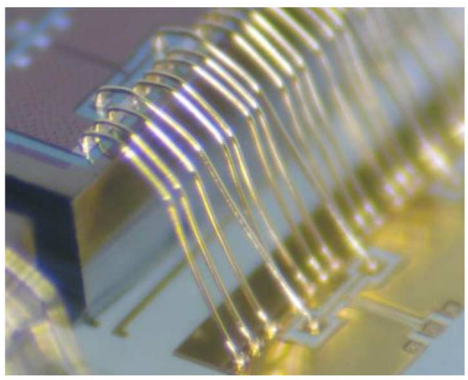
IV. Experimental Results

The micrograph of the proposed broadband interconnect is shown in Fig. 11. The chip and carrier are realized in 0.18-μm CMOS technology and GIPD process, respectively. Gold bondwires with a diameter of 20 μm are used for the proposed interconnect. The measurement is conducted by an on-wafer setup where the input and the output signals are applied through high-frequency ground–signal–ground (GSG) probes. Scattering parameters are measured from 2 to 110 GHz by a 110-GHz network analyzer. An L-2L multi-line de-embedding method using two transmission lines with a length of 250 and 500 μm is used to remove the influence of probing pads and move the reference plane of scattering parameters to the desired position [21]. Four proposed interconnects are measured to investigate the performance variation between samples.

The measured return loss and the insertion loss are illustrated in Fig. 12. $S11$ and $S22$ have similar trends, but exactly not the same because bondwires are not symmetric in practice. The measured insertion loss can be better than 3.0 dB from dc to 84 GHz while providing $S11$ and $S22$ smaller than -16.6 and -13.4 dB, respectively. The measured results show a similar trend with the simulated ones. Moreover, four samples show similar performance, which guarantees the robustness of the



(a)



(b)

Fig. 11. Micrograph of the proposed interconnect. (a) Top view. (b) Side view.

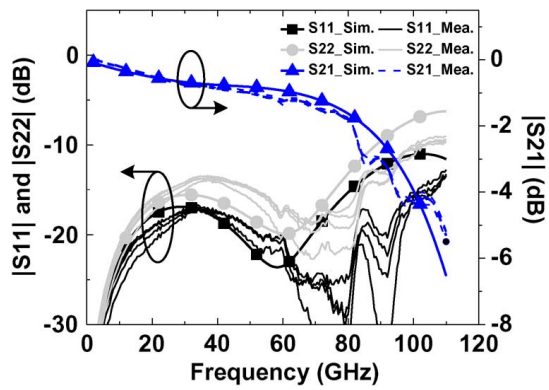


Fig. 12. Measured return loss and insertion loss of the proposed broadband bondwire interconnect.

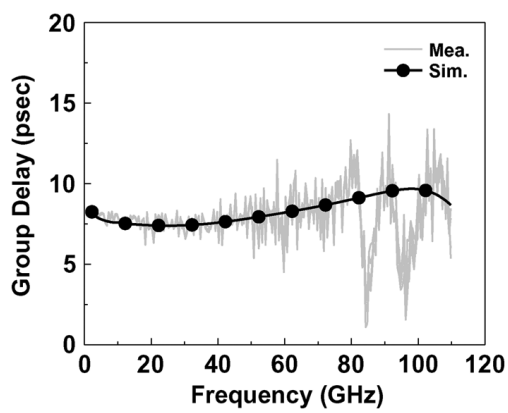


Fig. 13. Measured group delay of the proposed broadband bondwire interconnect.

proposed broadband interconnect against the bonding variation. The measured group delay is shown in Fig. 13. To the best of the authors' knowledge, this work demonstrates the bondwire interconnect with the widest operation bandwidth reported thus far. Hence, a low-cost and high-performance heterogeneous system can be realized using the proposed technique for the integration.

V. Conclusion

A broadband bondwire interconnect suitable for low-cost heterogeneous integration by using SoP is proposed and verified by experimental results. Transmission lines are co-designed with bondwires to reduce the bondwire effect. The interconnect has a 3.2× bandwidth of a single bondwire alone. Theoretical analysis is given to find an optimal electrical length of the transmission lines for providing the maximum operation bandwidth. An interconnect from a 0.18-μm CMOS chip to a GIPD carrier is designed to verify the technique. Measured results show that the insertion loss can be better than 3.0 dB from dc to 84 GHz while providing $S11$ and $S22$ smaller than -16.6 and -13.4 dB, respectively. The interconnect can be used to realize a low-cost and high-performance millimeter-wave heterogeneous system by using SoP.

Acknowledgment

The authors would like to acknowledge the National Device Laboratories (NDL), Hsinchu, Taiwan, for measurement support, and ANSYS, Taipei, Taiwan, for design support.

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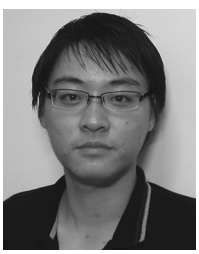

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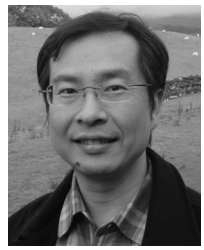

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