Si_xGe_{1-x} Epitaxial Tunnel Layer Structure for P-Channel Tunnel FET Improvement

Pei-Yu Wang, *Student Member, IEEE*, and Bing-Yue Tsui, *Senior Member, IEEE*

***Abstract*— The tunnel field-effect transistor (FET) is a promising candidate for use in ultralow-power applications because of its distinct operation principle, namely, band to band tunneling (BTBT). However, the ON-state current of the tunnel device is extremely low because of the poor tunneling efficiency of the BTBT. In this paper, a novel epitaxial tunnel layer (ETL) structure combining vertical tunneling orientation was proposed. The ETL structure performs more favorably than does the traditional lateral tunnel FET structure in an all-silicon device. By using low bandgap materials in the ETL, the ON-state BTBT current increases and an extremely low intrinsic OFF-state current is maintained because of the small low bandgap junction area. The onset voltage of the bipolar BTBT can also be postponed using ETL band engineering. The optimized parameters of the Si_xGe_{1-x} ETL tunnel FET structure increase the ON-state current 10^7–10^8 times compared with that of the traditional lateral silicon tunnel FET. The minimal subthreshold swing (SS) and ON/OFF current ratio also improve, the SS decreases from 47 mV/decade to 29 mV/decade, and the ON/OFF current ratio increase from 10^5 to 10^{10}. In this paper, the effects of the ETL parameters on device performance are discussed in detail.**

***Index Terms*— Band to band tunneling, epitaxial tunnel layer (ETL), silicon-germanium (Si_x Ge_{1-x}), subthreshold swing (SS), tunnel field-effect transistor, vertical tunneling.**

I. Introduction

In RECENT years, green energy has attracted substantial attention; however, as the metal-oxide-semiconductor field-effect transistor (MOSFET) rapidly scales down, numerous devices consequently demonstrate high standby and dynamic power consumption [1]. To eliminate this undesirable phenomenon, lowering the OFF-state leakage current or lowering the operating voltage are two intuitive methods that can be used. When the leakage current and operating voltage decrease, a steep subthreshold swing (SS) characteristic is required to achieve sufficient ON-state current to power the circuits. In conventional MOSFETs, the operation principle of thermionic carrier injection limits the SS to 60 mV/decade at room temperature. This physical constraint limits the scaling of the threshold and operating voltages.

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The authors are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: zomanto@gmail.com; bytsui@mail.nctu.edu.tw).

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Tunnel FET is an appropriate candidate for use in low-power applications because of the intrinsic operation characteristics of the tunnel FET. The distinct operation mechanism, band-to-band tunneling (BTBT), can be applied to a tunnel FET device, breaking the 60 mV/decade limit and facilitating the development of a new generation of low-power applications [2]–[6]. However, the steep SS in tunnel FETs occurs only at extremely low current levels and rapidly degrades because of inefficient BTBT [7]–[10]. To improve tunneling efficiency, various studies have proposed using low bandgap material to lower the tunnel barrier. Several researches have applied low bandgap material only on the source side to increase the tunneling current [11]–[14]. Although increasing the ON-state current and maintaining a low OFF-state current is a favorable goal, the device is extremely difficult to implement and the defects that occur at the hetero-junction interface is a serious problem. In addition, replacing the intrinsic region material instead of the source material is intuitive because the tunnel barrier is usually located in the intrinsic region. Therefore, other researches have used low bandgap material to replace the entire channel region [15]–[18]. However, those who apply this methodology must consider the bipolar BTBT effect, which can cause a high OFF-state current. Novel device structures have also been continually proposed to improve device performance [19]–[22]. All of them must control a special doping profile such as the ultrathin doping region and ultrahigh doping concentration levels. This is difficult to attain and may cause substantial fabrication variations.

To improve tunnel FET performance while considering fabrication feasibility, a novel epitaxial tunnel layer (ETL) tunnel FET was proposed, combining vertical tunneling and the band engineering of the ETL hetero-junction to enhance the ON-state current and maintain low OFF-state current [23]. The critical parameter in the ETL structure is the Si_xGe_{1-x} ETL film thickness, which is more controllable compared with the ultraabrupt doping profile of the other tunnel devices. In this paper, the ETL tunnel FET concepts, structural parameters, and effects thereof were evaluated in detail. The material chosen for complementary tunnel FET, ETL thickness, doping effect, and gate-to-source and drain overlap length were also included in the analysis. A qualitative analysis of the quantum confinement effect was also discussed.

II. Device Structure and Simulation Description

Fig. 1(a) illustrates the schematic structure of the ETL tunnel FET. A low bandgap material was capped on the channel surface to form the ETL structure, which consequently

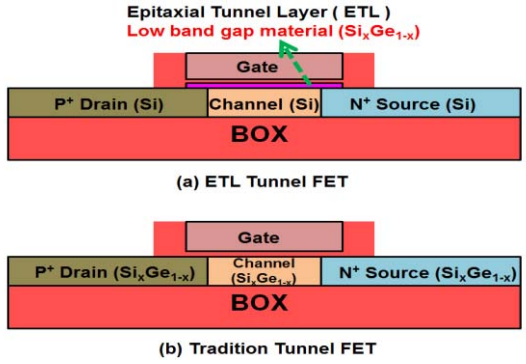

Fig. 1. Schematic cross-sectional structure. (a) ETL tunnel FET with vertical tunneling orientation design. (b) Traditional lateral tunnel FET. P-channel tunnel FET using low bandgap material of Si_xGe1-x is investigated in this paper.

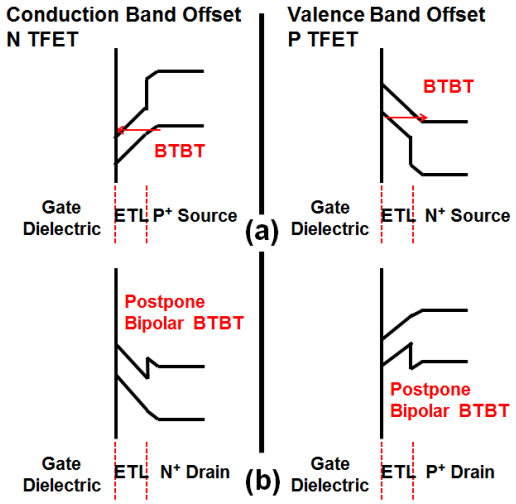

Fig. 2. Band diagrams of the ETL tunnel FET at the gate-to-source and drain overlap region along the vertical direction. The general concepts to improve the performance of the complementary tunnel FETs are demonstrated. (a) Operation-state ($V_G > 0$ for NFET, $V_G < 0$ for PFET). (b) Bipolar-state ($V_G < 0$ for NFET, and $V_G > 0$ for PFET).

reduced the tunneling barrier for BTBT. In this paper, process integration compatibility was considered. Silicon was subsequently chosen as the channel material and Si_xGe_{1-x} was chosen as the ETL material. The maximal level Ge content was set at 50% to maintain the defect-free fully strained Si_xGe_{1-x} layer because the ETL thickness ranged from 2 to 10 nm [24]. The channel thickness and length were 20 and 100 nm, respectively, with a boron doping concentration of 1×10^{15} cm^{-3}. The SiO_2 gate dielectric was 2-nm thick. The doping concentration of the P^+ drain and N^+ source regions were both 1×10^{20} cm^{-3}. The work function of the gate electrode was 5.0 eV. The gate-to-source and drain overlap ranged from 5 nm to 30 nm. The *n*-type ETL was aligned with the gate electrode and had a doping concentration of 1×10^{15} cm^{-3}, if no value was specified. The ON-state current and OFF-state current were extracted at $V_G = -1$ V, $V_D = -0.5$ V, and $V_G = 0$V, $V_D = -0.5$ V, respectively.

Sentaurus-TCAD tool was used [25]. The dynamic nonlocal BTBT model that comprised default indirect BTBT parameters was activated throughout the semiconductor region, including the source and drain channel and ETL regions, to emulate BTBT behavior. The recombination SRH model that comprised default parameters ($E_{trap} = 0$ eV), mobility model, and Fermi distribution were all considered to simulate the device characteristics. The nonideal effects such as defect-assisted tunneling and gate leakage current were ignored. Therefore, the leakage current was dominated by the ideal P^+-I-N^+ diode leakage current. In this paper, only the intrinsic device OFF-state characteristics of the ETL tunnel device in the ideal condition were investigated. With an extremely thin SOI channel, the OFF-state current was much lower than the actual current measurement limit. The quantization model was also ignored in this paper because using the TCAD model is insufficient for coupling the correlation between the BTBT model and the quantized level. In addition, a qualitative analysis of the ETL structure was used instead of a quantitative analysis. A traditional lateral tunnel FET, displayed in Fig. 1(b), was also simulated. This device possesses no ETL layer and the source and drain regions were constructed using low bandgap material.

III. ETL Tunnel FET Design Concept

A. Low Bandgap Material Choice

In the traditional tunnel FET structure, the tunneling barrier height of the ON-state BTBT is determined by the bandgap of the channel material. Applying low bandgap channel material is an effective method for enhancing tunneling efficiency. However, this increases the OFF-state current primarily because of the SRH generation current in the depletion region and the bipolar BTBT current if other nonideal effects are ignored. To maintain a low OFF-state current and increase the ON-state BTBT current, the ETL structure was proposed. BTBT occurs in the ETL region instead of the channel region. Therefore, the BTBT orientation is vertical and the tunneling region is ideally the gate-to-source and drain overlap region. The lateral BTBT was minimized by applying wide bandgap material to the channel region, including the source and drain regions. In the simulation results, lateral tunneling between the N^+ Si source region and the Si channel region did not occur because of the wide bandgap of the Si channel and the low electric field caused by the ETL.

Fig. 2 depicts the general concepts of low bandgap material selection for complementary tunnel FETs. It indicates that low bandgap material with conduction band offset is suitable for n-channel tunnel FET operation.The ON-state BTBT current may increase when the tunneling barrier height is lowered, and the onset voltage of the bipolar BTBT can be postponed by the conduction band offset. Conversely, the material with valence band offset is suitable for p-channel tunnel FET. One of the disadvantages of using low bandgap material is the high SRH generation current. However, the SRH generation current is suppressed in the ETL structure because of the extremely small low bandgap ETL region. Fig. 3 indicates that high SRH generation rate in the OFF-state occurs in the ETL region because of the low bandgap. Therefore, the

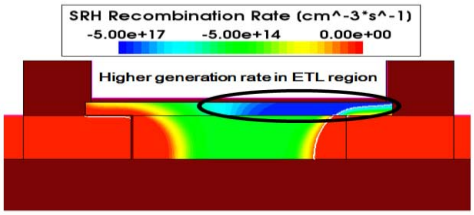

Fig. 3. SRH recombination profile in the ETL structure in the OFF-state ($V_D = -0.5$ V, $V_G = 0$ V). The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL thickness is 6 nm. Source and drain overlap length are 15 nm.

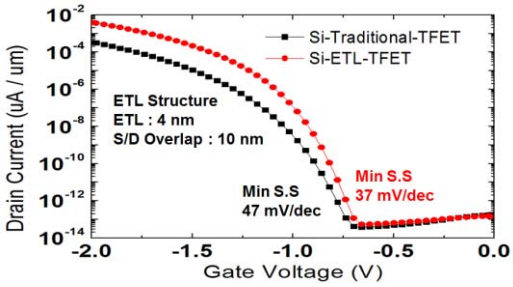

Fig. 4. Transfer characteristics of the ETL and traditional tunnel FET structure. In this simulation, the ETL is also Si in order to reveal the structural effect only.

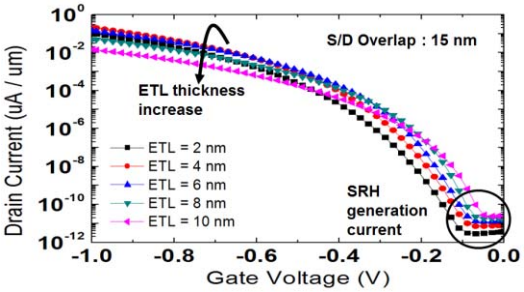

Fig. 5. Transfer characteristics of the ETL tunnel FET with different ETL thickness. The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL thickness ranges from 2 to 10 nm.

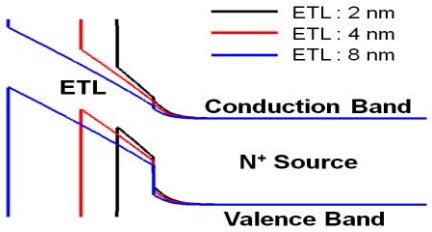

Fig. 6. ON-state band diagram along the vertical directionin the tunneling region. The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL thickness ranges from 2 to 8 nm.

two major components of the intrinsic OFF-state current were minimized by using the proposed ETL structure.

On the basis of this analysis, combining the Si_xGe_{1-x} ETL and Si channel was determined to be suitable for p-channel ETL tunnel FET operation. In addition, all the low bandgap materials that could grow on the channel surface without producing serious defects were suitable for the ETL structure. For example, InAs is suitable for n-channel ETL tunnel FET [11]. Numerous studies have developed the methods for growing InAs on a silicon surface [26]–[29].

B. Tunneling Area and Orientation

Regarding traditional tunnel FET, the lateral BTBT dominants the ON-state current regularly, and the tunneling area is located in only an extremely small local region. This decreases the tunneling efficiency and results in a low BTBT current in traditional lateral tunnel devices. Regarding ETL tunnel FET, vertical tunneling occurs in the ETL region, and the ideal tunneling area is approximately determined by the source and drain overlap length [30]. Therefore, the tunneling current can be improved by extending the gate-to-source and drain overlap length. In addition, the tunneling orientation is identical to the electric field direction modulated by the gate, indicating excellent gate coupling [31], [32].

The aforementioned information suggests that the ETL structure with a vertical tunneling orientation allows for improved tunneling efficiency compared with the traditional lateral BTBT structure. Fig. 4 shows the transfer characteristics of the all-silicon lateral tunnel FET and the all-silicon ETL tunnel FET, verifying the proposed concepts. The results indicate that the ETL structure produces a more favorable SS and a higher BTBT current than does the lateral structure.

IV. Effect of ETL Parameters

A. ETL Thickness Effect

Fig. 5 shows the transfer characteristics of the $Si_{0.5}Ge_{0.5}$ ETL tunnel FET based on the effect of ETL thickness. The results demonstrate that improper ETL thickness degrades the ON-state BTBT current. This is explained by the ON-state band diagram along the vertical orientation as shown in Fig. 6. A thin ETL would allow the vertical BTBT to be inhibited because the valence band would not be raised enough to align the conduction band. Therefore, the lateral BTBT primarily contributes to the ON-state current. However, an excessively thick ETL causes electric field degradation in the ETL because the ETL increases the distance from the gate. Consequently, the tunneling distance lengthens and the tunnel efficiency rapidly degrades. Fig. 5 shows how ETL thickness affects OFF-state current. The Si_xGe_{1-x} material possesses a low bandgap, which implies a high SRH generation current density. Therefore, thick Si_xGe_{1-x} ETL produces a high SRH generation current. Regarding Si_xGe_{1-x} ETL structure, the intrinsic OFF-state current is dominated by SRH generation current because the bipolar BTBT current is suppressed. Therefore, the OFF-state current increases as the ETL thickness increases because of the high SRH generation current in the Si_xGe_{1-x} material region.

B. ETL Doping Effect

Fig. 7 illustrates how the doping effect influences the ETL tunnel FET. For p-channel tunnel FET operation, an ETL with a high n-type doping level requires more negative gate voltage to produce a P^+ inversion layer. Therefore, an ETL with a high n-type doping concentration possesses a low BTBT threshold

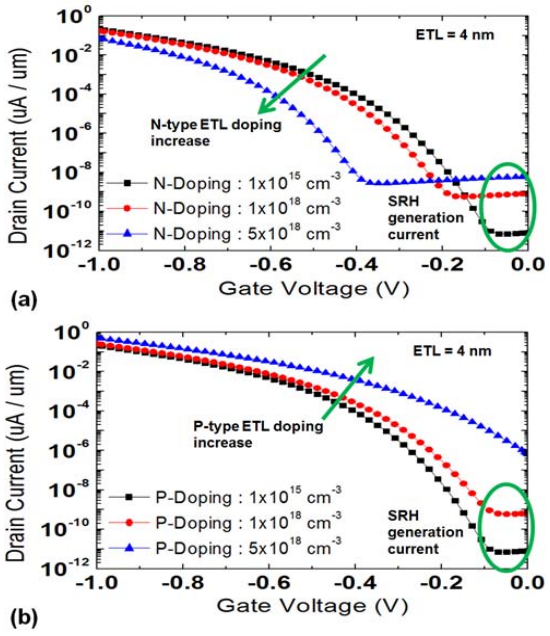

Fig. 7. Transfer characteristics of the ETL tunnel FET with different ETL doping type and concentration. (a) *n*-type ETL doping and (b) *p*-type ETL doping. The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL is 4-nm thick.

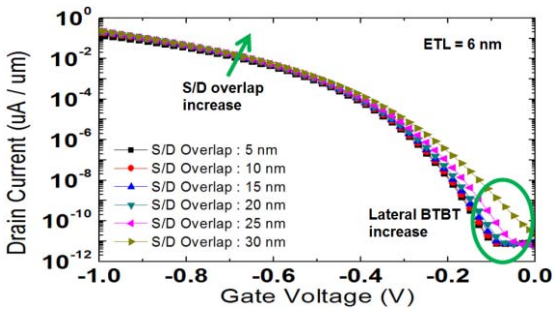

Fig. 8. Transfer characteristics of the ETL tunnel FETs with various gate-to-source and drain overlap length. The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL is 6-nm thick.

voltage and a low ON-state BTBT current. Conversely, an ETL with a high *p*-type doping concentration produces the opposite effect because little negative gate voltage is required. The influence of the ETL doping effect on the intrinsic OFF-state current was also analyzed. Regarding both the *n*-type doped and *p*-type doped ETL, a high doping concentration causes a short carrier lifetime, which increases the SRH generation current [25]. Thus the OFF-state current increases as the doping concentration increases. Regarding the heavily doped *p*-type ETL, BTBT occurs early and dominates the OFF-state current. Consequently, the OFF-state current increases abruptly, as illustrated in Fig. 7(b) (triangular symbol).

C. Source and Drain Overlap Length

Vertical tunneling is the key element of the ETL structure. The tunnel region is ideally determined by the gate-to-source and drain overlap length. Fig. 8 shows the transfer characteristics of the ETL tunnel FET with various overlap lengths. As expected, the ON-state BTBT current increase

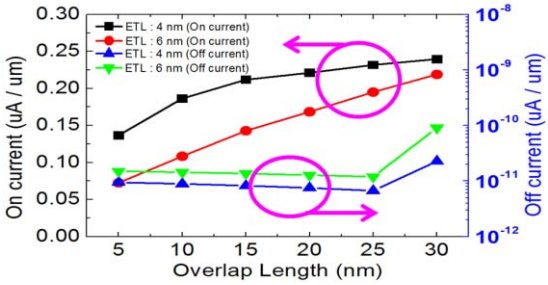

Fig. 9. ON-state and OFF-state current as a function ofgate-to-source and drain overlap length. The ETL thickness is 4 and 6 nm. ON-state and OFF-state are defined at $V_G = -1$ V, $V_D = -0.5$ V and $V_G = 0$ V, $V_D = -0.5$ V, respectively.

when the overlap length increases, but the rate of increment does not exhibit linear properties as shown in Fig. 9. Certain researches attribute this enhancement degradation to only the series resistance effect [30]. The simulation results produced in the study indicate that tunneling orientation is another crucial component of the nonlinear property. The tunnel path of the ETL tunnel FET is not completely vertical, and accompanies lateral orientation because of the potential difference in the ETL. The variation in the potential along the overlap region is attributed to the built-in junction potential and the series resistance effect [30]. The potential in the ETL is affected by the gate control ability and the built-in junction potential. The potential profile simulated at $V_G = -1$ V and $V_D = V_S = 0$ V indicates that the potential varies along the overlap region even without current flow. At the channel edge of the overlap region, the potential in the ETL is affected by the N^+ source and the lightly doped Si channel. However, the potential near the gate edge is affected by only the N^+ source. The difference in potential between the gate edge and the channel edge is 0.1 V when ETL = 6 nm and when the drain is biased at -0.5 V, the difference increases to 0.25 V. The increase in the difference in potential could be attributed to the series resistance effect in the ETL. Therefore, tunneling would most likely occur at the channel edge of the overlap region because of the difference in potential, causing current crowding. Consequently, the current enhancement caused by increasing the overlap length becomes weaker. Fig. 9 also indicates that OFF-state current increases abruptly when the overlap length excessively increases. This is attributed to the earlier occurrence of lateral BTBT in the ETL caused by the shrinkage of the depletion region. Fig. 10 indicates that the minimal SS also degrades when the overlap length increases. This implies that the additional contribution of the lateral BTBT, which occurs at low current levels, produces more unfavorable SS behavior than does pure vertical tunneling. Fig. 11 illustrates the band diagram of the ETL region at $V_G = -0.05$ V, $V_D = -0.5$ V. The early occurrence of lateral BTBT was discovered in the device with a long overlap length.

D. ETL Structure Enhancement

Fig. 12 compares the characteristics of the all-silicon lateral tunnel FET, the all-$Si_{0.5}Ge_{0.5}$lateral tunnel FET, and the $Si_{0.5}Ge_{0.5}$ ETL tunnel FET structure. The traditional lateral

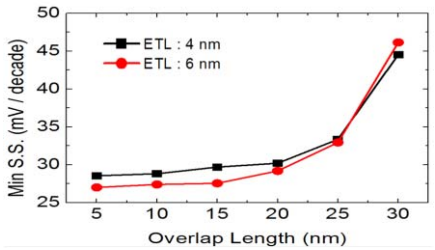

Fig. 10. Minimum SS behavior as a function of gate-to-source and drain overlap length. The ETL material is $Si_{0.5}Ge_{0.5}$ and the ETL thickness is 4 and 6 nm.

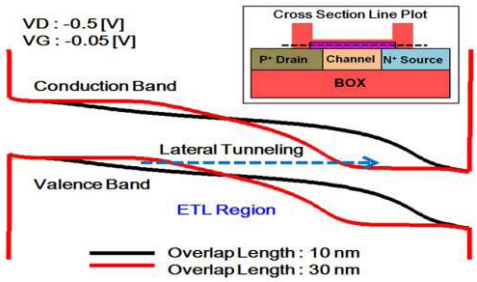

Fig. 11. Band diagram in the ETL region at $V_G = -0.05$ V and $V_D = -0.5$ V. The device with much longer overlap length shows the earlier occurrence of lateral band to band tunneling which does not occur with shorter overlap length.

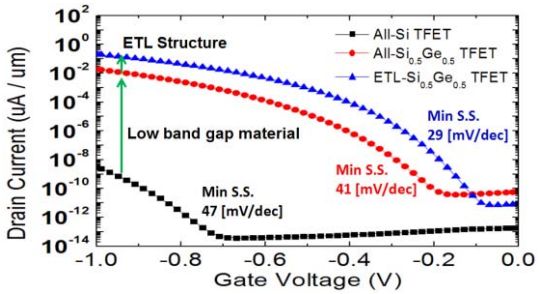

Fig. 12. Transfer characteristics of the all Si traditional tunnel FET, all $Si_{0.5}Ge_{0.5}$ traditional tunnel FET, and ETL tunnel FET. The ETL thickness is 4 nm and the gate-to-source and drain overlap length is 15 nm.

tunnel FET with low bandgap material exhibited a more favorable performance than does the all-silicon device. The optimized ETL structure with a vertical tunneling orientation further improved the tunnel FET performance. The SS behavior was also improved with the ETL structure.

E. Quantum Confinement Effect

Regarding tunnel FET devices, the BTBT occurs at the gate oxide interface. The quantum confinement effect is critical because of the severe band bending that occurs at the interface; however, existent literature has rarely discussed this effect because of the lack of elaborate models that can account for the correlation between the discrete quantized level and BTBT. Qualitative discussions regarding the effect of quantum confinement on the ETL structure are provided in this paper.

To study the quantization effect, the 1-D Schrödinger equation was used, employing default parameters included in the

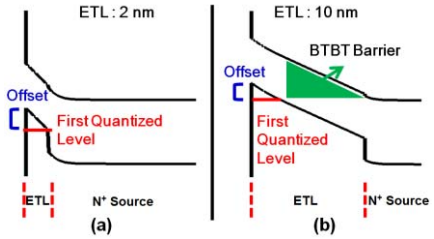

Fig. 13. ON-state ($V_D = -0.5$ V, $V_G = -1$ V) band diagram at the channel edge of the overlap region considering quantum confinement effect. 1-D Schrodinger solver with default parameters packaged in Sentaurus TCAD is applied to compute the quantized level in the ETL region. (a) ETL thickness is 2 nm. (b) ETL thickness is 10 nm.

Sentaurus TCAD to compute the quantized levels in the $Si_{0.5}Ge_{0.5}$ layer. Fig. 13 illustrates the ON-state band diagram. The ETL thickness ranged from 2 nm to 10 nm, and the offset between the valence band and the first quantized level was approximately 0.3–0.4 eV. With a thin ETL thickness (<4 nm), the first quantized level was located between the SiGe/Si interface and the oxide and SiGe interfaces shown in Fig. 13(a). The vertical BTBT was drastically suppressed because the first quantized level in the SiGe layer was located far below the Si conduction band (N^+ source). In addition, with a thin ETL, the ground level ignoring quantum confinement was also lower than the Si conduction band at $V_G = -1$V. Therefore, the vertical tunneling probability was diminished, and the lateral tunneling orientation dominated the ON-state current. With a thicker ETL thickness, the first quantized level was located in a triangular potential as shown in Fig. 13(b). As the quantized level aligned with the Si conduction band (N^+ source), the tunneling barrier is still determined by the ETL material bandgap. In this scenario, shifting the device onset voltage was the primary effect of quantization. The OFF-state bipolar tunneling current was increasingly suppressed by the quantization effect. The effects of quantization vary according to the degree of surface band bending at the interface. The ON-state current degraded because of the high onset voltage, which was caused by the strong surface band bending. Therefore, the SS behavior degraded because of the quantization effect.

This qualitative analysis suggests that the quantum confinement effect causes the performance of the ETL structure to weaken. All of the tunnel FET structures likely suffer from such effects for the same reasons. However, comprehensive models must be developed to quantitatively study the quantization effect.

F. Summary

Fig. 14 summarizes the effects of the ETL structure parameters, comprising ETL thickness, the doping effect, and gate-to-source and drain overlap length. Regarding the traditional tunnel FET structure, applying a small bandgap material (high concentration of Ge in Si_xGe_{1-x}) improved the ON-state current and increased the OFF-state current (star symbol). With the ETL structure, the performance of the ON-state and OFF-state characteristics improved. Controlling ETL thickness is

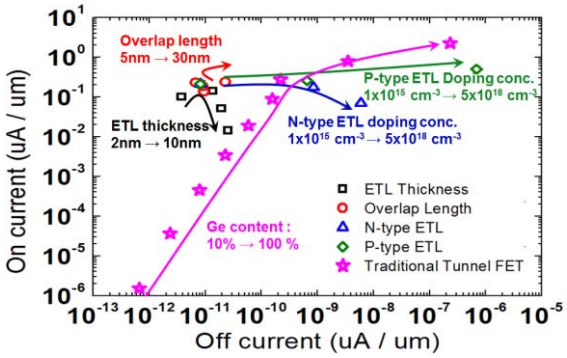

Fig. 14. Comparison of the ON-state current and OFF-state current with different ETL design parameters. The ranges of the parameters are inserted into the figure. The increment of the Ge content between two steps is 10%. The increment of the ETL thickness and overlap length are 2 nm and 5 nm, respectively. The n-type and p-type ETL concentration is 1×10^{15}, 1×10^{18} and 5×10^{18} cm^{-3}.

critical in optimizing the ETL tunnel FET. The results of this paper suggest that the proper ETL thickness, without considering quantization, is 4–6 nm (square symbol). A long gate-to-source and drain overlap length extended the tunneling region and increased the ON-state BTBT current. However, the amount that the ON-state BTBT current could increase was limited because of lateral tunneling and series resistance (circle symbol). The minimal SS increased as the overlap length increased because of the addition contribution of the lateral tunneling. ETL doping could modulate the onset voltage of the BTBT, but this process required addressing the OFF-state current increment. A high ETL doping concentration produced a high SRH generation current because of the short carrier lifetime (diamond and triangular symbols).

V. Conclusion

In this paper, a feasible and novel vertical-tunneling device structure, namely, the ETL tunnel FET, was proposed and its intrinsic characteristics were extensively investigated. The performance of $Si_{0.5}Ge_{0.5}$ ETL tunnel FET were unremarkable because of the process consideration; however qualitative analyses showed obvious performance enhancement in the proposed device compared with the tradition silicon tunnel FET structure. Therefore, ETL structures that integrate novel hetero-materials and advanced process nodes remain promising device considering the design concepts and fabrication feasibility.

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Bing-Yue Tsui (S'87-M'93-SM'01) received the Ph.D. degree from the National Chiao-Tung University, Hsinchu, Taiwan, R. O. C., in 1992. He is currently a Professor with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

Pei-Yu Wang received the B.S. degree from the National Chiao Tung University, Hsinchu, Taiwan, R. O. C., in 2009. He is currently working toward the Ph.D. degree at the National Chiao Tung University, Hsinchu Taiwan, R. O. C..