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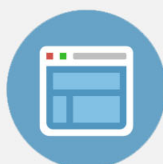
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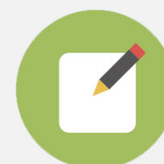

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Reduction of defect formation in amorphous indium-gallium-zinc-oxide thin film transistors by N_2O plasma treatment

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An abnormal sub-threshold leakage current is observed at high temperature in amorphous indium-gallium-zinc-oxide thin film transistors (a-IGZO TFTs). This phenomenon occurs due to a reduced number of defects in the device's a-IGZO active layer after the device has undergone N_2O plasma treatment. Experimental verification shows that the N_2O plasma treatment enhances the thin film bonding strength, thereby suppressing the formation of temperature-dependent holes, which are generated above 400 K by oxygen atoms leaving their original sites. The N_2O plasma treatment devices have better stability performance than as-fabricated devices. The results suggest that the density of defects for a-IGZO TFTs with N_2O plasma treatment is much lower than that in as-fabricated devices. The N_2O plasma treatment repairs the defects and suppresses temperature-dependent sub-threshold leakage current. *© 2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4832327]

I. INTRODUCTION

Recently, portable electronic products combined with display, memory,[1–5] and logic devices have been a tendency in modern digital age. As the size and resolution of active matrix displays increase, transparent oxide-based thin-film transistor (TFT) devices with fast response enable the design of peripheral circuits, where deposition of high uniform film at low temperatures such as room temperature (RT)[6,7] and good conducting mobility are required. Also, these characteristics allow for fabrication of flexible displays and computers on inexpensive substrates.[8] In particular, amorphous-$InGaZnO_4$ (a-IGZO) TFTs have several advantages over other transparent conducting oxides, such as high field-effect mobility,[9–13] small sub-threshold swing,[14] good short-range uniformity, and high electrical reliability. Moreover, amorphous oxide semiconductor-based materials are expected to be adopted as nonvolatile memory devices.[2,15–17] In order to achieve practical application of a-IGZO TFTs in active-matrix backplanes of future generations of large active-matrix liquid-crystal displays (AMLCDs) and organic light-emitting diode panels (OLEDs), some problems still remain to be improved, such as the forming of sub-threshold leakage current at high temperature, instability under light illumination,[18–22] and uncertainty over environmental change.[23–27]

In this study, we investigate the temperature dependence of a-IGZO TFTs using energy band diagrams. Moreover, we fabricate high-performance a-IGZO TFTs with a N_2O-plasma treatment, and find that the abnormal subthreshold leakage current stretch-out phenomenon can effectively be suppressed by such treatment. In addition, the hysteresis windows by capacitance-voltage (C-V) measurement can be also significantly suppressed in the N_2O-plasma treated devices

II. EXPERIMENT

Figure 1 represents the schematic cross-section view of the a-IGZO TFT. Bottom gate coplanar a-IGZO TFTs were produced on glass substrate, and plasma enhanced chemical vapor deposition (PECVD) was applied to grow SiOx (300 nm) film as gate insulator over the patterned Ti/Al/Ti (50/200/50 nm) trilayer gate electrodes at 370 °C. The Ti/Al/Ti (50/200/50 nm) source/drain electrodes were formed by sputtering and then patterned in channel width/length dimensions of (W/L) = 5–30 μm/10 μm. A 30 nm thick a-IGZO film was deposited by dc magnetron sputtering system at room temperature, using a target of In:Ga:Zn = 1:1:1 atomic ratio, a plasma discharge power of 300 W, and an

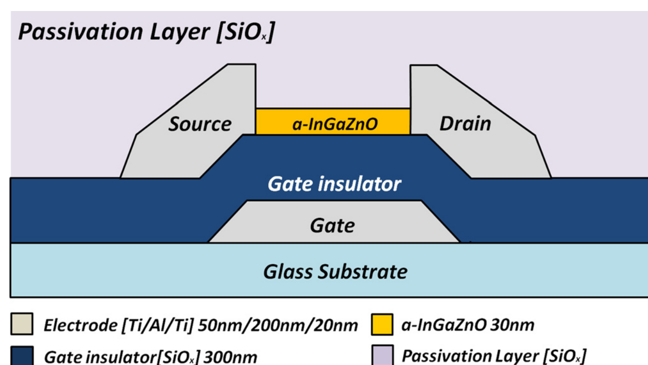

FIG. 1. The cross-section view of the bottom gate coplanar a-IGZO TFT device structure.

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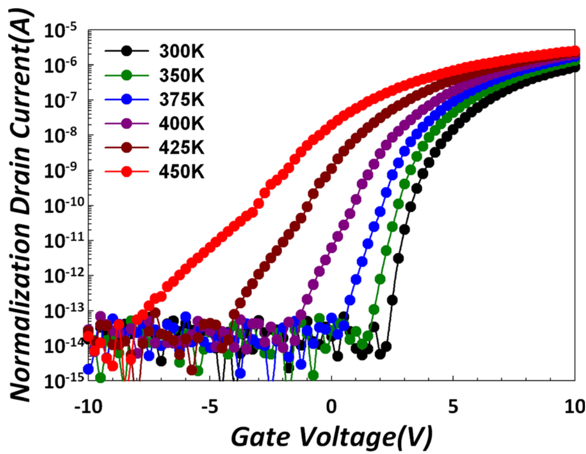

FIG. 2. Characteristics of V_G-NI_D transfer curves of devices without N_2O plasma treatment at temperatures between 300 K and 450 K.

ambiance of gas mixture ratio of O_2/Ar = 6.7% with a working pressure of 5 mTorr. After defining the active region, one group of TFTs was treated by N2O plasma to passivate the defects in the a-IGZO film. Finally, all devices were capped with a 200 nm SiO_X layer by PECVD at 170 °C, and sequentially annealed in an oven at 330 °C for 2 h. The electrical properties of a-IGZO TFTs were analyzed using an Agilent B1500A semiconductor device analyzer in a darkened environment.

III. EXPERIMENT RESULT AND DISCUSSIONS

Figure 2 shows the transfer characteristics of as-fabricated a-IGZO TFTs at different temperatures. As shown in this figure, the curves shift left with the increase of temperature. Also, the drain current in the entire gate voltage (V_G) region increases with increasing temperature. Below 375 K, the threshold voltage (V_T) decreases proportionally with an increase in temperature, with (V_T) defined as when normalized drain current (NID = ID × L/W, where L and W represent channel length and width, respectively) reaches 10^{-9} A. It is well known that the free electrons in oxide semiconductor materials are mainly due to the generation of point defects. Thermally excited oxygen atoms leave their original sites with free electrons left behind and vacancies are simultaneously created. The lower V_T observed at higher temperature can be attributed to more free electrons generated by point defects. Therefore, the threshold voltage substantially shifts towards the negative V_G direction at 450 K. Moreover, the transfer curve exhibits an apparent subthreshold leakage current stretch-out phenomenon above 400 K. The stretch-out phenomenon becomes serious with the increase in temperature. In addition, it should be noted that the transfer characteristics at room temperature (300 K) are reproducible after measurements at high temperature, implying that the change in transfer characteristics due to increasing temperature is reversible.

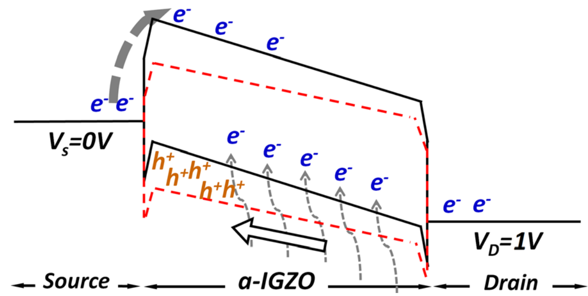

FIG. 3. Energy band diagram of a-IGZO TFTs at high temperature. Thermally induced holes accumulate at the source region and lead to the source side barrier lowering.

Figure 3 shows the energy band diagram of the proposed mechanism. The unique behavior of the subthreshold leakage current for a-IGZO TFTs appears at high temperature. We

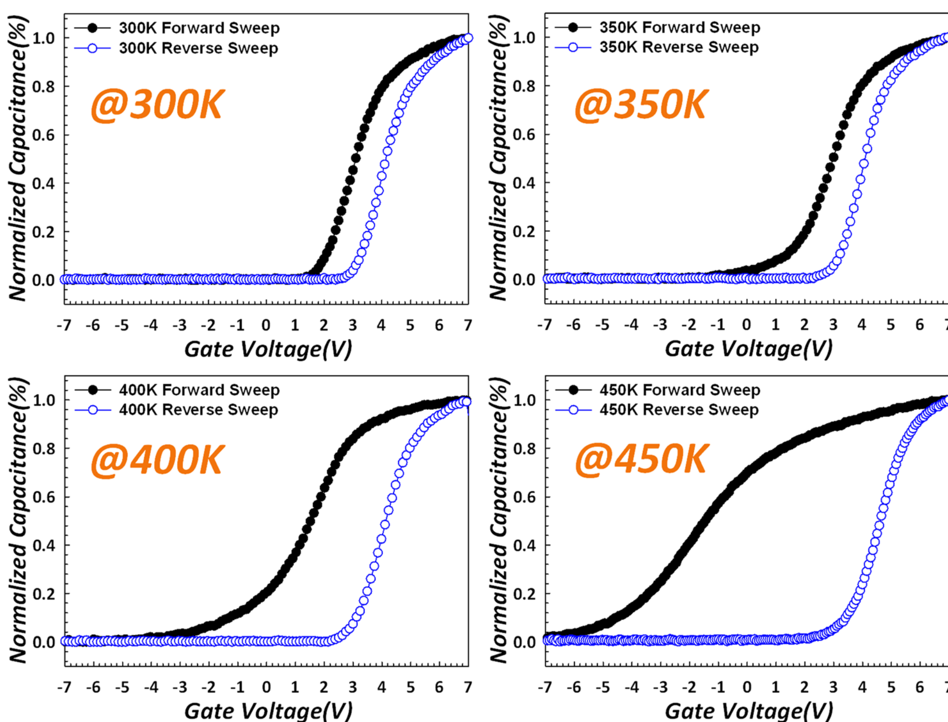

FIG. 4. Normalized capacitance of as-fabricated a-IGZO TFTs measured at different temperatures.

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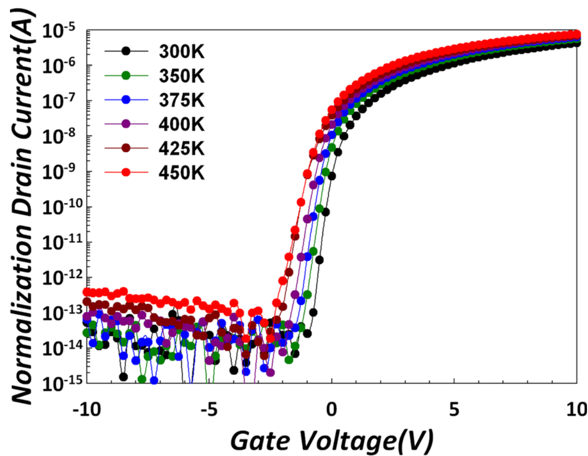

FIG. 5. Characteristics of V_G-NI_D transfer curves of devices with N_2O plasma treatment at temperatures between 300 K and 450 K.

have defined two distinctive regions in the transfer characteristics curve, the stretch-out and above-critical regions. For expediency, we define the critical voltage as when NID reaches 10^{-10} A. When the gate voltage is below critical voltage, thermally induced holes move to the source side due to the transverse electric field. Then, the holes accumulate at the source region and result in source side barrier lowering. The source side barrier lowering enhances electron injection from the source and causes the apparent subthreshold current leakage. Once the gate voltage is above critical voltage, however, the transfer characteristics are dominated by the barrier height between a-IGZO and source, with barrier height becomes much lower with increasing of gate voltage, making hole accumulation at the source region more difficult. Therefore, the transfer curve is separated into two regions with increasing gate voltage.

Figure 4 shows the capacitance-voltage (C-V) curve of as-fabricated a-IGZO TFTs at different temperatures. The device was measured under gate voltage from −7 V to 7 V as the forward sweep, and 7 V to −7 V as reverse sweep. After forward and reverse sweeping, a hysteresis phenomenon appears in as-fabricated a-IGZO TFTs. The shift of the transfer curve in the hysteresis loop can be attributed to the extra trap states generated during the deposition of the SiO_2 passivation layer by PECVD. Furthermore, the interface/oxide defects trap holes at negative gate voltage and electrons at positive gate voltage, respectively. At 300 K, the hysteresis phenomenon is caused by the captured electrons at positive gate voltage rather than hole carriers. Because of the low number of holes in IGZO TFTs at low temperature, it is thus difficult for many to be trapped at interface/oxide defects. However, it is worth noting that the hysteresis window increases with the increase in temperature. With gate voltage changing from −7 V to 7 V, the forward sweep curve shifts to the left with the increase in temperature. This left-moving tendency is caused by the trapped hole carriers at negative gate voltage at high temperature. This implies that the hole is induced by thermal energy. Therefore, the obvious hysteresis phenomenon appears in untreated a-IGZO TFTs at 450 K.

Figure 5 shows the transfer characteristics of a-IGZO TFTs with N_2O-plasma treatment at different temperatures. Compared with untreated a-IGZO TFTs, the curves shift only slightly to the left with increasing temperature. Also the apparent subthreshold leakage current stretch-out phenomenon is significantly suppressed at high temperature. This implies that the N_2O-plasma treatment can suppress defect generation at high temperature and enhance the atomic bonding strength. It becomes difficult for oxygen atoms to leave their original sites due to the stronger bonding energy. Moreover, the quantity of thermally induced holes is also reduced as fewer defects are formed. Thus only a few holes

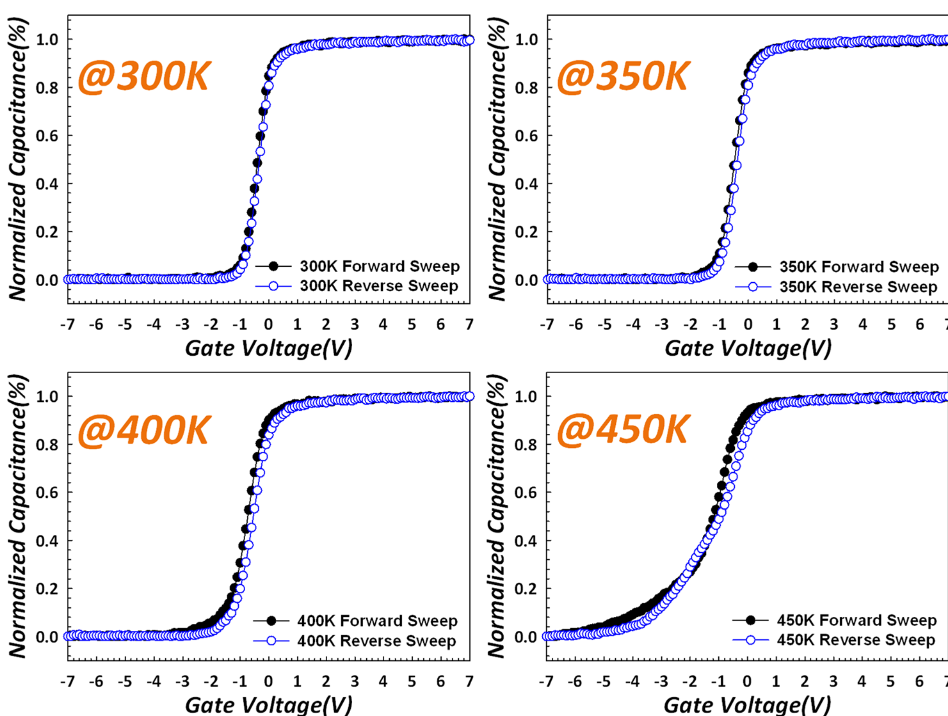

FIG. 6. Normalized capacitance of a-IGZO TFTs with N_2O plasma treatment measured at different temperatures.

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accumulate at the source barrier and the amount is too small to cause source side barrier lowering, which in turn suppresses subthreshold leakage current.

Figure 6 shows the capacitance-voltage (C-V) curve of N_2O-plasma treatment a-IGZO TFTs at different temperatures. The hysteresis phenomenon can be significantly suppressed in the device with N2O-plasma treatment. The N_2O-plasma treatment can improve SiO_2/IGZO interface properties as the oxygen-rich region effectively prevents damage during the SiO_2 deposition process. The shift in the transfer curve in the hysteresis loop can be clearly lessened due to the repairing of interface defects. Furthermore, the hysteresis phenomenon also lessened under high temperature. Therefore, N_2O-plasma treatment for a-IGZO TFTs can significantly enhance the stability of the performance of a-IGZO TFTs at high temperature.

IV. CONCLUSIONS

In conclusion, we have obtained better performance stability in a-IGZO TFTs with a N_2O plasma treatment on the a-IGZO channel region. For the as-fabricated device, the passivation layer deposition process can cause extra trap states due to PECVD plasma damage, which results in significant subthreshold current leakage stretch-out phenomenon at high temperatures. The N_2O-plasma treatment is applied to a-IGZO layer and improves the SiO2/IGZO interface property, as the oxygen-rich region effectively prevents damage during SiO_2 deposition process. The N_2O-plasma treatment therefore significantly enhances the performance stability of a-IGZO TFTs at high temperature. It is expected that N_2O-plasma will prove to be an effective surface treatment in other oxide semiconductor devices.

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