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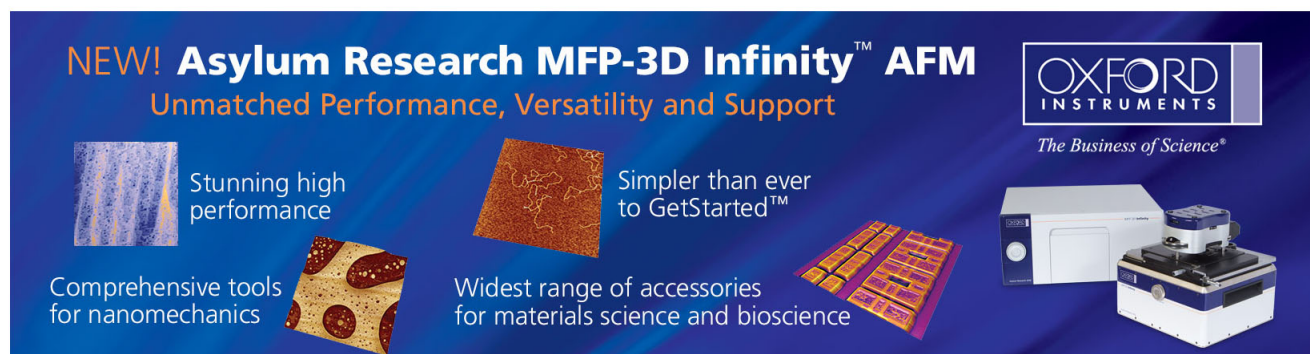
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## Double-metal-gate nanocrystalline Si thin film transistors with flexible threshold voltage controllability

Uio-Pu Chiou,<sup>1</sup> Jia-Min Shieh,<sup>2,3,a)</sup> Chih-Chao Yang,<sup>2</sup> Wen-Hsien Huang,<sup>1,2</sup> Yo-Tsung Kao,<sup>3</sup> and Fu-Ming Pan<sup>1,b)</sup>

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We fabricated nano-crystalline Si (nc-Si:H) thin-film transistors (TFTs) with a double-metal-gate structure, which showed a high electron-mobility ( $\mu_{FE}$ ) and adjustable threshold voltages ( $V_{th}$ ). The nc-Si:H channel and source/drain (S/D) of the multilayered TFT were deposited at 375 °C by inductively coupled plasma chemical vapor deposition. The low grain-boundary defect density of the channel layer is responsible for the high  $\mu_{FE}$  of 370 cm<sup>2</sup>/V-s, a steep subthreshold slope of 90 mV/decade, and a low  $V_{th}$  of -0.64 V. When biased with the double-gate driving mode, the device shows a tunable  $V_{th}$  value extending from -1 V up to 2.7 V. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4832072>]

Power consumption is one of the limiting factors for realizing high-performance ultimately scaled integrated circuits. Much effort has been done to address this limitation, and independently switched double-gate transistors are considered as one of the most promising solutions for the obstacle.<sup>1-3</sup> The double-gate transistor with the independent gate-driving capability can offer flexible controllability in the threshold voltage ( $V_{th}$ ) and can achieve a low off-state leakage current ( $I_{off}$ ) and a high on-state current ( $I_{on}$ ) in a single transistor. Because of the advantages, the double-gate transistor structure has also been implemented in the thin film transistor (TFT) technology to improve the electrical performance of the transistors. For example, Kandoussi *et al.* demonstrated that the dual-gate hydrogenated microcrystalline silicon ( $\mu$ c-Si:H) TFT structure had an efficient control of  $V_{th}$ .<sup>4</sup> However, the TFT device had poor electrical characteristics, such as field effect mobility ( $\mu_{FE}$ ) and subthreshold slope (S.S). To fabricate TFTs with a steep S.S and a high  $\mu_{FE}$ , it is essential to form the channel layer of low defect density. Therefore, the channel layer should have a high crystallinity for the improvement in the device performance of TFTs. Nano-crystalline Si (nc-Si:H) has been widely studied as the channel layer of high performance TFTs because of its tunable crystallinity,<sup>5-7</sup> high *in-situ* doping efficiency,<sup>8,9</sup> and simple fabrication process.<sup>10,11</sup> Lee *et al.* reported that nc-Si:H TFTs with the 300 nm-thick channel layer had an ultra-high mobility when the crystallinity of the channel layer reached 85%.<sup>12</sup> Our previous work used the continuous-wave laser-crystallization (CLC) technique to prepare a highly crystalline channel with a low tail-state density of  $3 \times 10^{19}$  eV<sup>-1</sup> cm<sup>-3</sup>.<sup>13</sup> In addition to the high crystallinity of the channel, heavily doped source/drain (S/D) regions are also important to the device performance of nc-Si:H TFTs. For fabrication of the S/D contacts, ion

implantation is commonly implemented for impurity doping. Metal silicides have also been used as S/D contacts of TFTs to achieve good electrical characteristics.<sup>14</sup> However, these fabrication methods require complex processes and, therefore, are not suitable for applications of large-area devices. Moreover, ion implantation can cause lattice damage in the S/D regions, and the succeeding activation process requires a high thermal budget. For applications of flexible or stackable three-dimensional (3D) electronics, low-temperature-processed TFT technology is desirable. It has been shown that high S/D conductivity and low contact resistance could be realized by *in-situ* doping in the nc-Si:H thin film with a low thermal budget.<sup>9</sup> Our previous study has shown that inductively coupled-plasma chemical vapor deposition (ICP-CVD) can produce Si thin films with a defect density as low as  $3 \times 10^{15}$  cm<sup>-3</sup> as a result of the high density plasma, which enhances the dissociation of reaction precursors.<sup>15</sup> Although defects are inevitably formed during the ICP plasma process, the crystallinity of Si thin films can be improved by the introduction of inert gases, such as Ar and Kr, in the precursor gas mixture as the diluting gas.<sup>16-18</sup> The inert gas in the SiH<sub>4</sub>/H<sub>2</sub> plasma can enhance dissociation and ionization of SiH<sub>4</sub> and H<sub>2</sub>, thereby increasing the density of H and SiH<sub>n</sub> ( $n = 1-3$ ) radicals and ions.<sup>6</sup> The ionized inert gas atoms produced in the high density plasma can moderately bombard and thus modify the growing Si thin film, resulting in a better crystallinity of nc-Si:H grains. In this study, we fabricated *in-situ* doped n<sup>+</sup> nc-Si:H TFT devices using ICP-CVD, and integrate the devices into a double-metal-gate structure. During the nc-Si:H deposition, Ar gas was added in the precursor gas mixture to improve the crystallinity of nc-Si:H grains. The double-metal-gate nc-Si:H TFT exhibits a tunable  $V_{th}$  ranging from -1 V up to 2.7 V when it was biased with the double-gate driving mode.

We first fabricated n<sup>+</sup> nc-Si:H TFTs with a single gate to study the effect of the Ar dilution on the electrical performance of the TFT device. The fabrication of the TFT started with the deposition of the *in-situ* doped n<sup>+</sup> nc-Si:H

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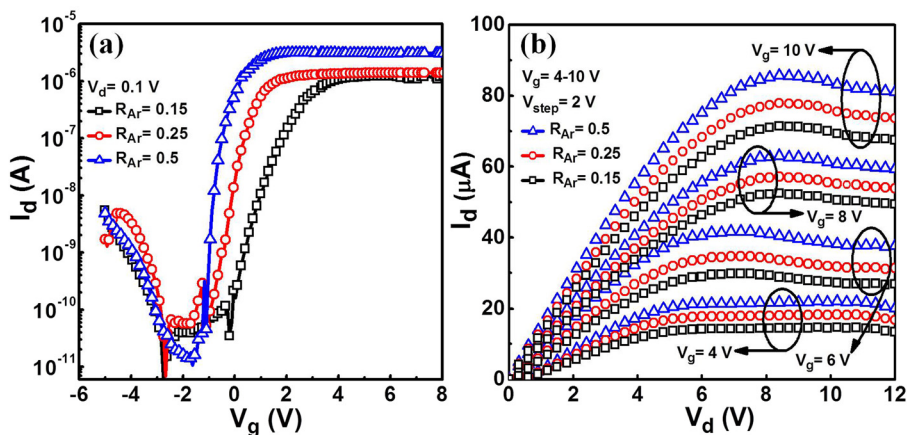


FIG. 1. (a) Transfer and (b) output characteristics of the top gate *in-situ* doped  $n^+$  nc-Si:H TFTs with different Ar dilution ratios. The drain current ( $I_d$ ) versus the gate voltage ( $V_g$ ) is plotted at a drain voltage ( $V_d$ ) of 0.1 V. Both the channel length ( $L$ ) and the width ( $W$ ) are  $60 \mu\text{m}$ .

S/D regions on the glass substrate by ICP-CVD using the  $\text{SiH}_4/\text{H}_2/\text{PH}_3$  gas mixture as the precursor, which was diluted by Ar gas with a dilution ratio ( $R_{\text{Ar}} = [\text{Ar}]/[\text{H}_2]$ ) from 0.15 to 0.5. After the S/D regions were patterned by photolithography, the intrinsic nc-Si:H channel layer of 100 nm in thickness was deposited on the glass plate using the same  $R_{\text{Ar}}$  as the  $n^+$  nc-Si:H S/D layers and subsequently patterned. The 100 nm-thick  $\text{SiO}_2$  gate dielectric layer was then deposited on the channel layer, followed by the e-gun evaporation deposition and the patterning of a 200 nm-thick Al thin film for the gate electrode. A 300 nm-thick  $\text{SiO}_2$  thin film was used as the passivation layer to prevent the TFT device from contamination, humidity, or degradation. The final process step was to fabricate Al metal pads on the  $\text{SiO}_2$ -passivated TFT for electrical measurements. For fabrication of the double-metal-gate nc-Si:H TFT, a 150 nm-thick TaN metal layer and a 25 nm-thick  $\text{SiO}_2$  gate dielectric layer were first deposited on the glass substrate, followed by the same fabrication process described above for the single-gate TFT device.

Figure 1 shows the transfer and output characteristics of the nc-Si:H TFTs with the channel length ( $L$ ) and width ( $W$ ) both of  $60 \mu\text{m}$ . Some of the device performance of the TFTs prepared with different  $R_{\text{Ar}}$  values are listed in Table I. Figure 1(a) represents the drain current-gate voltage ( $I_d$ - $V_g$ ) curves of the TFT operated at the drain voltage ( $V_d$ ) of 0.1 V. The S.S becomes steeper and the  $V_{\text{th}}$  is lower when the  $R_{\text{Ar}}$  is increased. The device with  $R_{\text{Ar}}=0.5$  shows better performance as compared with other devices with other dilution ratios, including a high turn-on current, very low  $V_{\text{th}}$  ( $-0.64 \text{ V}$ ), a high  $\mu_{\text{FE}}$  ( $370 \text{ cm}^2/\text{V}\cdot\text{s}$ ), and an extremely low S.S ( $90 \text{ mV/decade}$ ). Figure 1(b) shows the output characteristics of the TFTs as a function of the  $R_{\text{Ar}}$  at different gate voltages. It can be clearly seen that the TFT with  $R_{\text{Ar}}=0.5$  has the largest driving current for all gate voltages. The better performance of the TFT with  $R_{\text{Ar}}=0.5$  may result from a

higher  $\mu_{\text{FE}}$  of charge carriers and the smaller  $V_{\text{th}}$ . In general, better electrical characteristics can be obtained for nc-Si:H TFTs when the crystallinity of the channel layer is improved and the series resistance between the S/D regions and the channel layer is reduced. As described later, the better performance of the nc-Si:H TFT with  $R_{\text{Ar}}=0.5$  can be ascribed to the low defect density and the low ohmic contact as a result of the efficient *in-situ* doping during the S/D deposition.

Figure 2(a) shows the cross-sectional transmission electron micrograph (TEM) of the double-metal-gate nc-Si:H TFT. For clarity, only part of the nc-Si:H channel layer was shown in the figure. The high resolution TEM (HRTEM) image of a selected area in the channel layer is shown in Fig. 2(b). The marked lattice spacing indicates the presence of crystalline Si nanograins. The HRTEM image clearly shows that, in the channel layer, nanometer-sized Si grains are embedded in the amorphous Si (a-Si:H) matrix. Figure 2(c) shows X-ray diffraction (XRD) spectra of the nc-Si:H channel layer for different  $R_{\text{Ar}}$  values. The three peaks situated at  $28.4^\circ$ ,  $47.2^\circ$ , and  $56^\circ$  correspond to the (111), (220), and (311) lattice planes of Si, respectively. The Si nano-grains

TABLE I. The device performance of the top gate *in-situ* doped  $n^+$  nc-Si:H TFT with different Ar dilution ratios for the deposition of  $n^+$  and i-nc-Si:H layers.

| $[\text{Ar}]/[\text{H}_2]$ | $V_{\text{th}}(\text{V})$ | S.S(V/decade) | $\mu_{\text{FE}}(\text{cm}^2/\text{V}\cdot\text{s})$ | $R_c \times W(\text{M}\Omega - \mu\text{m})$ |
|----------------------------|---------------------------|---------------|--|--|
| 0.15                       | 1.66                      | 0.18          | 152  | 10.7   |
| 0.25                       | 1.43                      | 0.11          | 280  | 3.62   |
| 0.5                        | -0.64                     | 0.09          | 370  | 1.07   |

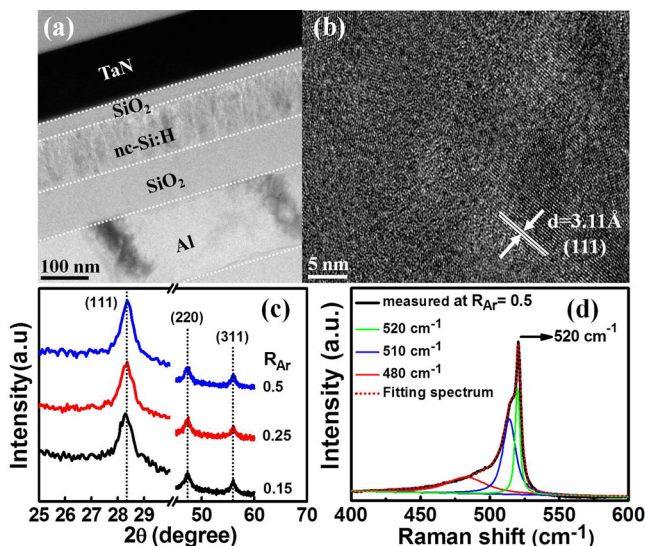


FIG. 2. (a) Cross-sectional TEM image of the double-metal-gate nc-Si:H TFT; (b) the high resolution TEM image of a selected area of the channel layer shown in (a); (c) XRD spectra of the nc-Si:H channel layer with different  $R_{\text{Ar}}$  ratios. (d) Raman spectra of nc-Si:H channel layer for the  $R_{\text{Ar}}=0.5$ .



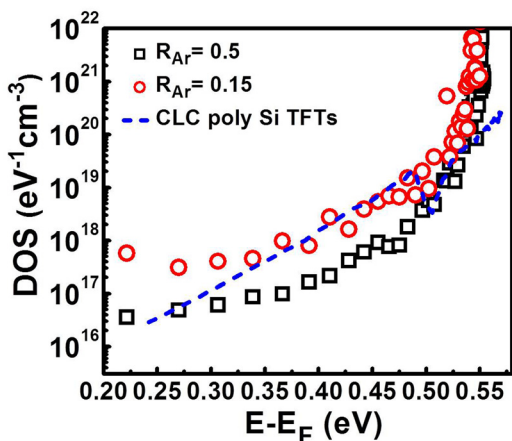


FIG. 3. The energy distribution of the density of states for the top gate *in-situ* doped  $n^+$  nc-Si:H TFTs with  $R_{Ar}=0.15$  and  $0.5$ . For comparison, the DOS distribution of a CLC-fabricated poly-Si TFT device is also presented.

embedded in the nc-Si:H thin film are about 33 to 43 nm according to Scherer's formula.<sup>19</sup> The peak intensity changes insignificantly when  $R_{Ar}$  is increased from 0.15 to 0.5, indicating that the crystallinity of the Si nanograins has a trivial dependence on the Ar dilution ratio.

Figure 2(d) shows the Raman spectrum of the nc-Si:H channel layer prepared with  $R_{Ar}=0.5$ . The Raman spectrum can be decomposed into three Gaussian peaks by curve fitting.<sup>20</sup> These three peaks are assigned to the transverse optical (TO) mode of crystalline silicon ( $520\text{ cm}^{-1}$ ), defects in the crystalline phase ( $510\text{ cm}^{-1}$ ), such as bond dilation at grain boundaries,<sup>21</sup> and the a-Si:H phase ( $480\text{ cm}^{-1}$ ).<sup>22</sup> The crystallinity ( $X_c$ ) of an nc-Si:H thin film can be estimated in terms of the intensity of the three Raman peaks. The  $X_c$  is defined by the ratio of the intensity sum of the two peaks at  $520\text{ cm}^{-1}$  and at  $510\text{ cm}^{-1}$  to the sum of the three peaks.<sup>22</sup> From the curve-fitted Raman spectrum, the ICP-CVD deposited nc-Si:H channel layer has a crystallinity of 69.3%. The high crystallinity of the channel layer results in a low bulk defect density, reducing carrier scattering and thus promoting the  $\mu_{FE}$ . In addition, because the S.S can be decreased by reducing the bulk defect density of the channel,<sup>23</sup> the high crystallinity of the nc-Si:H layer should yield a small S.S for the TFT device. According to Raman spectra of nc-Si:H layers prepared with a  $R_{Ar} < 0.5$  (not shown), the change in  $R_{Ar}$  has a little effect on the crystallinity of nc-Si:H grains in the channel layer.

In order to study bulk defects of the nc-Si:H channel layer, we used the field effect conductance (FEC) method<sup>24,25</sup> to extract the density of states (DOS) of the nc-Si:H TFT with various Ar dilution ratios. From Fig. 3, when the  $R_{Ar}$  increases from 0.15 to 0.5, the tail-state density at  $E-E_F=0.52\text{ eV}$  decreases from  $6.9 \times 10^{19}$  to  $2.6 \times 10^{19}\text{ eV}^{-1}\text{ cm}^{-3}$ , where  $E_F$  is the midgap energy. The low tail-state density of the nc-Si:H layer is nearly the same as that of our previously reported polycrystalline silicon (poly-Si) TFTs fabricated by CLC method.<sup>13</sup> The deep-state density at  $E-E_F=0.22\text{ eV}$  also reduces from  $5.69 \times 10^{17}$  to  $3.57 \times 10^{16}\text{ eV}^{-1}\text{ cm}^{-3}$ . The tail-state density and the deep-state density of nc-Si:H TFTs are associated with intra-grain defects ( $D_{intra}$ ) and grain boundaries defects ( $D_{GB}$ ) in the nc-Si:H layer, respectively.<sup>26</sup> The  $D_{intra}$  of the channel layer is defects present in nc-Si:H grains, and the  $D_{GB}$  is defects formed at the grain boundary between the a-Si:H matrix and the nc-Si:H. The lower  $D_{intra}$  and  $D_{GB}$  in the nc-Si:H channel layer with a larger  $R_{Ar}$  indicate that the Ar gas in the plasma during nc-Si:H deposition is beneficial to the reduction of the defect density of the channel layer. A lower tail-state density can enhance the  $\mu_{FE}$ , and a lower deep-state density can decrease the  $V_{th}$  and the S.S.<sup>26,27</sup> Therefore, the high  $\mu_{FE}$  of  $370\text{ cm}^2/\text{V}\cdot\text{s}$  and steep S.S of  $90\text{ mV}/\text{decade}$  of the nc-Si:H TFTs with  $R_{Ar}=0.5$  can be ascribed to the low  $D_{intra}$  and  $D_{GB}$  densities, respectively. Moreover, the hydrogen plasma is useful to passivate the tail-state.<sup>26,27</sup> During the deposition of the nc-Si:H thin film, the high-density ICP plasma enhances a high dissociation rate of hydrogen gas, resulting in efficient passivation of dangling bonds at grain boundaries.

According to four point probe resistivity measurements, the resistivity of the  $n^+$  nc-Si:H layer decreases with increasing  $R_{Ar}$ , and the resistivity is as low as  $0.09\text{ }\Omega\cdot\text{cm}$  for  $R_{Ar}=0.5$ . The low resistivity of the  $n^+$  nc-Si:H layer is due to the high doping efficiency of the *in-situ* doping technique.<sup>8,9</sup> The total resistance ( $R_{tot}$ ) from the source to drain is the series resistance of the channel resistance ( $R_{CH}$ ) and the contact resistance ( $R_C$ ).<sup>9,28</sup> Decreasing the  $R_{tot}$  can improve the carrier mobility. From the output characteristics of the  $I_d-V_d$  plot,  $R_{tot}$  can be determined by  $\partial V_d/\partial I_d$  in the linear regime. The transmission line method<sup>28</sup> is used to extract  $R_{CH}$  and  $R_C$  from the plot of  $R_{tot} \times W$  versus the channel length at different gate voltages as shown in Fig. 4(a). The  $R_{CH}$  is the slope of the plot, and  $R_C$  is determined from the intercept with the Y-axis. Figure 4(b) shows the  $R_{CH}$  and  $R_C \times W$  for the device with a channel length of

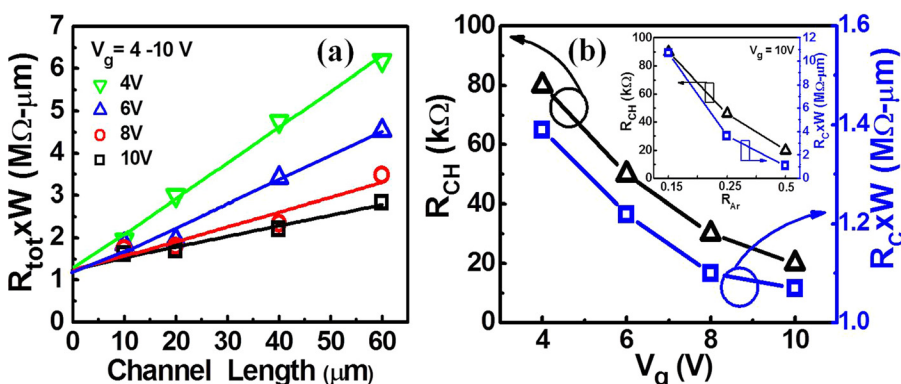


FIG. 4. (a) The plot of  $R_{tot} \times W$  versus the channel length (from 10 to  $60\text{ }\mu\text{m}$ ) at different gate voltages (from 4 to 10 V); (b) the  $R_{CH}$  and  $R_C \times W$  for the  $n^+$  nc-Si:H TFT with  $R_{Ar}=0.5$  as a function of the gate voltage. The device had a channel length of  $60\text{ }\mu\text{m}$  and was operated at  $V_d=0.1\text{ V}$ . The inset shows the  $R_{CH}$  and  $R_C$  of the nc-Si:H TFT (measured at  $V_g=10\text{ V}$ ) as a function of  $R_{Ar}$ .

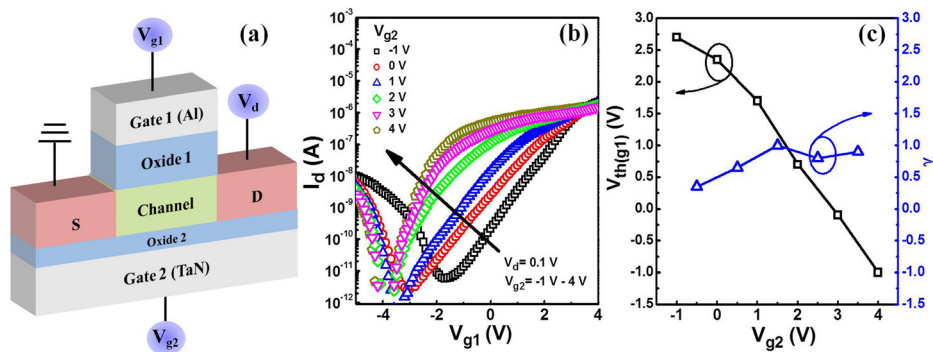


FIG. 5. (a) The schematic structure of the double-metal-gate nc-Si:H TFT; (b) transfer characteristics of the device.  $V_{g1}$  is the driving gate and  $V_{g2}$  is the  $V_{th}$ -control gate; (c) the extracted  $V_{th}$  of g1 and the back-gate-effect factor  $\gamma$  as a function of  $V_{g2}$ .

60  $\mu\text{m}$  and the  $R_{Ar} = 0.5$  at various gate voltages. The  $R_{CH}$  decreases from 80 to 20 k $\Omega$  and the  $R_C \times W$  decreases from 1.39 to 1.07 M $\Omega$ - $\mu\text{m}$  when  $V_g$  is increased from 4 to 10 V. The inset in Fig. 4(b) presents the dependence of the  $R_{CH}$  and  $R_C$  of the nc-Si:H TFT (measured at  $V_g = 10$  V) on  $R_{Ar}$ . Both the  $R_{CH}$  and  $R_C$  greatly decrease when  $R_{Ar}$  increases. When  $R_{Ar}$  increases from 0.15 to 0.5,  $R_{CH}$  declines from 90 to 20 k $\Omega$ , and  $R_C \times W$  decreases from 10.7 to 1.07 M $\Omega$ - $\mu\text{m}$ . The low  $R_{CH}$  and  $R_C$  of the nc-Si:H TFT can be ascribed to the low defect density of the nc-Si:H channel and the S/D layer as revealed by the density of states discussed above. Because of the low channel and S/D contact resistances, both the driving current and the S.S of the  $n^+$  nc-Si:H TFT are significantly improved. In combination with the above discussions about the crystallinity determination, defect analysis, and resistance measurement, we believe that the better  $n^+$  nc-Si:H TFT performance with increasing  $R_{Ar}$  results from the lower  $R_{tot}$ , which is a result of a smaller  $D_{GB}$  density.

The  $n^+$  nc-Si:H TFT of this work can be further integrated into the double-metal-gate stack scheme for additional flexibility in the  $V_{th}$  control. As shown in Fig. 5(a), the nc-Si:H channel of the double-metal-gate TFT is sandwiched between the bottom and top gate oxides to form the TFT structure with double-gate electrodes. The double-metal-gate structure consists of a sputter-deposited TaN bottom gate (g2) and a top E-gun-evaporation-deposited Al gate (g1). The g1 and g2 are used as the driving gate and the  $V_{th}$ -control gate, respectively. The use of metal as the gate material has advantages of avoiding poly-Si depletion effect and improving the drive current when the device is scaled down beyond 45 nm node. In addition, the fabrication process of metal gates generally requires a thermal budget lower than that of poly-Si gates. The low temperature nc-Si:H channel technology is therefore compatible with the fabrication of the metal gates for the double-metal-gate nc-Si:H TFT. Figure 5(b) shows the  $I_d$ - $V_{g1}$  characteristics of the double-metal-gate nc-Si:H TFT as a function of the back gate voltage ( $V_{g2}$ ). The  $I_d$  versus  $V_{g1}$  curves were measured at  $V_d = 0.1$  V and the  $V_{g2}$  varied from  $-1$  to 4 V. Figure 5(c) shows that the  $V_{th}$  of the device can be adjusted more positively or negatively by changing the bottom gate bias  $V_{g2}$ . Therefore, the double-metal-gate TFT can be free from the floating body effect. Also shown in Fig. 5(c) is the back-gate-effect factor  $\gamma$ ,<sup>1,29</sup> which is defined by  $|\Delta V_{th(g1)}/\Delta V_{g2}|$ . The calculated  $\gamma$  values of the double-metal-gate nc-Si:H TFT are in the range between 0.35 and 0.9. These values are comparable to the double-gate

MOSFET that has a poly-Si channel.<sup>1,30</sup> This indicates that the  $V_{th}$  of the g1 of the device can be effectively modulated by the back gate bias  $V_{g2}$ . Masahara *et al.* have proposed a linear potential distribution model to explain the back-gate effect on the  $V_{th}$  modulation for double-gate devices.<sup>1</sup> In the case of the double-metal-gate nc-Si:H TFT, when the back gate is biased negatively, the nc-Si:H channel surface near the g2 is essentially depleted. As the device is turned on by  $V_{g1}$ , conducting carriers are mainly induced near the g1 side; the narrow conduction path results in a low channel current. When inversion occurs near the side of the positively biased g2, a larger  $V_{g2}$  leads to a lower  $V_{th}$  value and a higher channel current. A small change in the  $V_{g2}$  will cause a large potential change at the g1 side,<sup>1</sup> resulting in a higher  $\gamma$  and the better  $V_{th}$ -controllability by the back gate bias  $V_{g2}$ . Because of the merits described above, the double-metal-gate nc-Si:H TFT technology with the tunable  $V_{th}$  capability is very promising for applications in low power circuits.<sup>1,29</sup> For example, in the standby mode, a lower leakage current can be achieved by raising the  $V_{th}$  of the transistors. While in the active mode, the  $V_{th}$  can be adjusted to a lower value to provide sufficient driving current. Moreover, due to the very low process temperature, the double-metal-gate nc-Si:H TFT technology is suitable for future 3D electronics.<sup>31</sup>

In conclusion, we have fabricated a top gate *in-situ* doping  $n^+$  nc-Si:H TFT on the glass substrate using ICP-CVD. By varying the Ar dilution ratio, we can prepare nc-Si:H channel layers of low grain boundary defect density. In combination with the *in-situ* doped nc-Si:H S/D layer of low resistivity, the device exhibits a high  $\mu_{FE}$  of 370 cm<sup>2</sup>/V-s and an extremely low S.S of 90 mV/decade. We also integrated the nc-Si:H TFT technology with the double-metal-gate structure to obtain additional flexibility in the  $V_{th}$  control. The double-metal-gate nc-Si:H TFT exhibits tunable  $V_{th}$  varying from  $-1.0$  V up to 2.7 V with the back-gate-effect factor  $\gamma$  in the range between 0.35 and 0.9. This technique is suitable for the application of future 3D electronics, which require transistors of high efficiency, low cost, and low operation voltage.

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