

High-k shallow traps observed by charge pumping with varying discharging times

Szu-Han Ho, Ting-Chang Chang, Ying-Hsin Lu, Bin-Wei Wang, Wen-Hung Lo, Ching-En Chen, Jyun-Yu Tsai, Hua-Mao Chen, Kuan-Ju Liu, Tseung-Yuen Tseng, Osbert Cheng, Cheng-Tung Huang, Tsai-Fu Chen, and Xi-Xin Cao

Citation: Journal of Applied Physics 114, 174506 (2013); doi: 10.1063/1.4828719

View online: http://dx.doi.org/10.1063/1.4828719

View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/114/17?ver=pdfcov

Published by the AIP Publishing

Articles you may be interested in

Temperature dependence of the resistive switching-related currents in ultra-thin high-k based MOSFETs J. Vac. Sci. Technol. B **31**, 022203 (2013); 10.1116/1.4789518

Investigation of extra traps measured by charge pumping technique in high voltage zone in p-channel metal-oxide-semiconductor field-effect transistors with HfO2/metal gate stacks

Appl. Phys. Lett. 102, 012106 (2013); 10.1063/1.4773914

Cross characterization of ultrathin interlayers in HfO2 high-k stacks by angle resolved x-ray photoelectron spectroscopy, medium energy ion scattering, and grazing incidence extreme ultraviolet reflectometry J. Vac. Sci. Technol. A **30**, 041506 (2012); 10.1116/1.4718433

Investigation on interface related charge trap and loss characteristics of high-k based trapping structures by electrostatic force microscopy

Appl. Phys. Lett. 99, 223504 (2011); 10.1063/1.3664222

The Relation Between Crystalline Phase, Electronic Structure, and Dielectric Properties in HighK Gate Stacks AIP Conf. Proc. **788**, 92 (2005); 10.1063/1.2062944



Re-register for Table of Content Alerts

Create a profile.



Sign up today!





High-k shallow traps observed by charge pumping with varying discharging times

Szu-Han Ho,¹ Ting-Chang Chang,^{2,3,a)} Ying-Hsin Lu,² Bin-Wei Wang,⁴ Wen-Hung Lo,² Ching-En Chen,¹ Jyun-Yu Tsai,² Hua-Mao Chen,⁵ Kuan-Ju Liu,² Tseung-Yuen Tseng,¹ Osbert Cheng,⁶ Cheng-Tung Huang,⁶ Tsai-Fu Chen,⁶ and Xi-Xin Cao⁴

¹Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

²Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan

(Received 26 July 2013; accepted 17 October 2013; published online 5 November 2013)

In this paper, we investigate the influence of falling time and base level time on high-k bulk shallow traps measured by charge pumping technique in n-channel metal-oxide-semiconductor field-effect transistors with HfO₂/metal gate stacks. N_T - $V_{high\ level}$ characteristic curves with different duty ratios indicate that the electron detrapping time dominates the value of N_T for extra contribution of I_{cp} traps. N_T is the number of traps, and I_{cp} is charge pumping current. By fitting discharge formula at different temperatures, the results show that extra contribution of I_{cp} traps at high voltage are in fact high-k bulk shallow traps. This is also verified through a comparison of different interlayer thicknesses and different Ti_xN_{1-x} metal gate concentrations. Next, N_T - $V_{high\ level}$ characteristic curves with different falling times ($t_{falling\ time}$) and base level times ($t_{base\ level}$) show that extra contribution of I_{cp} traps decrease with an increase in $t_{falling\ time}$. By fitting discharge formula for different $t_{falling\ time}$, the results show that electrons trapped in high-k bulk shallow traps first discharge to the channel and then to source and drain during $t_{falling\ time}$. This current cannot be measured by the charge pumping technique. Subsequent measurements of N_T by charge pumping technique at $t_{base\ level}$ reveal a remainder of electrons trapped in high-k bulk shallow traps. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4828719]

I. INTRODUCTION

As metal-oxide semiconductor field-effect transistors (MOSFETs) continue to shrink, the scaling of SiO₂ gate dielectrics is reaching its critical limit of only a few atomic layers thick. This scale causes a rise in gate current, degradation in performance, and an increase in power dissipation. Many years of research and development has shown that one valid way to solve these problems is by replacing conventional SiO₂ gate dielectric with high-k dielectric, especially with HfO₂ gate dielectric. HfO₂ gate dielectrics have been implemented at the 32 nm technology node and smaller, and Intel has been using high-k/metal gate since their 45 nm node. Furthermore, high-k gate dielectric can be integrated with strained-silicon, 1,2 silicon on insulator (SOI), 3-5 and architectures to improve device characteristics. High-k dielectric can also be combined with thin-film transistor devices⁶⁻¹⁰ and memory devices. 11-13 HfO₂ dielectrics have been heavily studied in recent years to replace SiO2-based dielectrics. 14,15 However, with the introduction of HfO₂ dielectrics, many measurement techniques must be refined, especially charge pumping techniques. For instance, in conventional SiO2-based dielectrics, with a decrease in frequency, I_{cp} decreases since carriers have enough time to

II. EXPERIMENTAL PROCEDURES

The HfO₂/metal gate n-MOSFETs used in this study were fabricated with a gate first process flow. First, a high quality 1 nm or 3 nm thick thermal oxide was grown as an interfacial layer. Second, 3 nm of HfO₂ dielectrics were sequentially deposited by atomic layer deposition. Third, 10 nm-thick TiN metal gate with varying N concentrations were deposited by radio frequency physical vapor deposition because metal gates can eliminate gate depletion and resist remote phonon scattering. ^{17,18} Next, poly-Si was deposited as a low resistance gate electrode. Finally, the dopant activation was performed at 1025 °C. The n-MOSFETs were measured by the charge pumping technique with different duty

³Advanced Optoelectronics Technology Center, National Cheng Kung University, Tainan, Taiwan

⁴Department of Embedded System Engineering, Peking University, Beijing, P.R.China

⁵Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan

⁶Device Department, United Microelectronics Corporation, Tainan Science Park, Taiwan

discharge from interface shallow traps. Conversely, in Hf-based dielectrics a decrease in frequency leads to an increase in I_{cp} since carriers have enough time to tunnel into high-k bulk traps. ¹⁶ Charge pumping techniques play an important role in inspection of defects. This study mainly focuses on high-k bulk shallow traps measured by the charge pumping technique at different falling and base level times for HfO_2 dielectric n-MOSFETs. To further investigate the behavior of these additional traps contributing to charge pumping current, devices with different interlayer thicknesses and different N concentrations in the Ti_xN_{1-x} metal gate are compared.

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw

ratios at different temperatures. A pulse train with low-voltage of $-0.6 \,\mathrm{V}$, high-voltage from $0 \,\mathrm{V}$ to $1.8 \,\mathrm{V}$, frequency of 200 kHz, and $t_{rising time} = t_{falling time} = 100 \text{ ns}$ was applied on the gate terminal. Ig-Vg transfer curves were measured with the source, drain, and body terminals all grounded, with V_g ranging from 0 V to 1.8 V. Then through body floating (BF), source/drain floating (SDF), and source/drain/body all grounded (SDB) process, the current path and carrier polarity were confirmed. Next, the I_g-V_g curve was fitted by Frenkel-Poole current and tunneling current. Then devices of different interlayer thicknesses and different Ti_xN_{1-x} metal gate N concentrations were measured by charge pumping technique at 60% and 98% duty ratios. For devices with different interlayer thicknesses, a pulse train with low-voltage of $-0.8 \,\mathrm{V}$, high-voltage from $0 \,\mathrm{V}$ to $1.8 \,\mathrm{V}$, frequency of 200 kHz, and $t_{rising time} = t_{falling time} = 100 \text{ ns}$ was applied on the gate terminal. For devices with different N concentrations of Ti_xN_{1-x} , a pulse train with low-voltage of $-0.8 \,\mathrm{V}$, high-voltage from $0 \,\mathrm{V}$ to $1.8 \,\mathrm{V}$, frequency of 200 kHz, $t_{rising time} = 100 \text{ ns}$, and $t_{falling time} = 500 \text{ ns}$ was applied to the gate terminal. Evidence showed that extra contribution of I_{CD} traps are in high-k bulk. Finally, to study the influence of falling time on high-k bulk traps measured by charge pumping technique, the other n-MOSFETs were measured by the charge pumping technique with different t_{falling time} and different t_{base level}. A pulse train with low-voltage of $-0.8 \,\mathrm{V}$, high-voltage from $0 \,\mathrm{V}$ to $1.71 \,\mathrm{V}$, t_{ris} $_{ing time}$ of 100 ns, $t_{high level}$ of 2.5 μ s, $t_{base level}$ from 0 s to 3 μ s, and $t_{falling time}$ from 20 ns to 5 μ s was applied on the gate terminal. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station.

III. RESULTS AND DISCUSSION

Figure 1 shows the N_T - $V_{high\ level}$ characteristic curves at different duty ratios. N_T is the number of traps ($N_T = I_{cp}/(qAf)$) and duty ratio = $((t_{rising\ time} + t_{high\ level})/t_{cycle})$. Clearly, N_T - $V_{high\ level}$ characteristic curves remain unchanged with an increase in duty ratio when $V_{high\ level} < 1.2\ V$. This implies that

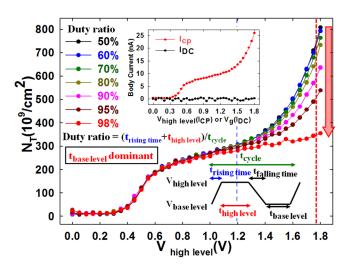


FIG. 1. N_T - $V_{high\ level}$ characteristic curves at different duty ratios by charge pumping measurement. Inset shows I_{cp} - $V_{high\ level}$ and I_{DC} - V_g curve with source and drain all grounded.

interface traps detected by the charge pumping technique are not dependent on t_{base level}. This is because the time for electrons in the interface traps to recombine with holes is very short since hole density is very large in the accumulation area $(\tau = 1/p_s \sigma V_{th})$. Hence, the numbers of interface traps measured by Icp are not sensitive to duty ratio. On the contrary, N_T decreases with a rise in duty ratio when $V_{high level} > 1.2 \text{ V}$. Furthermore, N_T measures only interface traps with a duty ratio value of 98% ($t_{base level} = 0 s$). In other words, extra contribution of I_{cp} traps almost disappears. The detrapping time $(t_{base\,level})$ of electron dominates the value of N_T such that N_T becomes smaller with a decrease in detrapping time. This demonstrates that electrons need time to discharge. Thus, it is necessary to know the relationship between N_T and the detrapping time ($t_{base\ level}$) for $V_{high\ level} > 1.2 \text{ V}$. The inset of Fig. 1 shows body current- $V_{high\ level}$ (I_{cp}) and body current- V_{g} (I_{DC}) curves with source and drain all grounded. I_{cp} and I_{DC} body currents are measured when AC and DC gate voltage are applied. It can be observed that I_{DC} is much smaller than I_{cp} . In addition, N_{T} is dependent on the detrapping time. Hence, these results mean that N_T measured by the charge pumping technique is not caused by gate leakage current, but rather high-k bulk traps that have been detected, as shown in the energy band diagram of Fig. 3. Figure 2 shows the N_T-V_{high level} characteristic curves at different $t_{\text{base level}}$. A pulse train with low-voltage of $-0.8 \, \text{V}$, high-voltage from 0 V to 1.7 V, $t_{high level}$ of 2.5 μ s, $t_{rising time}$ = $t_{\text{falling time}}$ = 100 ns, and $t_{\text{base level}}$ from 0 s to 3 μ s was applied on the gate terminal. Obviously, N_T measured at the body terminal by charge pumping measurement is similar to that when measured at source/drain terminal when $V_{high level} < 1 \text{ V}$ since this current is generated by recombination of electrons and holes in the interface traps. When $V_{high level} > 1 \text{ V}$, however, N_T measured at the body terminal is much smaller than when measured at source/drain terminal. In addition, N_T measured at source/drain terminal is independent of t_{base level} because this current is gate leakage current from gate to source/drain whereas N_T measured at the body terminal is dependent on $t_{base\ level}$. Thus, Figure 2 confirms that N_T measured through the body terminal is not an artifact related to gate leakage.

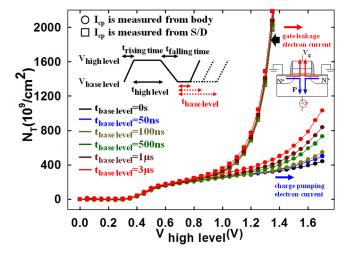


FIG. 2. N_T - $V_{high\ level}$ characteristic curves at different $t_{base\ level}$. A pulse train with low-voltage of $-0.8\ V$, high-voltage from $0\ V$ to $1.7\ V$, $t_{high\ level}$ of $2.5\ \mu s$, $t_{rising\ time} = t_{falling\ time} = 100\ ns$, $t_{base\ level}$ from $0\ s$ to $3\ \mu s$ was applied on the gate terminal.

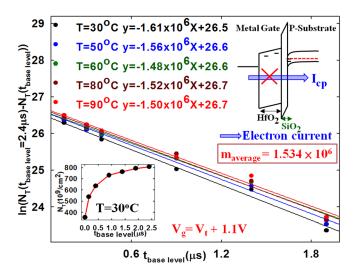


FIG. 3. $ln(N_T (t_{base\ level} = 2.4\ \mu s) - N_T (t_{base\ level}) - t_{base\ level}$ curves at different temperatures at $V_{high\ level} = V_t + 1.1\ V$. Inset shows $N_T - t_{base\ level}$ curve at 30 °C at $V_{high\ level} = V_t (0.67\ V) + 1.1\ V$. The energy band diagram shows I_{cp} is not gate leakage current.

Next, in order to characterize extra contribution of I_{cp} traps at high voltage, useful information can be extracted by fitting the curves. The lower left inset of Figure 3 shows N_T -t_{base level} curve at 30 °C, for $V_{high level} = V_t$ (0.67 V) + 1.1 V, as shown by the dashed red line in Fig. 1. Since N_T can also represent the numbers of electrons discharged from high-k bulk traps, N_T ($t_{base level} = 2.4 \mu s$)– N_T ($t_{base level}$) is the number of electrons still charged in the high-k bulk traps at t_{base level}, an important parameter. Figure 3 shows ln $(N_T (t_{base level} = 2.4 \mu s) - N_T (t_{base level})) - t_{base level}$ curves fitted by the discharge equation from the inset of Figure 3, where t_{base level} is the time for electrons to discharge from traps. Clearly, fitting these curves can be accomplished with straight lines even for different temperatures. In addition, slopes are also similar at these temperatures. The discharge equation can be described by 19

$$\begin{split} dQ(t)/dt &= -\Delta Q(t)/\tau_p = -e_p \Delta Q(t), \\ \Delta Q(t) &= \Delta Q(0) \exp(-e_p t), \end{split} \tag{1}$$

where e_p is the escape probability and τ_p is the average escape time. Thus, slope is indicated by e_p or $1/\tau_p$ with e_p not dependent on temperature. Hence, e_p may be the tunneling probability in large-area device. The average value of the slope at different temperatures ($m_{average}$) is 1.53×10^6 , and $\tau_{p,average}$ is $6.52 \times 10^{-7} (s)$. Now the value of tunneling distance can be determined by using $\tau_{p,average}$ and can verify that the traps are actually in the high-k bulk. The relationship between tunneling time and distance can be approximated by 21,22

$$t = \tau_0 \exp(\alpha_e x), \alpha_e = 2(2m_e q \phi_0/\hbar^2)^{0.5},$$
 (2)

where τ_0 is an electron tunneling characteristic time, m_e is electron effective mass for SiO_2 , and $q\varphi_0$ is the effective tunneling barrier height. However, because electrons are tunneling through two layers, SiO_2 and HfO_2 , this equation can be described by

$$t = \tau_0 \exp \left(\alpha_{e,SiO2} d_{SiO2} + \alpha_{e,HfO2} d_{HfO2,trap} \right), \tag{3}$$

where $\alpha_{e,SiO2} = 2(2m_{e,SiO2}q\varphi_{0,SiO2}/\hbar^2)^{0.5};$ $\alpha_{e,HfO2} = 2(2m_{e,HfO2}q\varphi_{0,HfO2}/\hbar^2)^{0.5};$ d_{SiO2} is the thickness of SiO₂; $d_{HfO2,trap}$ is the distance from traps to interlayer between SiO₂ and HfO₂; $m_{e,SiO2}$ and $m_{e,HfO2}$ are electron effective mass in SiO₂ and HfO₂, respectively; and $q\varphi_{0,SiO2}$ and $q\varphi_{0,HfO2}$ are effective tunneling barrier heights in SiO₂ and HfO₂, respectively. τ_0 , $m_{e,SiO2}$ and $m_{e,HfO2}$ can be obtained from literature. ^{21,23,24} Thus, only one parameter $(\varphi_{0,HfO2})$ is unknown.

The inset in Figure 4(a) shows I_g-V_g characteristic curves with BF, SDF, and SDB for distinguishing gate current at 30 °C. Clearly, the I_g-V_g characteristic curve in BF is similar to that in SDB, and the Ig-Vg characteristic curve in SDF is much smaller than either. These results indicate that electrons transfer from source/drain to the gate, rather than holes transferring from gate to body. Section A of Fig. 4(a) indicates the tunneling current detailed in Fig. 4(b), from $V_g = 0.35 \text{ V}$ to $V_g = 0.75 \text{ V}$, while section B is Frenkel-Poole current, shown in detail in Fig. 4(c), from $V_g = 1.1 \text{ V}$ to $V_g = 1.8 \text{ V}$. $\varphi_B = 0.49 \text{ eV}$ can be obtained by fitting the Frenkel-Poole mechanism in the inset in Fig. 4(c). 25-27 When $V_{high\ level} < 1.2 \text{ V}$, N_T is interface traps (N_{it}) only. On the contrary, when $V_{high level} > 1.2 \text{ V}$, N_T is both high-k bulk shallow traps (N_{hkst}) and N_{it}. A comparison of Fig. 1 with Fig. 4(a) shows that N_T is only N_{it} when gate current is tunneling current and Frenkel-Poole current is very small. Conversely, N_T is both N_{it} and N_{hkst} when gate current is Frenkel-Poole current. This indicates that bulk traps charging electrons via the Frenkel-Poole mechanism and bulk traps discharging electrons at V_{base level} in charge pumping measurement may be the same. In order to confirm this theory, $\varphi_{\rm B} = \varphi_{0,\rm HfO2} = 0.49 \, \rm eV$ is substituted into formula (3), where $m_{e,SiO2}$ is 0.95 m_0 , $m_{e,HfO2}$ is 0.03 m_0 , $\tau_0 = 6.6 \times 10^{-14}$ (s), d_{SiO2} is 10 Å, and $\phi_{0,SiO2} = 1.6 \text{ eV} + \phi_{0,HfO2}$. Finally, it can be determined that d_{HfO2,trap} is 13 Å. This is a reasonable value. While V_g transits from V_{high level} to V_{base level}, electrons in the high-k bulk shallow traps near the gate and substrate discharge to the gate and source/drain, respectively. Hence, only traps in the middle of the high-k bulk shallow traps can be measured by the charge pumping technique. In addition, when I_{cp} is measured at a duty ratio of 98%, at $t_{base level} = 0$ (s), electrons in the middle of the high-k bulk shallow traps have no time to tunnel to the substrate in the accumulation area. Thus, only interface traps are measured by I_{cp} at a duty ratio value of 98%.

The Figure 5(a) shows the N_T -($V_{high\ level}$ - V_t) characteristic curves at 60% and 98% duty ratio for 10 Å and 30 Å thick interlayer devices, respectively. Obviously, when $V_{high\ level}$ - V_t > 0.45 V, the value of N_T at 60% duty ratio is larger than that at 98% duty ratio for 10 Å-thick interlayer devices. However, for the 30 Å-thick interlayer devices, the values of N_T at both 60% and 98% duty ratios are similar. From the previous result, N_T (duty ratio = 60%)- N_T (duty ratio = 98%) is the value of high-k bulk shallow traps. In other words, high-k bulk shallow traps measured in the 30 Å-thick interlayer devices are insignificance. In addition, the gate current in 10 Å-thick interlayer devices is much larger than in

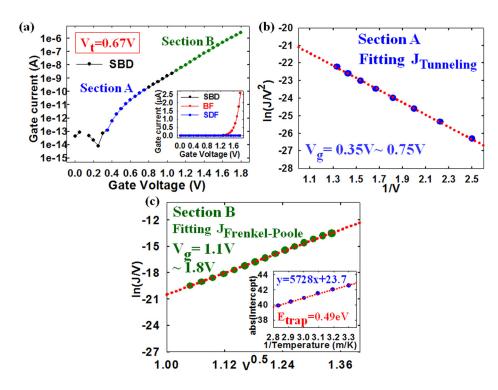


FIG. 4. (a) log(I_g)-V_g characteristic curves with SDB. Inset shows I_g-V_g characteristic curves with BF, SDF, and SDB. (b) Gate current in section A is fitted by tunneling model. (c) Gate current in section B is fitted by Frenkel-Poole model.

30 Å-thick interlayer devices, where practically none exists, as shown in Fig. 5(b). This phenomenon means that electrons in the channel are not able to tunnel through the interlayer to high-k bulk shallow traps due to its thickness, leading to high-k bulk shallow traps not charging electrons at accumulation and inversion areas in the charge pumping measurement. Hence, high-k bulk traps cannot be measured for 30 Å-interlayer devices when $V_{high\ level}$ - V_t > 0.45 V. Figure 5(c) shows the N_{T} -($V_{high\ level}$ - V_t) characteristic curves at 60% and 98% duty ratios for different of Ti_xN_{1-x} metal gate N concentrations. Obviously, with an increase in N concentration, two things occur, i.e., interface traps increase (as

indicated by the large blue arrow), and the value of N_T (duty ratio = 60%)– N_T (duty ratio = 98%) becomes smaller when $V_{high\ level}$ - V_t >0.45 V (as indicated by the blue, green, and red arrows). A previous paper shows that nitridation processes cause N to diffuse to the interlayer and Si substation interface, causing to a rise in interface traps, a reduction in mobility and an increase in Negative-bias temperature instability (NBTI). Thus, interface traps increase due to N diffusion to the interlayer. Other previous literature has shown that N can passivate high-k bulk shallow traps, 29 leading to a rise in effective barrier height in the Frenkel-Poole mechanism and a decrease in gate current. Gate current indeed reduces with an increase in

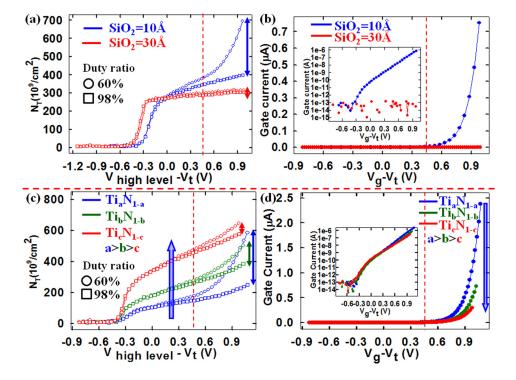


FIG. 5. (a) $N_{T^-}(V_{high\ level^-}V_t)$ characteristic curves with 60% and 98% duty ratio for 10 Å and 30 Å interlayer devices. (b) $I_{g^-}(V_{g^-}V_t)$ in 10 Å and 30 Å interlayer devices. Inset shows log (I_g) - $(V_g$ - $V_t)$ in 10 Å and 30 Å interlayer devices (c) $N_{T^-}(V_{high\ level^-}V_t)$ characteristic curves at 60% and 98% duty ratio in different N concentrations for Ti_xN_{1-x} metal gates. (d) I_g - $(V_g$ - $V_t)$ for different N concentration Ti_xN_{1-x} metal gate devices. Inset shows log (I_g) - $(V_g$ - $V_t)$ for different N concentration Ti_xN_{1-x} metal gate devices.

N concentration of the Ti_xN_{1-x} metal gate, as shown in Fig. 5(d). Therefore, high-k bulk shallow traps are passivated by N, causing the high-k bulk traps measured by charge pumping measurement to become smaller. These above results show that extra contribution of I_{cp} traps measured by charge pumping technique are actually high-k bulk shallow traps.

Next, the influence of falling time on high-k bulk traps measured by I_{cp} is discussed. Figure 6(a) shows the N_T - V_{high} level characteristic curves for different t_{falling time} and t_{base level}. N_T is the number of traps. Obviously, three main phenomena can be observed. First, with an increase in falling time, N_T decreases when V _{high level} < 1.2 V (as indicated by the large blue arrow). In this condition, N_T includes both N_{it} and N_{cp,gc} caused from the "geometrical component" of I_{cp.} With an increase in t_{falling time}, those channel electrons have enough time to diffuse back to source and drain (S/D) rather than drift to the body in the accumulation area, leading to a decrease in N_T. Second, with fixed t_{falling time} and an increase in $t_{base\ level}$, N_T increases when $V_{high\ level} > 1.2\,V$ (as indicated by the large red arrow). This is because electrons trapped in high-k bulk shallow traps need time to tunnel to the body in the accumulation area from the previous result. Third, with fixed t_{base level} and an increase in $t_{falling time}$, ΔN_T decreases when $V_{high level} > 1.2 V$ (as indicated by the red and green arrows). ΔN_T is high-k bulk traps $(N_T (t_{base level})-N_T (t_{base level} = 0 s))$. This phenomenon is further investigated in following discussion. The inset of Figure 6(b) shows I_g-V_g characteristic curves with BF, SDF, and SDB to distinguish gate current at 30 °C. Clearly, the I_g-V_g characteristic curve in BF is similar to that in SDB, and the Ig-Vg characteristic curve in SDF is much smaller than either one. These results indicate that electrons transfer from source/drain to the gate, rather than holes transferring from gate to body. Section A of Fig. 6(b) indicates the tunneling current detailed in Fig. 6(c), from $V_g = 0.62 \text{ V}$ to $V_g = 0.84 \text{ V}$, while section B

is Frenkel-Poole current, shown in detail in Fig. 6(d), from $V_g = 1.2\,\mathrm{V}$ to $V_g = 1.7\,\mathrm{V}$. $\phi_B = 0.49\,\mathrm{eV}$ can be obtained by fitting the Frenkel-Poole mechanism in the inset of Fig. 6(d). A comparison of Fig. 6(a) with Fig. 6(b) shows that N_T is N_{it} and $N_{cp,gc}$ when gate current is tunneling current, and Frenkel-Poole current is very small. Conversely, N_T is N_{it} , $N_{cp,gc}$, and N_{hkst} when gate current is Frenkel-Poole current. Hence, this indicates that bulk traps charging electrons from channel via the Frenkel-Poole mechanism and bulk traps discharging electrons to the body measured by I_{cp} are the same.

The left inset of Figure 7 shows the N_T-t_{base level} curve at 30 °C, for $V_{high\ level} = 1.71 \text{ V}$ and $t_{falling\ time} = 5 \times 10^{-8} \text{ s}$, as shown by the dashed green line in Fig. 6(a). Since N_T can also represent the numbers of electrons discharged from high-k bulk traps, N_T ($t_{base level} = 3 \mu s$)- N_T ($t_{base level}$) is the number of electrons still charged in the high-k bulk traps at $t_{base level}$. Figure 7 shows $ln (N_T (t_{base level} = 3 \mu s) - N_T$ (t_{base level}))-t_{base level} curves fitted from the left inset of Figure 7 by the discharge equation in formula (1). The parameter $t_{\text{base level}}$ is the time for electrons to discharge from traps. Clearly, fitting these curves can be accomplished with straight lines even for different t_{falling time}. In addition, slopes are also similar at these falling times and e_p is the tunneling probability in the previous result. From formula (3), the distance of high-k bulk shallow traps from the interlayer boundary (HfO₂/SiO₂) can be computed. It can be obtained that d_{HfO2,trap} is about 15 Å for different t_{falling time}, as shown in the right inset of Fig. 7. This is a reasonable value, and this result provides evidence that electrons are in fact in high-k bulk shallow traps. Furthermore, with an increase in t_{falling time}, the slopes remain the same while the intercepts decrease, indicating that the trap distances are the same. The intercept represents $\Delta Q(t_{base\ level} = 0 \text{ s})$, the number of electrons which are still charged in the high-k bulk traps when $t_{\text{base level}} = 0 \text{ s. Thus, with an increase in } t_{\text{falling time}}$, electrons

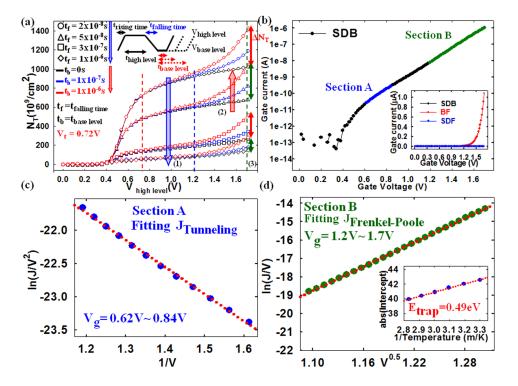


FIG. 6. (a) N_T-V_{high level} characteristic curves with different t_{falling time} and t_{base level} for charge pumping measurement. (b) log(I_g)-V_g characteristic curves with SDB. Inset shows I_g-V_g characteristic curves with BF, SDF, and SDB. (c) Gate current in section A is fitted by tunneling model. (d) Gate current in section B is fitted by Frenkel-Poole model.

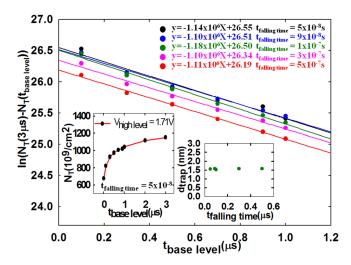


FIG. 7. ln (N_T ($t_{base\ level} = 3\ \mu s$)– N_T ($t_{base\ level}$))- $t_{base\ level}$ curves at different falling times at 30 °C with $V_{high\ level} = 1.71\ V$. Left inset shows N_T - $t_{base\ level}$ curve at 30 °C with $V_{high\ level} = 1.71\ V$. Right inset shows d_{trap} - $t_{falling\ time}$.

still charged in the high-k bulk traps decrease. The lost electrons should go to body terminals, but in fact do not. This is because electrons trapped in the high-k bulk traps discharge to the channel and then to S/D during $t_{\rm falling\ time}$. This current cannot be measured by the charge pumping technique. Thus, at $t_{\rm base\ level}$, N_{hkst} measured by I_{cp} represents leftover electrons in high-k bulk. This theory is similar to the mechanism of the "geometrical component" of I_{cp} $(N_{cp,gc})$.

Fig. 8(a) shows an N_T - $t_{base\ level}$ - $t_{falling\ time}$ characteristic surface diagram at $V_{high\ level} = 0.81\ V$ while Fig. 8(b) shows a ΔN_T - $t_{base\ level}$ - $t_{falling\ time}$ characteristic surface diagram at $V_{high\ level} = 1.71\ V$. N_T includes N_{it} and $N_{cp,gc}$. However, ΔN_T represents only N_{hkst} (N_T ($t_{base\ level}$)- N_T ($t_{base\ level}$)- N_T ($t_{base\ level}$). Obviously, with an increase in $t_{falling\ time}$, N_T and ΔN_T both decrease due to more channel electrons and electrons trapped in high-k bulk shallow traps flowing to the S/D rather than to the body. In addition, N_T is independent of $t_{base\ level}$ since channel electrons drifting to body do so quickly. On the contrary, with an increase in $t_{base\ level}$, ΔN_T increases since electrons trapped in high-k bulk shallow traps

need time to tunnel to the body in the accumulation area. In this way, $N_{cp,gc}$ and N_{hkst} can be easily distinguished.

Combining these results above, the energy band diagram of the model for charge pumping measurement can be determined, as shown in Fig. 9. When $V_{high level} < 1.2 \text{ V}$, gate current is tunneling-path dominated, leading to high-k bulk shallow traps not charging electrons. Electrons are in interface traps and the channel, as shown in Fig. 9(a). Subsequently, electrons recombine with holes in the interface traps at V_{base level} or drift from the channel to the body, as shown in Fig. 9(b). Thus, I_{cp} detects N_{it} and $N_{cp,gc}$. On the contrary, when $V_{high\ level}\!>\!1.2\,V,$ the gate current is dominated by the Frenkel-Poole mechanism, causing high-k bulk shallow traps to charge electrons. Therefore, electrons are in interface traps, high-k bulk shallow traps, and the channel, as shown in Fig. 9(c). Subsequently, three currents exist at V_{base level} in Fig. 9(d). Electrons in the interface traps recombine with holes. Electrons from high-k bulk shallow traps flow to the body, as do electrons in the channel. Therefore, I_{cp} measures N_{it} , N_{hkst} , and N_{ch} . In addition, electrons trapped in high-k bulk shallow traps first discharge to S/D at $t_{falling\ time}.$ This current cannot be measured by $I_{cp}.$ Therefore, N_{hkst} (ΔN_T) measured by I_{cp} at $t_{base\ level}$ is the electrons remaining in the high-k bulk.

IV. CONCLUSION

In summary, N_T - V_{high} level characteristic curves are nearly the same in value for V_{high} level < 1.2 V with a rise in duty ratio. However, N_T decreases with an increase in duty ratio for V_{high} level > 1.2 V. This indicates that the electron detrapping time dominates the value of N_T . Comparison of I_{cp} and I_{DC} results show that extra contribution of I_{cp} traps is not gate leakage current. Next, from curve fitting, the values of e_p obtained by the slope of I_{cp} (I_{base} level I_{cp})- I_{base} level are found to be independent of temperature. Hence, electrons discharge from high-k bulk shallow traps via the tunneling mechanism. Then, the distance of traps can be acquired by the equation I_{cp} exp(I_{cp})- I_{cp} 0 with I_{cp} 1 with I_{cp} 2 value I_{cp} 3 and I_{cp} 4 value I_{cp} 4 value I_{cp} 6 value

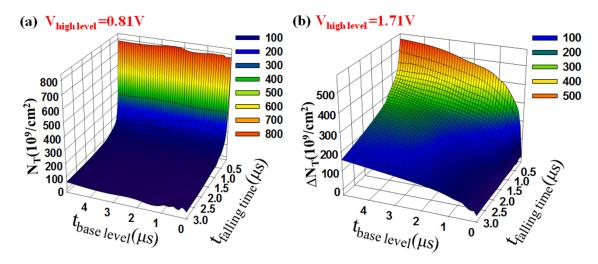


FIG. 8. (a) N_T - $t_{base\ level}$ - $t_{falling\ time}$ characteristic surface diagram at $V_{high\ level}$ = 0.81 V; (b) Δ N_T - $t_{base\ level}$ - $t_{falling\ time}$ characteristic surface diagram at $V_{high\ level}$ = 1.71 V.

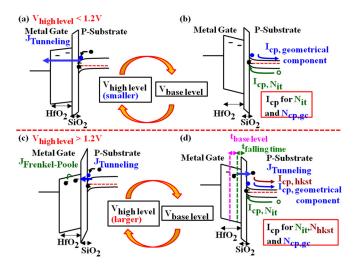


FIG. 9. The energy band diagram of high-k/metal gate MOSFETs with charge pumping measurement (a) for $V_{high\ level}$ and (b) for $V_{base\ level},$ when $V_{high\ level} < 1.2\ V$. The energy band diagram of high-k/metal gate MOSFETs with charge pumping measurement (c) for $V_{high\ level}$ and (d) for $V_{base\ level},$ while $V_{high\ level} > 1.2\ V$.

obtained from fitting the gate current with the Frenkel-Poole mechanism. From this, d_{HfO2,trap} can be calculated to be 13 Å, a reasonable value. This result is proof that extra contribution of I_{cp} traps is actually located in the high-k shallow bulk. In addition, comparison of different thickness interlayer devices and different N concentrations in the Ti_xN_{1-x} metal gate show that extra contribution of I_{cp} traps can be measured only when high-k bulk traps charge electrons in the gate current. $N_{cp,gc}$ and N_{hkst} (ΔN_T) decrease with an increase in t_{falling time} since more channel electrons and electrons trapped in high-k bulk shallow traps flow to the S/D rather than to the body. Those currents cannot be measured by I_{cp} . Furthermore, through fitting ln $(N_T (t_{base level}))$ $=3 \mu s$)-N_T (t_{base level}))-t_{base level} for different falling times and computing the trap distance by the equation $t = \tau_0$ ex $(\alpha_{e,SiO2}d_{SiO2} + \alpha_{e,HfO2}d_{HfO2,trap})$, the results show that d_{HfO2,trap} is about 15 A for different falling times, which means that the trap distances are the same. In addition, the intercept decreases with an increase in t_{falling time}. This indicates that electrons still charged in the high-k bulk traps decrease when $t_{\text{base level}} = 0 \text{ s}$ since electrons trapped in high-k bulk shallow traps discharge to S/D during t_{falling time}. This current cannot be measured by I_{cp}. This study shows that the longer the $t_{falling\ time}$, the less $N_{cp,gc}$ and N_{hkst} that are observed. When $t_{base\ level} = 0 s$, N_{hkst} disappears. Thus, only N_{it} is obtained for a more correct value.

ACKNOWLEDGMENTS

Part of this work was performed at United Microelectronics Corporation, at National Science Council Core Facilities Laboratory for Nano-Science and Nano-Technology in Kaohsiung-Pingtung area, NSYSU Center for Nanoscience and Nanotechnology. The work was supported by the National Science Council of the Republic of China under Contract No. NSC-102-2120-M-110-001.

- ¹Y. J. Kuo, T. C. Chang, P. H. Yeh, S. C. Chen, C. H. Dai, C. H. Chao, T. F. Young, O. Cheng, and C. T. Huang, Thin Solid Films **517**, 1715 (2009).
- ²Y. J. Kuo, T. C. Chang, C. H. Dai, S. C. Chen, J. Lu, S. H. Ho, C. H. Chao, T. F. Young, O. Cheng, and C. T. Huang, Electrochem. Solid-State Lett. 12. H32 (2009).
- ³C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. T. Tsai, W. H. Lo, S. H. Ho, G. Xia, O. Cheng *et al.*, Surf. Coat. Technol. 205, 1470–1474 (2010).
- ⁴C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, F. Y. Jian, W. H. Lo, S. H. Ho, C. E. Chen, W. L. Chung, J. M. Shih *et al.*, IEEE Electron Device Lett. **32**(7) 847–849 (2011).
- ⁵W. H. Lo, T. C. Chang, C. H. Dai, W. L. Chung, C. E. Chen, S. H. Ho, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **33**(3), 303–305 (2012)
- ⁶L. Y. Su, H. K. Lin, C. C. Hung, and J. J. Huang, IEEE J. Display Technol. **8**(12), 695–698 (2012).
- ⁷C. J. Chiu, S. P. Chang, and S. J. Chang, IEEE Electron Device Lett. **31**(11), 1245–1247 (2010).
- ⁸J. S. Lee, S. Chang, S. M. Koo, and S. Y. Lee, IEEE Electron Device Lett. **31**(3), 225–227 (2010).
- ⁹C. T. Tsai, T. C. Chang, S. C. Chen, I. Lo, S. W. Tsao, M. C. Hung, J. J. Chang, C. Y. Wu, and C. Y. Huang, Appl. Phys. Lett. **96**, 242105 (2010).
- ¹⁰T. C. Chen, T. C. Chang, C. T. Tsai, T. Y. Hsieh, S. C. Chen, C. S. Lin, M. C. Hung, C. H. Tu, J. J. Chang, and P. L. Chen, Appl. Phys. Lett. 97, 112104 (2010).
- ¹¹Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, IEEE Electron Device Lett. 32(4), 545–547 (2011).
- ¹²T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, Mater. Today **14**(12), 608 (2011).
- ¹³M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, Appl. Phys. Lett. **96**, 262110 (2010).
- ¹⁴C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. H. Ho, T. Y. Hsieh, W. H. Lo, C. E. Chen, J. M. Shih, W. L. Chung *et al.*, Appl. Phys. Lett. **99**, 012106 (2011).
- ¹⁵C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, W. H. Lo, S. H. Ho, C. E. Chen, J. M. Shih, H. M. Chen, B. S. Dai *et al.*, Appl. Phys. Lett. **98**, 092112 (2011).
- ¹⁶M. B. Zahid, R. Degraeve, M. Cho, L. Pantisano, D. R. Aguado, J. Van Houdt, G. Groeseneken, and M. Jurczak, Reliab. Phys. Symp. 21–25 (2009)
- ¹⁷W. J. Zhu and T. P. Ma, Electron Device Lett. **25**(2), 89–91 (2004).
- ¹⁸R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, Electron Devices Lett. 25(6), 408–410 (2004).
- ¹⁹H. Aozasa, I. Fujiwara, A. Nakamura, and Y. Komatsu, Jpn. J. Appl. Phys. 38, 1441–1447 (1999).
- ²⁰T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. J. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, IEEE Trans. Electron Devices 58(11), 3652–3666 (2011).
- ²¹I. Lundström and C. Svensson, J. Appl. Phys. **43**, 5045 (1972).
- ²²T. Wang, N. K. Zous, J. L. Lai, and C. Huang, IEEE Electron Device Lett. 19(11), 411–413 (1998).
- ²³M. J. Chen and C. Y. Hsu, IEEE Electron Device Lett. 33(4), 468–470 (2012).
- ²⁴C. Y. Hsu, H. G. Chang, and M. J. Chen, IEEE Trans. Electron Devices 58(4), 953–959 (2011).
- ²⁵C. C. Yeh, T. P. Ma, N. Ramaswamy, N. Rocklein, D. Gealy, T. Graettinger, and K. Min, Appl. Phys. Lett. 91, 113521 (2007).
- ²⁶K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, Appl. Phys. Lett. 87, 183505 (2005).
- ²⁷S. H. Ho, T. C. Chang, C. W. Wu, W. H. Lo, C. E. Chen, J. Y. Tsai, H. P. Luo, T. Y. Tseng, O. Cheng, C. T. Huang, and S. M. Sze, Appl. Phys. Lett. **101**, 052105 (2012).
- ²⁸X. Garros, M. Cassé, G. Reimbold, F. Martin, C. Leroux, A. Fanton, O. Renault, V. Cosnier, and F. Boulanger, in 2008 Symposium on VLSI Technology Digest of Technical Papers (2008), pp. 68–69.
- ²⁹W. C. Wu, T. S. Chao, T. H. Chiu, J. C. Wang, C. S. Lai, M. W. Ma, and W. C. Lo, IEEE Electron Device Lett. 29(12), 1340–1343 (2008).
- ³⁰G. Groesennken, H. E. Maes, N. Beltran, and R. F. Dekeersmancker, IEEE Trans. Electron Devices 31(1), 42–53 (1984).