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Fully room-temperature IGZO thin film transistors adopting stacked gate dielectrics on flexible polycarbonate substrate

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ABSTRACT

This study demonstrates the feasibility of producing an InGaZnO thin-film transistor (TFT) using a high-κ germanium oxide (GeO_2)/titanium oxide (TiO_2)/GeO_2 gate stack on a flexible polycarbonate substrate. The flexible TFT exhibited a small sub-threshold swing of 0.132 V/decade, an acceptable field effect mobility of 8 $cm^2/(V\,s)$, and a robust I_{on}/I_{off} ratio of 2.4×10^7. The improved device performance can be attributed to the combined effect of high-κ TiO_2 and the large band gap of GeO_2 that exhibits a tendency to remain in a Ge^{4+} oxidation state at room temperature.

1. Introduction

Compared with poly-Si thin-film transistors (TFTs), which possess a high thermal budget for channel activation, InGaZnO (IGZO) TFTs [1–7] have the advantage of high mobility in low-temperature processes, which provides improved uniformity of device characteristics, including threshold voltage, sub-threshold swing, and device mobility. Recently, amorphous IGZO, which does not exhibit any grain boundary issues, has been extensively studied because of its low-temperature fabrication process, high drive current, and low channel leakage on low-cost flexible substrates. However, these flexible IGZO TFTs require high operating and threshold voltages, which hinder the application of low-power flexible electronics. High-gate dielectrics can be used for lowering operational voltage, but low-temperature processed high-dielectrics cannot gain robust transistor characteristics on flexible substrates. To study these issues in a flexible TFT device, this paper presents a stacked gate dielectric consisting of high-κ titanium oxide (TiO_2) and a large band gap of germanium oxide (GeO_2) that was integrated with an amorphous IGZO TFT. The room-temperature (RT)-fabricated IGZO TFT using a high-κ $GeO_2/TiO_2/GeO_2$ gate dielectric exhibits a small sub-threshold swing of 0.132 V/decade, a low threshold voltage of 1.5 V, an acceptable field effect mobility of 8 $cm^2/(V\,s)$ and a robust on/off current ratio of 2.4×10^7 at an operating voltage of 5 V.

2. Experimental details

The bottom gate TFT was fabricated on a 300-nm-thick insulating SiO_2 layer thermally grown on a flexible polycarbonate (PC) substrate. A 35-nm-thick TaN gate electrode was deposited using dc sputtering. Subsequently, the 23-nm-thick GeO_2/58-nm-thick TiO_2/7-nm-thick GeO_2 (GTG) and 23-nm-thick GeO_2/58-nm-thick TiO_2 (GT) were deposited using electron beam evaporation at RT. This physical vapor deposition process is preferred in gate dielectric deposition because of the low thermal budget, especially on plastic substrates [8,9]. A 20-nm-thick IGZO active layer was then deposited using radio frequency sputtering from an IGZO target (99.99%) in a gas mixture of argon (70%) and oxygen (30%). Finally, 300-nm-thick Al source/drain electrodes were thermally evaporated and patterned, and the channel was 521×32 μm. The devices were characterized by using atomic force microscopy, transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS). The devices were characterized by current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements using an HP4156C semiconductor parameter analyzer and an HP4284A precision LCR meter, respectively.

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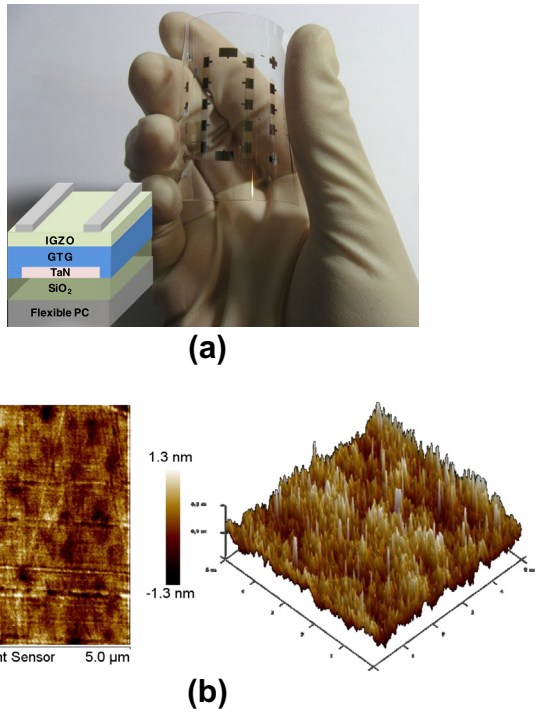

Fig. 1. (a) Photograph of IGZO TFT with $GeO_2/TiO_2/GeO_2$ dielectric on flexible PC and (b) AFM images of PC substrate. The inset of Fig. 1(a) is schematic structure of IGZO TFT using GTG gate dielectric.

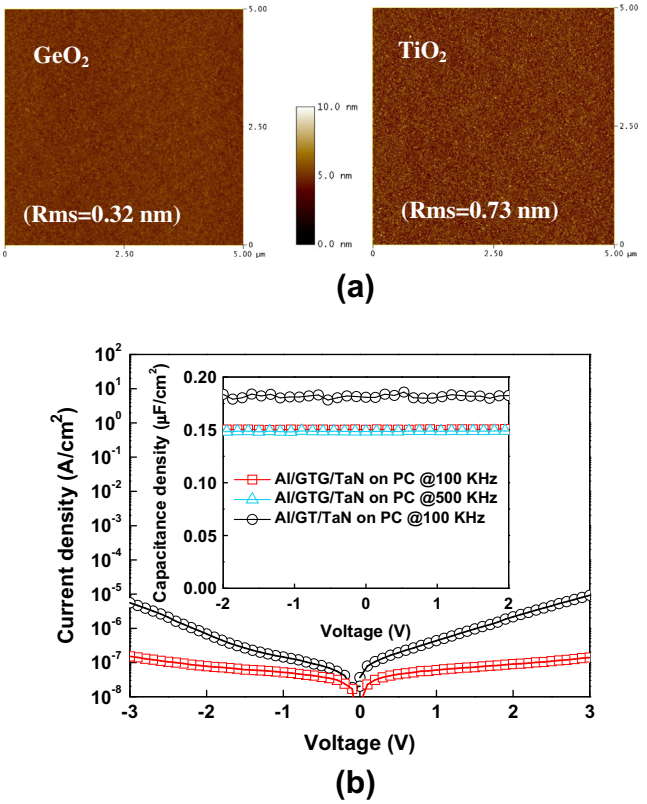

Fig. 2. (a) AFM images of TiO_2 and GeO_2 dielectrics and (b) *C–V* and *I–V* characteristics of Al/[GTG or GT]/TaN MIM capacitors on flexible PC substrate.

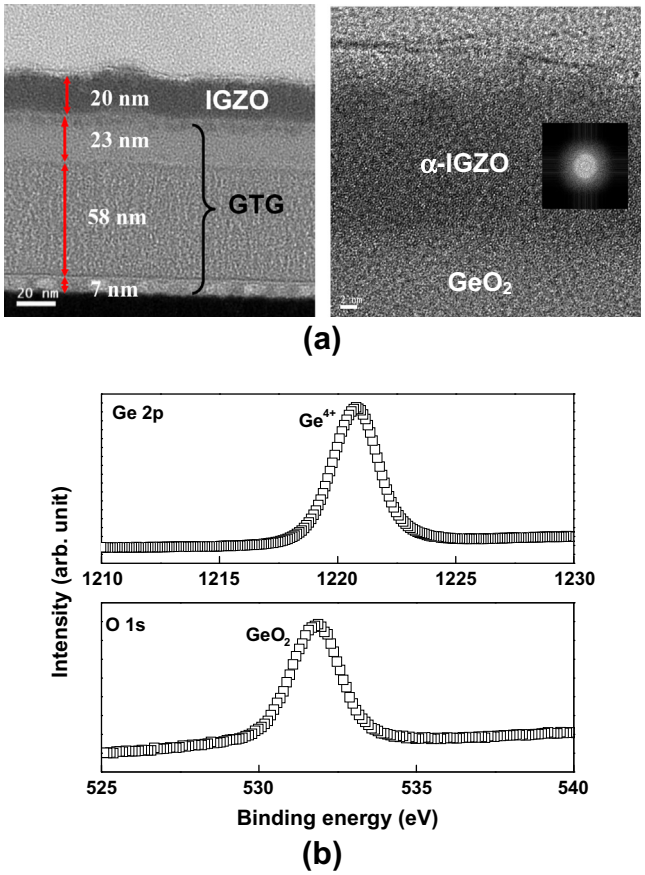

Fig. 3. (a) Cross-sectional view of high-resolution TEM images and (b) core-level XPS spectra of buffered GeO_2.

3. Results and discussion

Fig. 1(a) shows a photograph of the flexible IGZO/GTG TFT that was successfully fabricated on a transparent PC substrate. The inset is a schematic structure of the IGZO TFT. As shown in Fig. 1(b), the root-mean-square (*Rms*) surface roughness of PC substrate was only 0.34 nm, which was similar to the 0.1-nm *Rms* surface roughness of the Si substrate (not shown here). The flat substrate is necessary for reducing bottom gate leakage and improving the uniformity of characteristics in the flexible TFT device. Because amorphous TiO_2 possesses a high dielectric constant of >40 and low crystallization temperature of 300 °C [10,11], TiO_2 can achieve high gate capacitance at a low thermal budget. In addition, the native GeO_2 is easily formed on a Ge substrate at RT and the naturally formed oxide has a bonding preference of Ge^{4+} [12], which indicates the feasibility of fabricating an RT flexible TFT.

As shown in Fig. 2(a), the surface roughness (*Rms* = 0.32 nm) of the GeO_2 gate dielectric was considerably smaller than that (*Rms* = 0.73 nm) of the TiO_2 gate dielectric. Although high-κ TiO_2 can achieve a large capacitance density for high drive current, the rough surface morphology, narrow band gap of 3.05 eV, and small conduction band offset (ΔE_C – 0.05 eV) [13] are concerns when considering low gate leakage and off-state power. Therefore, the medium-κ GeO_2, which contains a large band gap of 5.6 eV [14] and is involved as a buffer layer, plays a crucial role in lowering gate leakage current because of the smooth surface and high potential barrier at the GeO_2/bottom TaN interface.

To evaluate film quality, stacked dielectrics consisting of TiO_2 and GeO_2 were fabricated and the structural properties in an RT process were investigated. The *C–V* and *I–V* characteristics of the

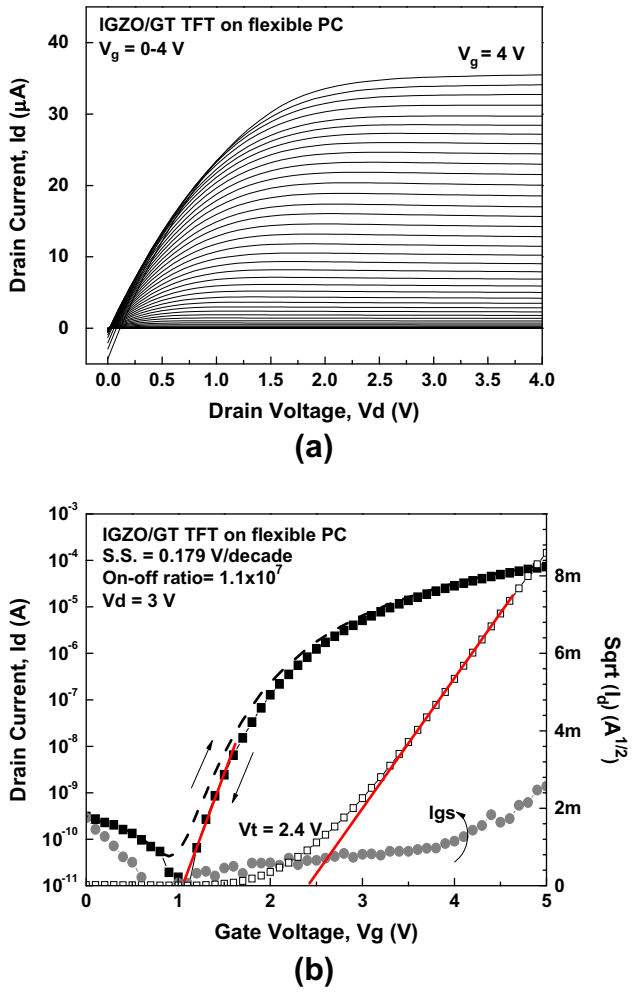

Fig. 4. (a) I_d–V_d and (b) I_d–V_g characteristics of IGZO/GT TFT device on flexible PC substrate.

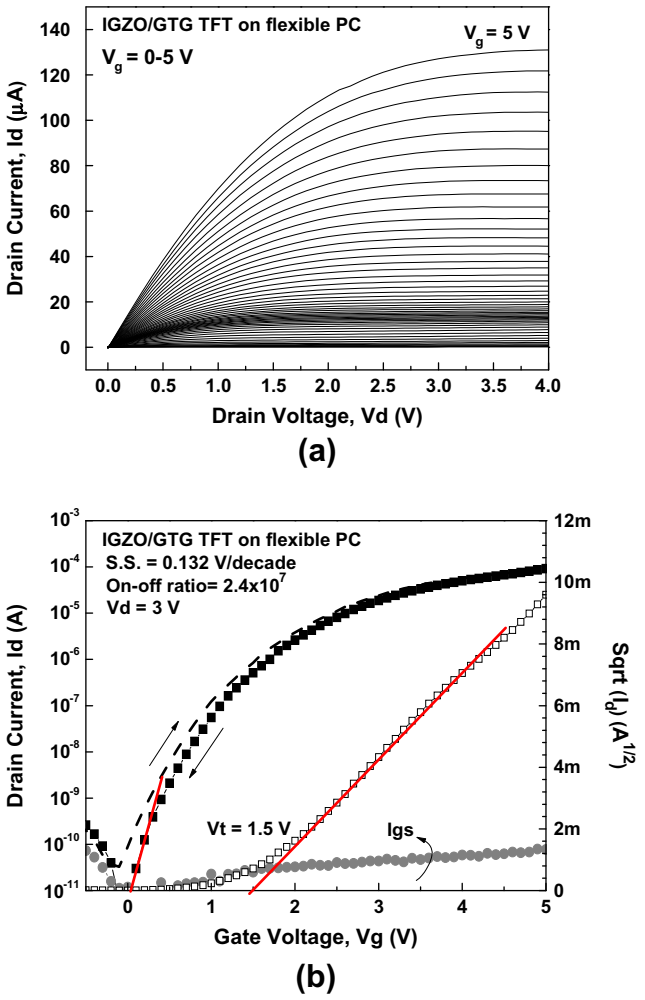

Fig. 5. (a) I_d–V_d and (b) I_d–V_g characteristics of IGZO/GTG TFT device on flexible PC substrate.

$Al/GeO_2/TiO_2/GeO_2/TaN$ and $Al/GeO_2/TiO_2/TaN$ metal-insulator-metal (MIM) capacitors on flexible PC substrates are shown in Fig. 2(b). A leakage current of 9.2×10^{-6} A/cm^2 at 3 V was obtained in the Al/GT/TaN MIM capacitor at a capacitance density of 0.18 F/cm^2 and exhibited severe voltage-dependent capacitance variation that was higher than the 1.4×10^{-7} A/cm^2 of the Al/GTG/TaN MIM capacitor. This is because the small ΔE_C and defective TiO_2-containing oxygen vacancies contributed excess bottom-injected carriers (1), which resulted in high capacitance variation and leakage current in the biasing fields.

$$V^{2+}_{\mathrm{Ti-Ox}} + 2e^- + \mathrm{Ti} - \mathrm{O}_x \rightarrow \mathrm{Ti} - \mathrm{O}^*_x \quad (1)$$

where $V^{2+}_{\mathrm{Ti-Ox}}$ is the oxygen vacancy in TiO_2 that is responsible for gate leakage current. Because of improved leakage immunity in the large GeO_2 band gap, the sandwich structure of GTG is beneficial for reducing the voltage/frequency dependence of gate capacitance, which also ensures that the transistor characteristics cannot be influenced by gate leakage when maintaining a high on-state current at a drive voltage.

A cross-sectional TEM image of the IGZO/GTG gate stack is shown in Fig. 3(a). The 20-nm-thick IGZO processes at RT had an amorphous phase, which was examined by using the fast Fourier transform (FFT) technique, in which the smooth bottom interface between the IGZO and GeO_2 buffer layer was clearly observed. In addition to lacking the formation of leakage current driven by the grain boundary, the amorphous IGZO exhibited fewer trap densities near or on the interface of the high-gate stack than did the crystallized IGZO. Additional material analysis on the gate dielectric was performed by using XPS (Fig. 3(b). The XPS spectrum showed that the Ge 2p peak centered at the binding energy of 1220.7 eV corresponded to the oxidation state of Ge^{4+}, which was assigned to the GeO_2 exhibiting a binding energy of 1220.6 eV [12,15]. The O-1s value in the XPS spectrum positioned at 531.8 eV may be attributed to Ge–O [12] or Ge–OH [16] bonds.

Table 1
Comparison of various flexible TFTs with different gate dielectrics fabricated at room temperature or <100 °C.

Gate dielectric	Operating voltage (V)	Threshold voltage (V)	Mobility [cm^2/(V s)]	*SS* (V/decade)	I_{on}/I_{off}	Temperature (°C)/substrate
GeO_2/TiO_2/GeO_2 (this work)	5	1.5	8	0.13	2.4×10^7	RT/PC
Y_2O_3 [6]	10	1.6	5.6	–	$\sim 10^3$	RT/PET
SiO_x [7]	10	1.9	1.2	0.65	1×10^4	100 °C/paper
SiN_x [18]	10	1.13	5.3	0.55	8×10^4	<100 °C/PI
SiN_x [19]	6	1.25	12.1	0.35	$>10^5$	90 °C/PET
Y_2O_3 [20]	6	1.4	3.9	0.2	1.7×10^6	RT/PET
BST-MgO [21]	15	4.2	1.04	1.85	7.48×10^5	RT/PET

Although GeO_2 can easily be influenced by moisture, the low gate leakage and strong transistor characteristics were acceptable in fully RT-TFT processes. Therefore, the GeO_2 and TiO_2 dielectrics deposited by high vacuum evaporation exhibit potential in the implementation of high-performance RT TFTs after moisture absorption is excluded.

To further study the issue of band-offset engineering, an IGZO TFT was fabricated using a bi-layer GeO_2/TiO_2 gate dielectric on a flexible PC. The I_d–V_d output and I_d–V_g transfer characteristics are shown in Fig. 4(a) and (b). In addition to a low operating voltage of 5 V, a small sub-threshold swing of 0.179 V/decade, I_{on}/I_{off} ratio of 1.1×10^7, threshold voltage of 2.4 V, and small hysteresis (approximately 0.1 V) were simultaneously achieved in the RT-TFT process. However, the flexible IGZO/GT TFT containing high gate leakage ((Fig. 2(a)) exhibited poor I_d–V_d characteristics (the inset of Fig. 4(a)) because the high gate-leakage-induced I_d lowered the magnitude limit of the drive voltage.

By contrast, a tri-layer GTG was also used as a gate dielectric in the flexible TFT. The I_d–V_d and I_d–V_g characteristics of the IGZO/GTG TFT in the flexible PC are shown in Fig. 5(a) and (b). Favorable transistor output characteristics were observed even when biasing at a low operational voltage below 5 V, which is beneficial in low-power flexible electronics applications. The I_d–V_g curve also showed that the low sub-threshold swing of 0.132 V/decade of the IGZO/GTG TFT was considerably improved compared with that (0.179 V/decade) of the IGZO/GT TFT. The sub-threshold swing (SS) was linked to the interface trap density (D_{it}) that was calculated based on the following equation [17]: $SS = kT/q \times \ln 10 \times [1+(C_b + C_{it})/C_{ox}]$, where C_{ox}, C_b, and C_{it} ($=qD_{it}$) are the gate capacitance, bulk capacitance, and interface charge capacitance, respectively. The variable C_{ox} was acquired from the Al/[GTG or GT]/TaN MIM capacitor of the flexible PC substrate. By neglecting C_b, the maximum D_{it} values for the IGZO/GTG and IGZO/GT TFTs were 1.1×10^{12} and 2.3×10^{12} cm^{-2} eV^{-1}, respectively, thereby indicating the improved interface quality in the IGZO channel, GTG dielectric, and TaN gate electrode. Compared with the IGZO/GT TFT device featuring an I_{on}/I_{off} of 1.1×10^7 and field effect mobility (μ_{FE}) of 5.3 cm^2/(V s), the IGZO/GTG TFT achieved a greater I_{on}/I_{off} of 2.4×10^7, a 2-fold higher reduction of trap density, and higher μ_{FE} at 8 cm^2/(V s). The reduction of threshold voltage or sub-threshold swing could be attributed to the improvement of the off-state current, which indicated a switching power decrease. Table 1 presents a comparison of the major characteristics of various flexible TFTs with different gate dielectrics that were fabricated at RT or <100 °C. The performance of this IGZO/GTG TFT is comparable with that of other devices, and provides the extra benefits of possessing the smallest sub-threshold swing, lowest operation voltage, and largest on–off ratio [6,7,18–21].

4. Conclusions

A $GeO_2/TiO_2/GeO_2$ dielectric was successfully integrated into IGZO TFTs by using a RT process on flexible PC substrates. The flexible IGZO/GTG TFT exhibited a low threshold voltage of 1.5 V, a small sub-threshold swing of 0.132 V/decade, and μ_{FE} of 8 cm^2/(V s) at a low operation voltage below 5 V, thereby indicating high potential in low-power portable electronics applications.

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