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Through-Silicon-Via Characterization and Modeling Using a Novel One-Port De-Embedding Technique

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SUMMARY In this paper, a novel and simple one-port de-embedding technique has been applied to through-silicon-via (TSV) characterization and modeling. This method utilized pad, via, and line structures to extract the equivalent circuit model of TSV. The main advantage of this de-embedding method is that it can reduce the chip area to fabricate test element groups (TEGs) for measurements while keeping S-parameter measurement accuracies. We also analyzed the electrical characteristics of substrate coupling and TSV equivalent impedance. Our results shows good agreements between measurement data and the equivalent circuit model up to 20 GHz.

key words: *3D IC, TSV, de-embedding, TEGs, microwave, RF modeling*

1. Introduction

To keep up with Moore's law, conventional CMOS scaling is facing increasing and risky capital investments. Therefore, industries have started to develop a relatively economical and simple solution that is through-silicon via (TSV) technology. 3D-IC packaging based on TSV is a promising technology that can overcome the challenges of Moore's law by directly using through-silicon substrates to connect the topside metal with the backside metal via through-wafer interconnects. The TSV technique has been utilized with CMOS sensors, microelectromechanical systems, and memory application. Furthermore, TSV has also been successfully implemented in 28 nm CMOS technology [1]. However, there are still many challenges for 3D-IC packages [2], difficulties related to mass production, and manufacturing reliability issues [3]. Therefore, the TSV silicon interposer (2.5D-IC), which is a low-cost, simple, and preliminary solution, has been developed and realized. This 2.5D-IC technology can integrate various function chips with different processes into stacked chip packages [4]. TSV takes advantage of vertical interconnects and die stacks to shorten the interconnect length. This efficient method can reduce signal loss and parasitic effects, and can increase the transmission speed to meet the increasing demands for smaller size, lower signal propagation delay, lower power consumption, and high frequency performance [5]. Consequently, analog and RF circuits are expected to adapt this technique in the near future. Therefore, it is necessary to accurately analyze and model the TSV RF behavior. Previous papers have focused on a TSV RF model over the past years. The inter-TSV coupling model was proposed in [6]. The TSV impedance also has been extracted in [7]. The RF analytical modeling of TSV and RF lines with different lengths on the back-side has also been demonstrated [8]. In this paper, we propose a novel and simple de-embedding technique to model the TSV behavior using one-port layout testkeys. In contrast to conventional two-port technique, this method can preclude the effects of direct coupling and insertion loss between two opposing ports. Therefore, we can improve the measurement accuracy to enhance the modeling accuracy. As shown in Fig. 1, these testkeys require at least two TSV (a) pad and (b) via structures with different pitch lengths to extract model parameters of substrate coupling effects. Here, the filled pillars of TSV via structures with copper are placed below a probing pad to mitigate the vertical substrate coupling. Similarly, we also need a couple of TSV (c) line structures with the same line width, but with varying line numbers.

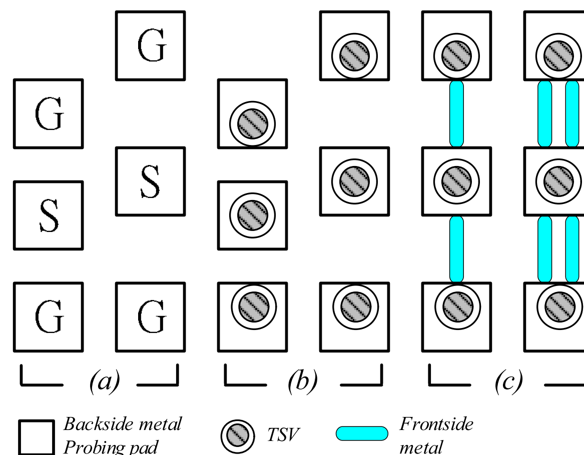

Fig. 1 Proposed TSV De-embedding testkeys include (a) pad, (b) via, (c) line.

2. Experiments

TSV testkeys were fabricated using the via-middle approach in a 1P7M 28 nm CMOS process with backside metal adhesion. An interface SiN layer was used to isolate the backside metal and substrate. We used Cascade Microtech's ground-

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signal-ground Infinity probes with 50-, 75-, and 100-μm pitch lengths to probe the contact pad on the backside metal. One-port S-parameter measurements were performed for the frequency range 100 MHz to 20 GHz using an HP8510C network analyzer, and we used the short-open-load calibration procedure with a ceramic impedance standard substrate.

3. Model Description

Figure 2 shows cross-sectional views of the proposed TSV de-embedding testkeys. Figure 2(a) illustrates the equivalent circuit model of TSV pad structures. where *Co* represents the insulator capacitance between the backside metal and the silicon substrate the via SiN layer. Here, the topmost layer is the backside metal used for probing. Because the coupling effect of the silicon substrate is frequency dependent [9], the *Rs* and *Cs*-*Rss* branches are connected in parallel in order to model this characteristic. Figure 2(b) shows the equivalent circuit model of a TSV via structure, accounting for the substrate coupling effect between the signal and ground pads. In this case, *Cox* depicts the insulating capacitance composed of circular silicon dioxide between the TSV and substrate. The TSV is encircled by this insulating dielectric layer to provide DC isolation between the TSV and silicon substrate. The dielectric layer also results in the substrate model of via structures being different from the pad structure; hence, we use the new elements, denoted as *Rsi*, *Csi*, and *Rssi*, to model the silicon substrate coupling. Figure 2(c) shows the equivalent circuit of the TSV line structure model. These TSV pillars are filled with copper metal, and its model is similar to a metal line. L_{TSV} represents the effective inductance, R_{TSV} specifies the effective resistance, and *Lp* and *Rp* are used to model the skin effect. In addition, L_{L} and R_{L} are used to model the equivalent impedance of the frontside metal lines.

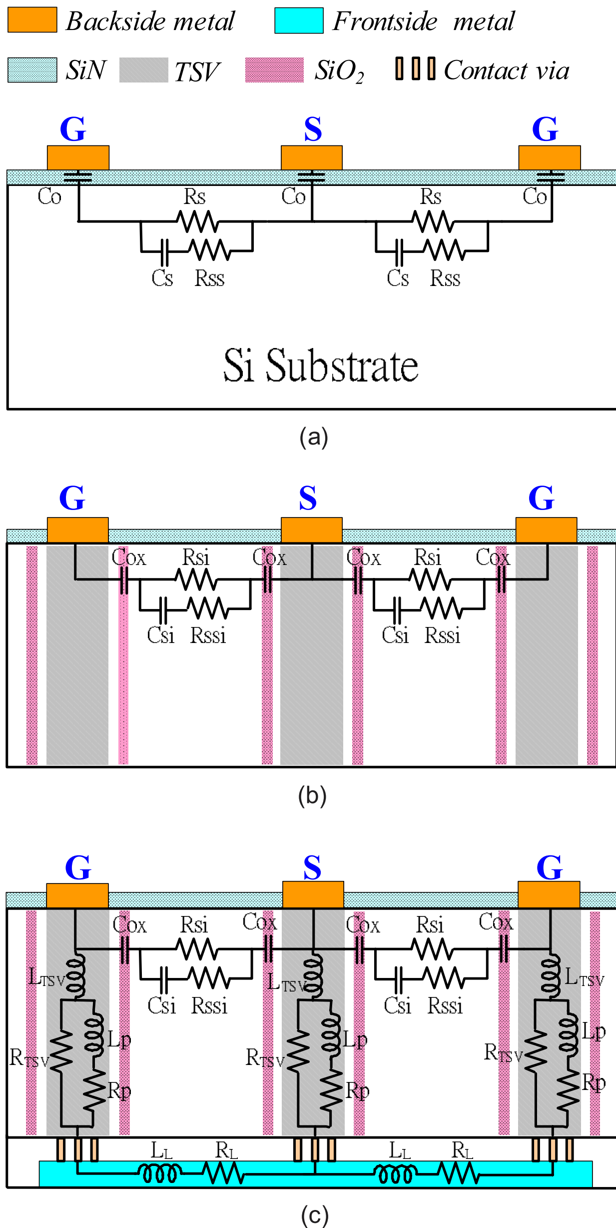

Fig. 2 Equivalent circuits for TSV structures (a) pad, (b) via, (c) line.

4. Model Extraction

We start to extract the TSV pad structures at first. Because the TSV pad structures are bilateral symmetrical, the electrical impedance of TSV pad structures, denoted Z_{pad}, can be written as

$$2Z_{pad} = \frac{2}{j\omega C_O} + Rs \,//\, \left(Rss + \frac{1}{j\omega C_s}\right) \tag{1}$$

Where ω represent the angular frequency and symbol // indicate a parallel connection. At low frequencies, the impedance of *Rs* is so small compared with *Rss*-*Cs* branch that it can be neglected. Therefore, we can also extract the initial value of *Rs* and *Co* as follows:

$$Rs = Re(2Z_{pad}) \tag{2}$$

$$Co = \frac{1}{-\omega Im(Z_{pad})} \tag{3}$$

At high frequencies where the current flows mostly through the branch of *Rss*-*Cs* relative to *Rs*, Therefore, we can calculate total capacitance in sereis at high frequencyies as follows:

$$\frac{2}{Co} + \frac{1}{Cs} = -\omega Im(2Z_{pad}) \tag{4}$$

Then, we can obtain the *Cs* by using the Eq. (4) and the extracted *Co* from Eq. (3). In addition, *Rss* is mainly used for fitting the slope of S_{11} from 5 GHz to 20 GHz. Figure 3 shows the $(-\omega \mathrm{Im}(2Z_{\mathrm{pad}}))^{-1}$ as function of frequency. The extraction results are listed in Table 1. As the pitch lengths increase, *Rss* and *Rs* are seen to increase linearly while *Cs* decreases inversely. In addition, *Co* is independent of the different pitch lengths. This means that the model of TSV via structures are scalable. Figure 4 compares the measured (symbols) and simulated (lines) reflection S_{11} of TSV

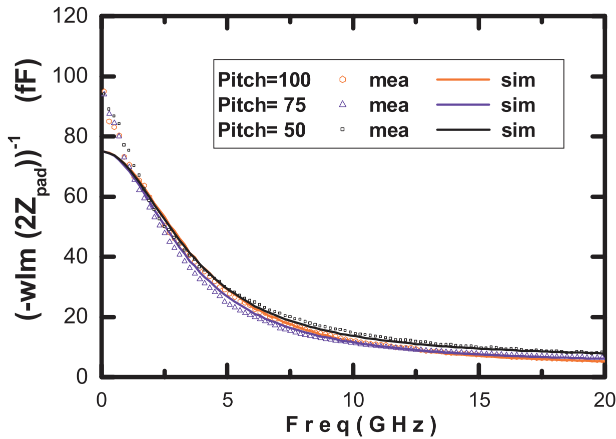

Fig. 3 Measured (symbols) and simulated (lines) $(-\omega\mathrm{Im}(2Z_{\mathrm{pad}}))^{-1}$ of TSV pad structures with 50-, 75-, and 100-μm pitch lengths.

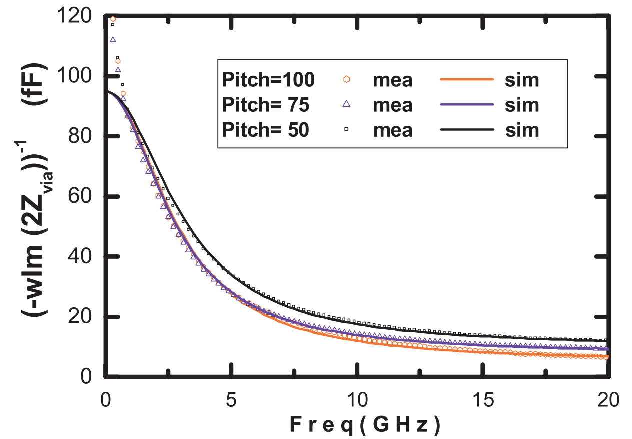

Fig. 5 Measured (symbols) and simulated (lines) $(-\omega\mathrm{Im}(2Z_{\mathrm{via}}))^{-1}$ of TSV via structures with 50-, 75-, and 100-μm pitch lengths.

Table 1 Electrical model parameters of TSV pad structures with various pitch lengths extracted by experiment.

Pitch (um)	*Co* (fF)	*Rs* (Ω)	*Cs* (fF)	*Rss* (Ω)
50	150	2000	6	34
75	150	2600	4	90
100	150	3000	2.5	180

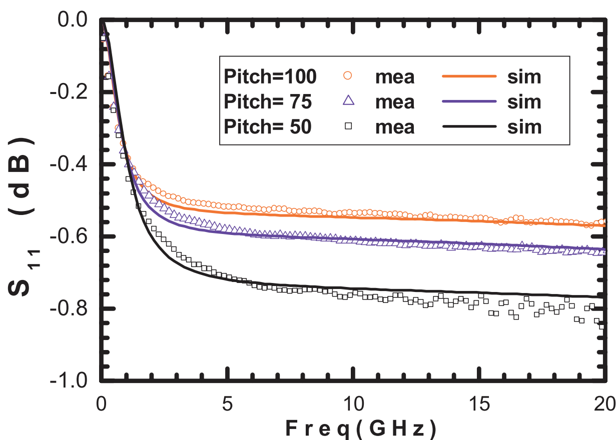

Fig. 4 Measured (symbols) and simulated (lines) reflection S_{11} of TSV pad structures with 50-, 75-, and 100-μm pitch lengths.

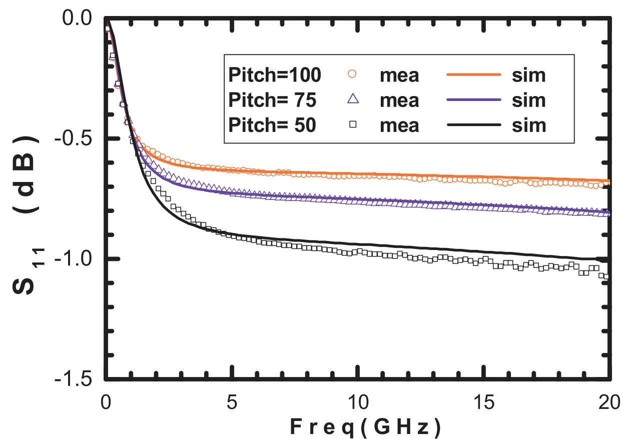

Fig. 6 Measured (symbols) and simulated (lines) reflection S_{11} of TSV via structures with 50-, 75-, and 100-μm pitch lengths.

Table 2 Electrical model parameters of TSV via structures with various pitch lengths extracted by experiment.

Pitch (um)	*Cox* (fF)	*Rsi* (Ω)	*Csi* (fF)	*Rssi* (Ω)
50	190	1520	10.5	40
75	190	2000	8	50
100	190	2450	5	60

pad structures to estimate for the impact of substrate noise coupling, which is an important issue in RF/Mixed-signal IC. The noise of digital circuits injected through the substrate will degrade the performances of sensitive RF circuits. The higher S_{11}, the less signals run through the substrate to ground pad, has better noise isolation. Therefore, this physical based, scalable TSV pad model can be used to predict the influence of substrate noise coupling with different pitch lengths and pad size for RF circuit designers.

Because the TSV pad and via structures are similar, we can extract the model parameters of TSV via structures as well as pad structures. Figure 5 and Fig. 6 show the $(-\omega\mathrm{Im}(2Z_{\mathrm{via}}))^{-1}$ and reflection S_{11} of TSV via structures as function of frequency. Where Z_{via} represents the electrical impedance of TSV via structures. The extraction results are listed in Table 2. Because TSV via structures have extra cu pillar, the effective substrate lengths are shorter than TSV pad structures. This explains why TSV pad structures have lower substrate resistances and higher substrate capatances.

To extract the model parameters, TSV line structures are de-embedded from the substrate coupling effect using

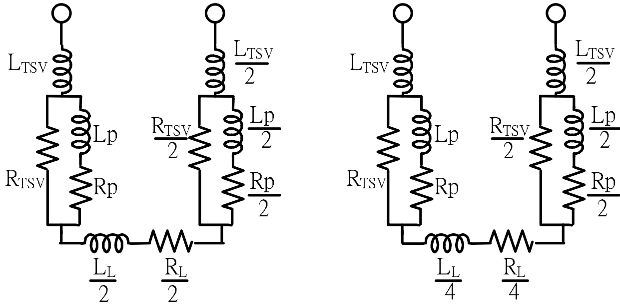

Fig. 7 Equivalent circuits for TSV line structures with single and double line numbers.

Y_{Line} - Y_{Via}. Here, Y_{Line} and Y_{Via} are the admittance matrices of the TSV line and via structures. Because the TSV line structures are symmetrical along a centrally vertical axis, the model after de-embedding can be simplified as in Fig. 7. The series impedance of TSV line structures with single and double line numbers, simply written as Z_1 and Z_2, can be calculated as shown below.

$$Z_1 = \frac{3}{2}\left[j\omega L_{TSV} + \frac{R_{TSV}(R_P + j\omega L_P)}{R_{TSV} + R_P + j\omega L_P}\right] + \frac{j\omega L_L}{2} + \frac{R_L}{2} \quad (5)$$

$$Z_2 = \frac{3}{2}\left[j\omega L_{TSV} + \frac{R_{TSV}(R_P + j\omega L_P)}{R_{TSV} + R_P + j\omega L_P}\right] + \frac{j\omega L_L}{4} + \frac{R_L}{4} \quad (6)$$

Thus,

$$2Z_2 - Z_1 = \frac{3}{2}\left[j\omega L_{TSV} + \frac{R_{TSV}(R_P + j\omega L_P)}{R_{TSV} + R_P + j\omega L_P}\right] \quad (7)$$

Therefore, the impedance of a single TSV pillar

$$Z_{TSV} = j\omega L_{TSV} + \frac{R_{TSV}(R_P + j\omega L_P)}{R_{TSV} + R_P + j\omega L_P} \quad (8)$$

can be expressed as

$$Z_{TSV} = \frac{2}{3}[2Z_2 - Z_1] \quad (9)$$

In the frequency range of roughly 5 GHz to 20 GHz, the electrical impedance of R_{TSV} is so small compared with *Rp*-*Lp* branch that it can be neglected, Eq. (8) can be rewritten as

$$Z_{TSV} = \frac{2}{3}[2Z_2 - Z_1] \approx j\omega L_{TSV} + R_{TSV} \quad (10)$$

We can extract L_{TSV} and R_{TSV} at high frequencies as follows:

$$R_{TSV} = Re(Z_{TSV}) \quad (11)$$

$$L_{TSV} = \frac{Im(Z_{TSV})}{\omega} \quad (12)$$

To prevent the contact resistance effect on parameter extraction, Cascade Microtech's Infinity probes that have low contact resistance (typically < 0.05 Ω) and automatic measurement technique [10] were employed in this study. The extraction results for the TSV line structures are summarized in Table 3. R_{TSV} and L_{TSV} are about 0.11 Ω and 30.7 pH, respectively. Figure 8 shows the measured and simulated $Re(Z_{TSV})$ and $Im(Z_{TSV})/\omega$ as a function of frequency. As was expected, $Re(Z_{TSV})$ and $Im(Z_{TSV})/\omega$ remain constant beyond 4 GHz. At low frequencies from 0.1 GHz to 4 GHz, the effective R_{TSV} increases and effective L_{TSV} decreases with increasing frequency are mainly due to skin effect. *Rp* and *Lp* have been used to successfully model the contributions of the skin effect. Furthermore, It's noted that the effective R_{TSV} starts decreasing with increasing frequency when the frequencies go beyond the bounds of applicability range of equivalent circuits. The limitations of TSV model range are caused by the effect of distributed R_{TSV}, L_{TSV}, *Cox* and *Cssi*.

Table 3 TSV electrical model of TSV line structures.

R_{TSV} (Ω)	L_{TSV} (pH)	R_P (Ω)	L_P (pH)	R_L (Ω)	L_L (pH)
0.11	30.7	0.26	48	0.15	16.2

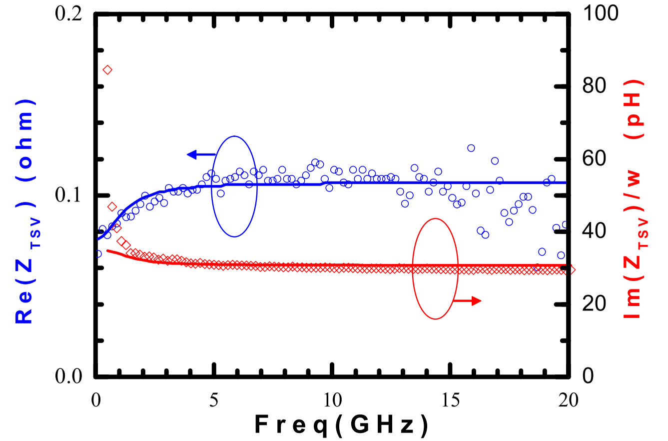

Fig. 8 Measured (symbols) and simulated (lines) $Re(Z_{TSV})$ and $Im(Z_{TSV})/\omega$ as functions of frequency.

5. Conclusions

This paper presents the one-port de-embedding technique for TSV characterization and modeling. We analyzed the coupling effects between TSVs and extracted the substrate coupling parameters using the TSV via structures with different pitch lengths. Then, the TSV line structures with single and double line numbers were used to extract the transfer impedance of TSV. The agreements between the measurement and simulation results show that this proposed approach is dependable and accurate up to 20 GHz.

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