Analysis of Surface State Effect on Gate Lag Phenomena in GaAs MESFET's

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Abstract—**A two-dimensional transient simulation of the gate lag phenomenon in GaAs MESFET's has been performed. Our results show that the charge exchanges in the population of the surface states at the ungated access region of FET's are responsible for this slow transient phenomenon. The measured "hole-trap-like" DLTS signal is directly related to the re-emission of the holes, trapped during the filling pulse. Higher gate pulse can cause more serious lag phenomenon due to larger modulation of surface charge density. Devices with shorter N^+-gate spacing and lower surface state densities are shown to have less gate lag effect.**

I. Introduction

IT is well known that in GaAs MESFET's, a current lag phenomenon often occurs when the FET is turned on by a sudden voltage pulse applied to the gate [1]–[3]. When the gate is forward pulsed from pinchoff, the drain current switches only partly on, and then gradually increases toward the steady state value. The time constant of the current lag ranges from 1 ns to several seconds, depending on pulse magnitude, device parameters (such as channel doping, gate recess depth and N^+-gate spacing), passivation conditions, and so on. The percentage of the partially "on" current to the steady-state "on" current for a typical MESFET is in the range of 30-80%. This phenomenon, the so-called "*gate lag effect*" is a detrimental parasitic effect, which can seriously limit the performance of GaAs-based devices and integrated circuits. For example, gate lag affects digital circuits such as inverter chains by causing pulse narrowing [1], [4]. As the pulse passes through the inverter chain, it gets narrower and narrower and finally disappears, thus causing the chain not to function correctly. Dumas *et al.* [3] observed the occurrence of the gate-lag phenomenon on power FET's during aging and recommended performing gate lag measurement during FETs' reliability investigations.

Several methods have been proposed to alleviate the gate lag effect. Yeats *et al.* [1] used tight gate structures in their MESFET's and a moderate to high doping near the edges of the gate and observed a reduced gate lag effect. A special pre-passivation cleaning procedure followed by a special dielectric passivation has also been suggested to reduce the gate lag effect, but no conclusive result has been obtained [1], [2].

Several causes for the gate lag phenomenon have been proposed, including the slow surface states induced by free ions in the dielectric passivation layer or deep traps in the disordered region close to the GaAs surface in the access region [2], and deep traps at the channel-substrate interface [5]. Ozeki *et al.* [6] measured the frequency dependence of the transconductance and confirmed that the surface states between the passivation film and the active layer had a strong influence on the performance of GaAs MESFET's. Other evidence supporting the role of surface states was reported by Blight *et al.* [7] using conductance deep level transient spectroscopy (DLTS) measurements. Blight *et al.* suggested that the main contribution to the "*hole-trap-like*" spectrum in the conductance DLTS is not due to bulk hole traps located at the active channel-substrate interface but from a surface origin. They believe that the gate lag phenomenon arises from charge exchanges in the population of surface states in the ungated access regions of the device, resulting in time-dependent modulation of the surface depletion layer in series with the gate depletion region.

Until now, all the reported works concerning this anomalous large-signal transient behavior have been based on experimental measurements [1], [2], [7]. There are still remaining questions needing to be explained and better understood. They include:

1) roles in the gate lag phenomenon played by the deep traps existing at the channel-substrate interface and those high-density surface states existing in the ungated access region;
2) anomalous "hole trap-like" conductance DLTS spectrum. Whether it is from the re-injection, after the pulse, of free electrons into surface states, or from the re-emission of holes trapped during the pulse;
3) dependence of negative surface charge density and the surface potential upon different gate voltages;
4) time-dependent modulation of depletion region width of ungated access regions between the ohmic contacts and the gate edge, i.e., time-dependent R_S and R_D, during the gate lag process.

In this paper, the results from a fully two-dimensional numerical simulation for the gate lag phenomenon in GaAs MESFET's are presented. The questions listed above are

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addressed. Devices with different surface state densities and N^+-gate spacing are simulated and compared.

II. Device Structures and Physical Models

A. Device Structures

The two GaAs MESFET structures used in the simulation are shown in Fig. 1(a) and 1(b). For both structures, the n-type channel beneath the gate is 0.2 μm thick and is uniformly doped with a concentration of 1×10^{17} cm^{-3}. The gate length is 0.5 μm and both the source-gate and the gate-drain spacing are 1.5 μm. While Fig. 1(a) represents a conventional MESFET, Fig. 1(b) represents a more advanced structure with N^+ access regions close to the gate. The doping concentration in the N^+ region is 5×10^{17} cm^{-3} and the spacing between the gate and the edge of the N^+ region is varied from 0.1, 0.2, 0.3, 0.4 or 0.5 μm. For the device shown in Fig. 1(a), the threshold voltage is about -2.5 V and for the devices with different N^+-gate spacing shown in Fig. 1(b), the threshold voltage is about or less than -2.5 V, depending on the spacing length. The threshold voltage for devices with shorter N^+-gate spacing is more negative due to the short channel effect [8].

The EL2 concentration N_{EL2} and the shallow-acceptor concentration N_A in the semi-insulating substrate beneath the channel layer are chosen to be 1×10^{16} and 1×10^{15} cm^{-3}, respectively. Both N_{EL2} and N_A assumed in this study are typical values found in normal undoped LEC substrates [9], [10]. The total depth simulated is 1.2 μm which is deep enough to encompass all physical phenomena.

B. Models

For the transient simulation, a two-dimensional, two-carrier device simulation program based on the drift-diffusion formulation was developed. The emission and capture of free carriers for deep traps (EL2) in the substrate followed the Shockley-Read-Hall model [11]. The energy difference between the conduction band edge and the EL2 level was assumed to be 0.69 eV at room temperature [12]. The electron and the hole capture cross sections were 3.5683×10^{-15} and 1×10^{-18} cm^2, respectively [13]. The work function difference of the gate metal-semiconductor contact is assumed to be 0.8 eV. Current transport across the Schottky-barrier junction is described by the thermionic emission-diffusion theory.

The surface model used in this study was based on Spicer's unified defect model [14]. Two surface deep states were assumed, i.e., a single donor-type trap, $E_{\mathrm{CT},D} = 0.925$ eV, below the conduction band edge and a single acceptor-type trap, $E_{\mathrm{TV},A} = 0.8$ eV, above the valence band edge [15]. The areal density of the surface atoms of [100] GaAs is of the order of 10^{15} cm^{-2}. For an n-type semiconductor with a doping concentration of $1 \times 10^{17} \sim 5 \times 10^{17}$ cm^{-3}, a surface state density of greater than 2×10^{12} cm^{-2} is required to pin the surface Fermi level at the position of the defect states [16]. In this study, different surface state densities varied from 2×10^{13} to 1×10^{14} cm^{-2}, uniformly distributed along the surface of the access region between the ohmic contacts and the gate contact, were assumed. At thermal equilibrium, the surface Fermi level in the ungated region is calculated to be pinned by the surface

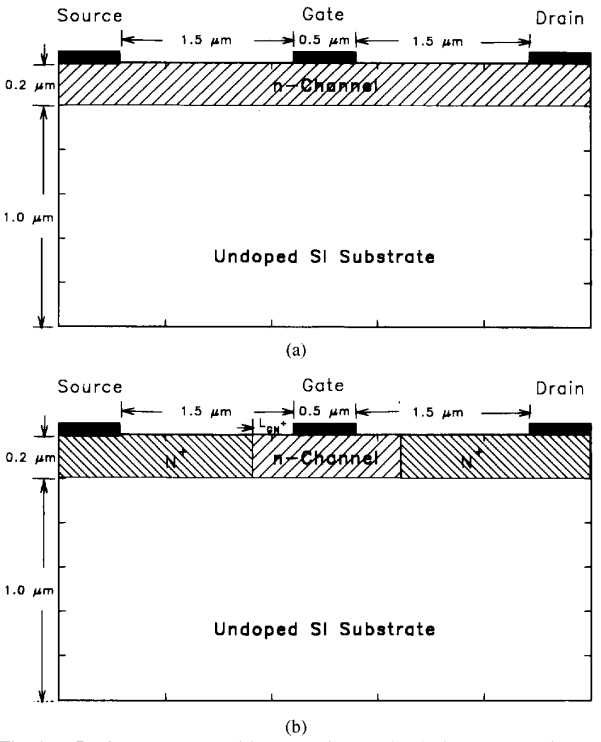

Fig. 1. Device structure used in the study. For the device structure shown in (b), a spacing is left between the N^+ region and the gate edge.

states at 0.7 eV below the conduction band edge, which agrees with the measured result. The electron and the hole emission rates for surface traps are two important physical parameters determining the charge trapping and detrapping rates for surface traps. From the conductance DLTS experiments on MESFET's performed by Zylbersztejn *et al.* [5] and Blight *et al.* [7], a large hole trap peak with an emission rate of about 100 s^{-1} appears around room temperature. From another conductance DLTS experiments by Harrang *et al.* [17], with the rate window varied from 8.656 ms to 0.4431 s, a large peak corresponding in sign to "hole-trap-like" also appears at around room temperature. Therefore, it is reasonable to assume the electron and the hole emission rates for acceptor-type surface states, i.e., $e_{pS,A}$ and $e_{nS,A}$, to be 100 s^{-1} at room temperature. We also assumed that the electron and the hole capture cross sections for the donor-type surface state were the same as those for the acceptor-type surface states, i.e., $\sigma_{pS,D} = \sigma_{pS,A}$ and $\sigma_{nS,D} = \sigma_{nS,A}$.

According to the Shockley-Read-Hall model, the rate equations for surface acceptor and donor traps can be expressed as

$$\frac{\partial N^-_{\mathrm{TS},A}}{\partial t} = \left[c_{nS,A}\left(N_{\mathrm{TS},A} - N^-_{\mathrm{TS},A}\right)n - e_{nS,A}N^-_{\mathrm{TS},A}\right] - \left[c_{pS,A}N^-_{\mathrm{TS},A}p - e_{pS,A}\left(N_{\mathrm{TS},A} - N^-_{\mathrm{TS},A}\right)\right] \quad (1)$$

$$-\frac{\partial N^+_{\mathrm{TS},D}}{\partial t} = \left[c_{nS,D}N^+_{\mathrm{TS},D}n - e_{nS,D}\left(N_{\mathrm{TS},D} - N^+_{\mathrm{TS},D}\right)\right] - \left[c_{pS,D}\left(N_{\mathrm{TS},D} - N^+_{\mathrm{TS},D}\right)p - e_{pS,D}N^+_{\mathrm{TS},D}\right] \quad (2)$$

where $N_{\mathrm{TS},A}$ and $N^{-}_{\mathrm{TS},A}$ denotes the total and the occupied acceptor-type surface state densities, respectively. The $c_{pS,A}$ and the $c_{nS,A}$, respectively, are the hole and the electron capture rates by the acceptor-type surface traps. The $e_{pS,A}$ and the $e_{nS,A}$, respectively, are the hole and the electron emission rates for the acceptor-type surface traps. The symbols used in (2) have similar meanings as those used in (1). The relationships between $c_{pS,A}$ and $e_{pS,A}$ and between $c_{nS,A}$ and $e_{nS,A}$ can be expressed as

$$\begin{aligned} c_{nS,A} &= \sigma_{nS,A} v_{n,\mathrm{th}} \\ c_{pS,A} &= \sigma_{pS,A} v_{p,\mathrm{th}} \\ e_{nS,A} &= c_{nS,A} N_C e^{-(E_G - E_{\mathrm{TV},A})/kT} \\ e_{pS,A} &= c_{pS,A} N_V e^{-E_{\mathrm{TV},A}/kT} \end{aligned} \tag{3}$$

where $v_{n,\mathrm{th}}$ and $v_{p,\mathrm{th}}$ are the thermal velocities of electrons and holes, respectively. For $e_{pS,A} = e_{nS,A} = 100\ \mathrm{s}^{-1}$, we have $\sigma_{pS,A} = 3.9 \times 10^{-11}\ \mathrm{cm}^2$ and $\sigma_{nS,A} = 6.4 \times 10^{-13}\ \mathrm{cm}^2$.

For boundary conditions at the ungated surface region, the total number of electrons and that of holes recombining at the surface per unit area and per unit time are

$$\begin{aligned} R_{nS} - G_{nS} = &\left[c_{nS,A}\left(N_{\mathrm{TS},A} - N^{-}_{\mathrm{TS},A}\right)n - e_{nS,A}N^{-}_{\mathrm{TS},A}\right] \\ &+ \left[c_{nS,D}N^{+}_{\mathrm{TS},D}n - e_{nS,D}\left(N_{\mathrm{TS},D} - N^{+}_{\mathrm{TS},D}\right)\right] \end{aligned} \tag{4}$$

$$\begin{aligned} R_{pS} - G_{pS} = &\left[c_{pS,A}N^{-}_{\mathrm{TS},A}p - e_{pS,A}\left(N_{\mathrm{TS},A} - N^{-}_{\mathrm{TS},A}\right)\right] \\ &+ \left[c_{pS,D}\left(N_{\mathrm{TS},D} - N^{+}_{\mathrm{TS},D}\right)p - e_{pS,D}N^{+}_{\mathrm{TS},D}\right] \end{aligned} \tag{5}$$

and the normal electrical field due to the surface charge can be described by

$$\vec{E} \cdot \hat{n} = \frac{q\left(N^{-}_{\mathrm{TS},A} - N^{+}_{\mathrm{TS},D}\right)}{\varepsilon} \tag{6}$$

where $\hat{n}$ denotes the unit vector normal to the surface and ε is the GaAs permittivity.

III. Analysis of Gate Lag Phenomenon

In this simulation, the source voltage and the drain voltage were fixed at 0 V and 2 V, respectively, and a square voltage pulse is applied to the gate contact at $T = 0$ s. The added voltage pulse has a width of 250 ms and has 1 ns rising and falling times. In our calculation, a constant time step, $\Delta T = 0.01/|V_G|$ ns, is used during the rising and the falling of gate voltage and a time-step selection scheme is adopted to reduce the total step number when the gate voltage is constant. Before the application of the gate voltage pulse, the device was at a steady state with an initial gate voltage. At $T = 0$ s, the voltage pulse is applied to change the gate voltage from the initial value to 0 V during 1 ns, and at $T = 250$ ms, the gate voltage is changed back to the initial voltage again during 1 ns.

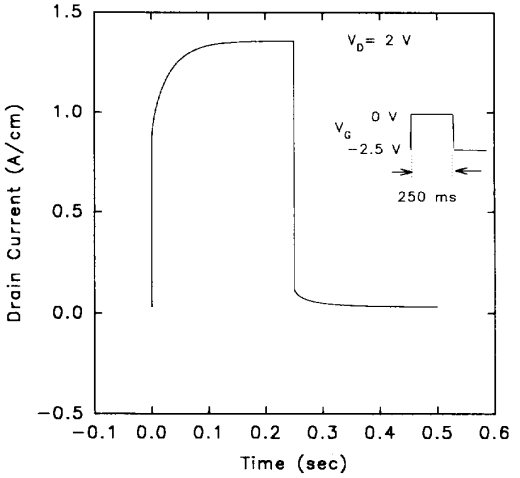

Fig. 2. Calculated drain lag phenomenon. The gate voltage is changed from −2.5 V to 0 V during 1 ns and immediately after 250 ms, the gate voltage falls to 0 V during 1 ns and is kept constant for another 250 ms.

After the gate voltage pulse, the gate voltage is kept constant for another 250 ms. The total time elapsing is 500 ms. Two quantities concerned with the gate lag phenomenon have been calculated in the simulation: the gate lag percentage and the lag time. The calculated gate lag percentage is defined as

$$\begin{aligned} &\text{Gate Lag } (\%) \\ &\quad = [I_D(T = 250\ \mathrm{ms}) - I_D(T = 1\ \mathrm{ns})]/I_D(T = 250\ \mathrm{ms}) \end{aligned} \tag{7}$$

where $T = 1$ ns is the time immediately after the rising of the gate voltage. The lag time is defined as the response time for the drain current to reach 0.99 I_D ($T = 250$ ms).

Fig. 2 shows the calculated current lag phenomenon for the device shown in Fig. 1(a). The surface states are assumed to be uniformly distributed with a density of $10^{14}\ \mathrm{cm}^{-2}$ along the top surface of the ungated access region. The initial gate voltage is −2.5 V. From the results, we found that immediately after gate voltage rising, the drain current is 0.8424 A/cm and is only partially on. The drain current is less than the steady-state drain current of 1.36 A/cm at $V_G = 0$. The drain current then gradually increases with time. The response time to reach a steady value is about 121 ms and the calculated gate lag percentage is about 36%. These results agree with the typical measured results for conventional MESFET's [1], [2]. At the falling edge of the gate voltage pulse, the drain current also does not return to the steady-state value immediately but falls to a value of 0.1223 A/cm before it slowly returns to zero. Comparing the current lag phenomena at the rising edge and the falling edge of the gate voltage pulse, the gate lag is clearly worse when the FET is turned on (from −2.5 V to 0 V) than when the FET is turned off (0 V to −2.5 V). This is consistent with the reported measured results [1].

The transient phenomenon can be best understood from the slow response of the surface traps and the bulk traps. In our calculation, we find the ionized donor-type surface trap

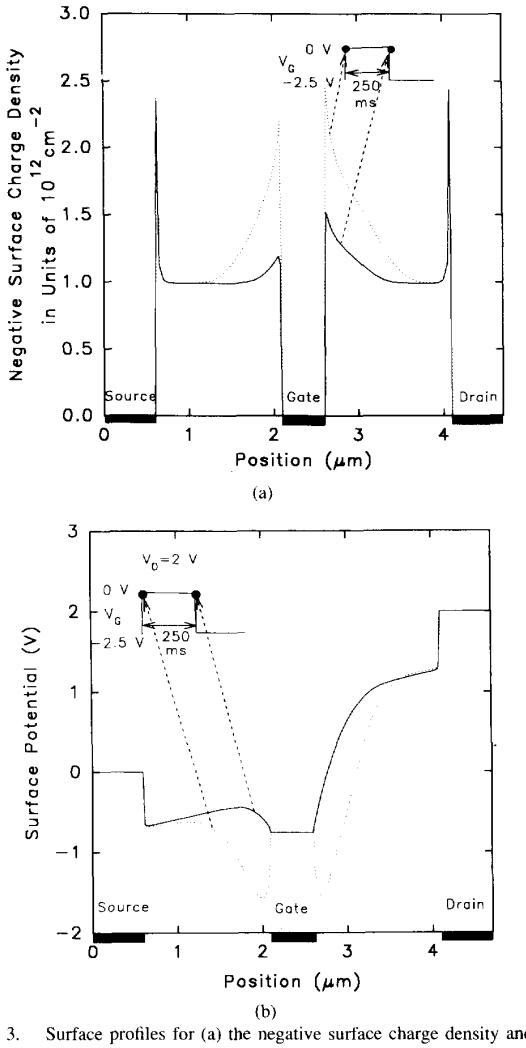

Fig. 3. Surface profiles for (a) the negative surface charge density and (b) the surface potential immediately after the rising of gate voltage and at steady state (T = 250 ms).

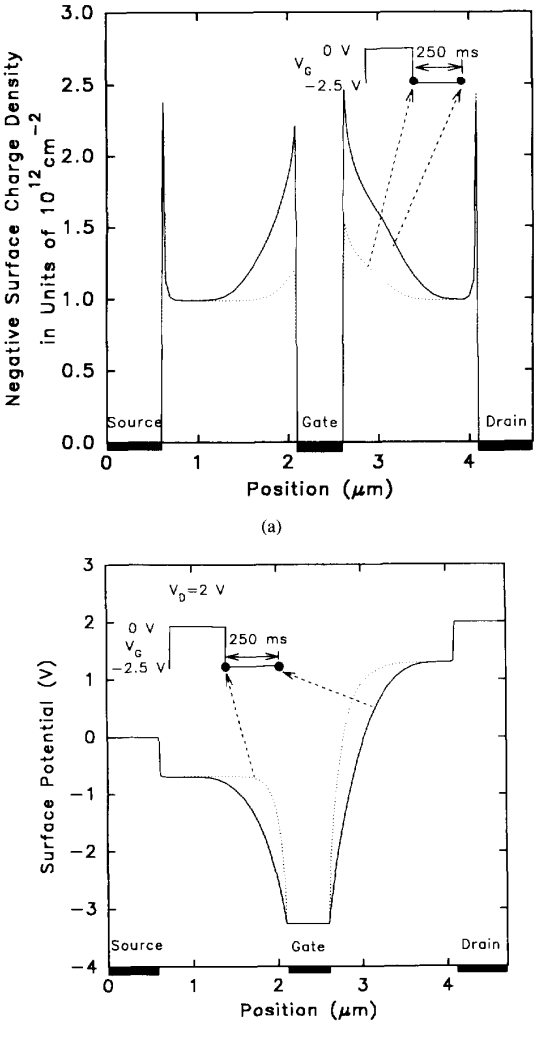

Fig. 4. Surface profiles of (a) the negative surface charge density and (b) the surface potential immediately after the falling of gate voltage and at steady state (T = 500 ms).

density, $N^{+}_{\mathrm{TS},D}$, is usually less than one-tenth of the occupied acceptor-type surface trap density, $N^{-}_{\mathrm{TS},A}$. The acceptor-type surface traps have a larger effect on the surface-related phenomena. The surface profiles for the negative surface charge density, $N^{-}_{\mathrm{TS},A} - N^{+}_{\mathrm{TS},D}$, and the surface potential immediately after the gate voltage rises and at steady state, are shown in Fig. 3(a) and 3(b), respectively. From Fig. 3(a), we can see that the negative surface charge density near the gate edge immediately after the gate voltage rises is about twofold higher than the value at steady state. The distribution of the surface potential, shown in Fig. 3(b), is consistent with the negative surface charge distribution shown in Fig. 3(a). Because of the surface states, a potential barrier exists at the surface. But because of the slow response of the surface states, the magnitude of the potential barrier and the population of the surface states can not follow the fast changes of the gate voltage. At the ungated surface near the gate edge the magnitude of the surface potential immediately after the rising of the gate voltage is much higher than that of the steady-state value.

The surface profiles for negative surface charge density and surface potential immediately after the gate voltage falls and at steady state ($V_G = -2.5$ V) are shown in Fig. 4(a) and 4(b). From Fig. 4(a), the negative surface charge density near the gate edge immediately after the gate voltage falls is twofold lower than that at steady state. Because of this, the magnitude of the surface potential immediately after drain voltage falls is lower than that at steady state. The situation, similar to what we have seen in Fig. 3, is again due to the slow response of the surface states.

To clearly see the effect of the slow response of the surface states and the bulk traps on the behaviors of the depletion widths at the ungated access region and at the

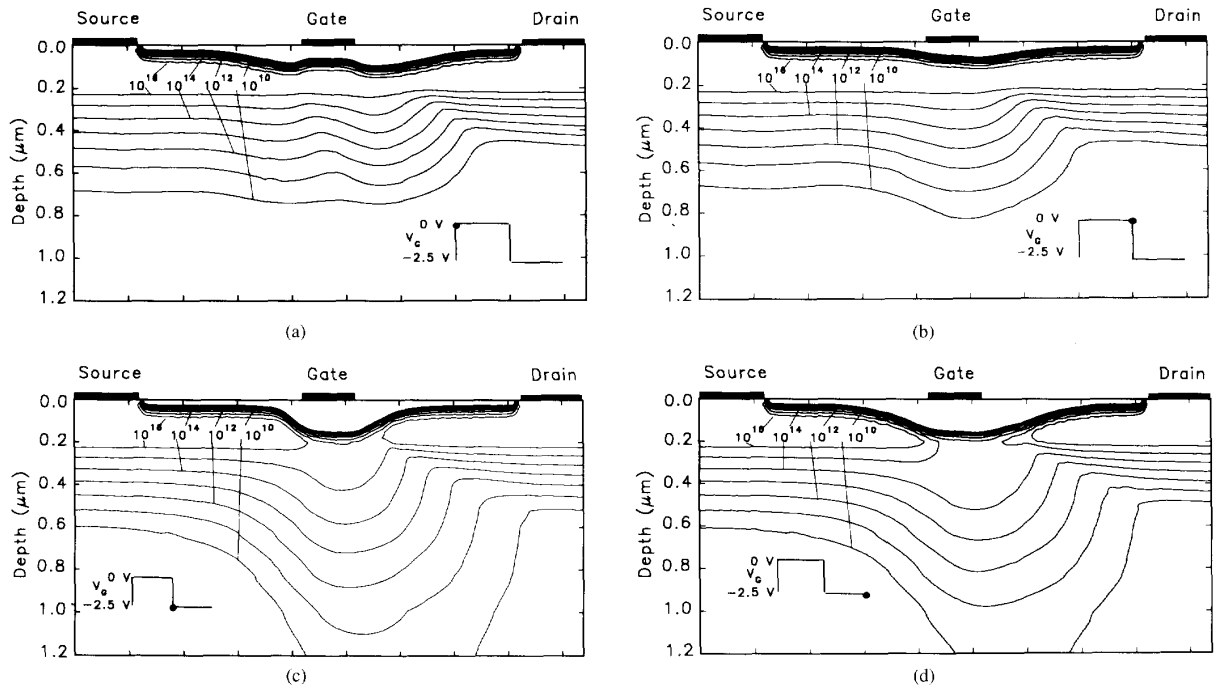

Fig. 5. Contour plots for free electron concentrations (a) immediately after the rising of gate voltage, (b) at steady state at $V_G = 0$ V, (c) immediately after the falling of gate voltage, and (d) at steady state at $V_G = -2.5$ V.

channel-substrate interface, the contour plots for free electron concentrations in the depletion regions near the surface and below the channel-substrate interface are illustrated in Fig. 5(a)–(d) at various times. Comparing Fig. 5(a), which is right after gate voltage rising, and 5(b), which is at the steady-state "on" condition, we can see the depletion region under the free surface is wider immediately after the gate voltage rises. But from the distributions of free electron concentrations below the channel-substrate interface, the total space charge is about the same for both cases, which implies that the depletion widths at channel-substrate interface are approximately equal. In other words, the bulk traps located at the channel-substrate interface contribute very little to the gate lag process. Because of a wider surface depletion region immediately after the gate is turned on, the parasitic resistance's, R_S and R_D, between the ohmic contacts and the Schottky contact are larger and the drain current is lower. As the surface states gradually reach steady state, R_S and R_D slowly decrease and the drain current recovers, resulting in the current lag phenomenon. Fig. 5(c) and 5(d) are the contour plots of free electron concentration right after the falling of the gate voltage and when the device is at the steady-state "off" condition. Again, we can see that the surface effect is much stronger than the bulk trapping effect. The surface depletion region is clearly narrower immediately after the gate is turned off than that at the steady "off" state. Because the gate is very small, the surface depletion can influence the channel charge under the gate. At the steady "off" state, the channel is pinched off. But during the transient state, the reduced surface depletion causes residual channel current flow. So the drain current does not go completely off when the gate is suddenly turned off.

Based on the analysis presented above, the gate lag phenomenon is caused by changes in the population of surface states at the ungated access regions of the device, resulting in time-dependent modulation of the surface depletion layer and the drain current. Our analysis supports Blight's explanation for the conductance transient of a GaAs MESFET following a long positive filling pulse to the gate (Fig. 6 and 7 in [7]).

IV. Explanation of Anomalous Hole-Trap-Like Signal in DLTS Measurements

Conductance DLTS measures small transient changes in the source-drain resistance of a MESFET operating in the linear region of its I-V curve as carriers are emitted from traps after they are filled by a filling gate pulse. It is commonly observed that in short-gate devices, the conductance DLTS spectra show a signal corresponding to a very large concentration of hole traps [5]. These observations are usually attributed to hole trapping at the active layer-substrate interface. However, Blight *et al.* presented a different explanation that, whereas a true DLTS signal arises from the re-emission, following a filling pulse, of charges trapped during the pulse, that anomalous "hole-trap" signal arises from the re-injection, after the pulse, of electrons into surface states that had emptied during the pulse [7]. He believed the hole-trap signal is a purely electronic phenomenon, and does not require generation of holes to explain it. However, Harrang *et al.* had done the conductance DLTS experiment under light exposure and

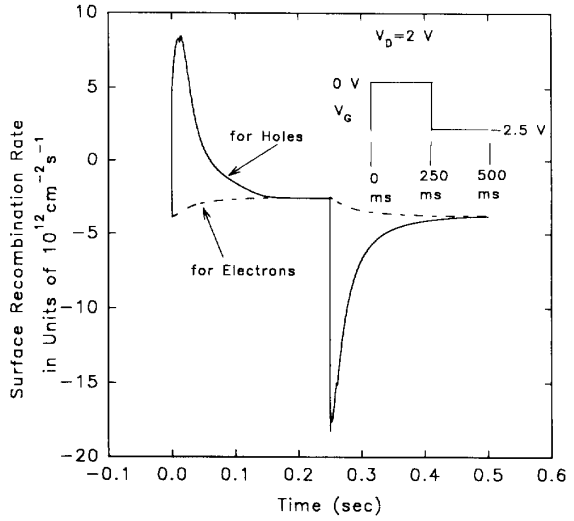

Fig. 6. Time-dependent net recombination rate for holes and electrons through surface traps at a position of 0.2 μm at the source side near the gate edge.

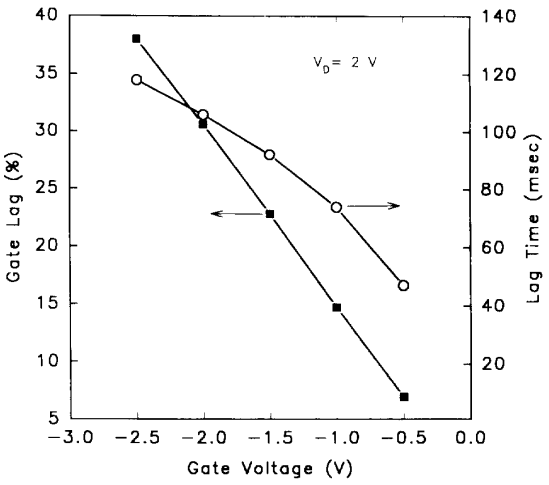

Fig. 7. Calculated lag percentage and lag time when the gate voltage is changed from −2.5, −2, −1.5, −1, and −0.5 V, individually, to 0 V.

suggested that the thermally activated surface-conductance channel might be due to hole conduction [17]. So, there still exists a controversy as to whether the hole or the electron conduction contribute to the hole trap-like signal. The principle of conductance DLTS techniques is basically very similar to our theoretical approach for studying the gate lag effect, except in our simulation, the MESFET is biased in the saturation region with a constant voltage, while in real conductance DLTS measurements, the drain is operated at a small constant current and the MESFET is always biased in the linear region. Despite the difference between the real conductance DLTS measurement and our simulation, the simulation approach is able to emulate the carrier emission and the capture processes through the deep level traps during DLTS measurements. The transient decrease of drain conductance (i.e., increase of drain resistance) in DLTS measurements just corresponds to the simulated transient decrease of the drain current after the gate voltage falls, as shown in Fig. 2.

The time-dependent net surface recombination rates for holes and electrons, $R_{pS} - G_{pS}$ and $R_{nS} - G_{nS}$, through surface traps at a position of 0.2 μm at the source side near the gate edge are monitored and plotted in Fig. 6. Initially, the device is at steady state and the net surface recombination rates for holes and electrons are negative and equal ($R_{pS} - G_{pS} = R_{nS} - G_{nS} = -3.79 \times 10^{12}$ cm^{-2}.s^{-1}). Immediately after the rising of the gate voltage from −2.5 V to 0 V, the hole surface recombination rate, R_{pS}, exceeds its emission rate G_{pS}, and the net recombination rate for holes becomes positive and is 4.73×10^{12} cm^{-2}.s^{-1} (at the end of the 1 ns rise time). After the gate voltage rises, $R_{pS} - G_{pS}$ first continues to rise to a maximum value of 8.44×10^{12} cm^{-2}.s^{-1}, then becomes negative and finally approaches a steady value of -2.59×10^{12} cm^{-2}.s^{-1} at about $T = 100$ ms, at which time $R_{pS} - G_{pS}$ and $R_{nS} - G_{nS}$ become equal again. It is noticed that during the 250-ms carrier filling pulse, the situation, $R_{pS} - G_{pS} > R_{nS} - G_{nS}$, is kept and therefore the negative surface charge density at the ungated surface region decreases with time. Right after the gate voltage falls (from 0 V to −2.5 V), $R_{pS} - G_{pS}$ becomes more negative ($R_{pS} - G_{pS} = -1.75 \times 10^{13}$ cm^{-2}.s^{-1}), i.e., the generation rate, $G_{pS} - R_{pS}$, becomes larger. As time proceeds, the drain current approaches its steady value (as shown in Fig. 2), and the net surface generation rate for holes is reduced and approaches the surface generation rate for electrons with a response time of about 150 ms. From Fig. 6, after the gate voltage falls to −2.5 V, $R_{pS} - G_{pS} < R_{nS} - G_{nS}$. So the negative surface charge density at the ungated surface region and thus the source-drain resistance increases with time. An increasing source-drain resistance just corresponds to the hole emission process measured by the conductance DLTS method. At all time, the net recombination rate for electrons, $R_{nS} - G_{nS}$, remains negative and approximately constant, i.e., no matter when the gate voltage rises or falls, the electrons are emitted from surface traps. From our simulated transient behaviors for DLTS measurement, we can find that the hole capture is the dominant process during the 250–ms long filling pulse and the hole emission is dominant after the filling pulse.

We can conclude that in conductance DLTS measurement on MESFET's, the hole-trap-like signal (the transient decrease in drain conductance corresponds to the transient current reduction after the gate voltage falls, as shown in Fig. 2), following a positive filling pulse, is primarily caused by the re-emission of holes trapped during the positive filling pulse. Our results support the explanation by Harrang *et al.*. Further explanation of the hole-trap-like signal will be reported elsewhere in the future.

V. Gate Voltage and Device Parameters Dependence

A. Gate Voltage Dependence

It has been found that the gate lag percentage increases with the magnitude of the gate voltage pulse [1]. We have studied

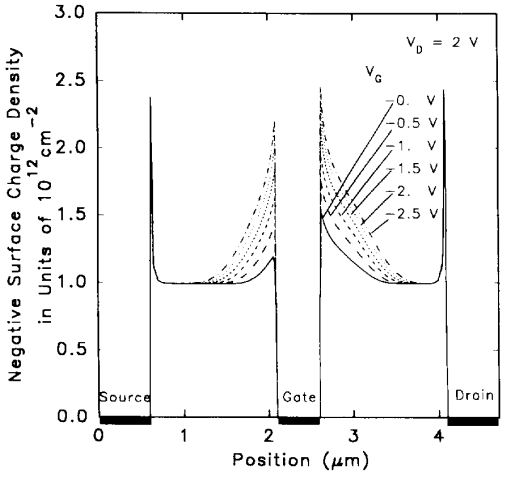

Fig. 8. Surface profiles for steady-state negative surface charge density at different gate voltages. The gate voltages are −2.5, −2, −1.5, −1, −0.5 and 0 V.

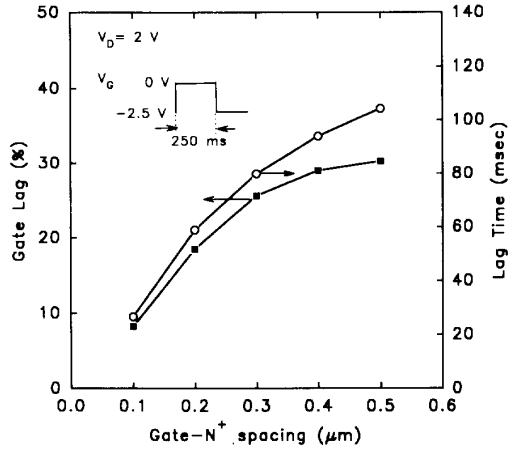

Fig. 9. Calculated gate lag percentage and lag time for five devices with spacing L_{GN^+} = 0.1, 0.2, 0.3, 0.4, and 0.5 μm.

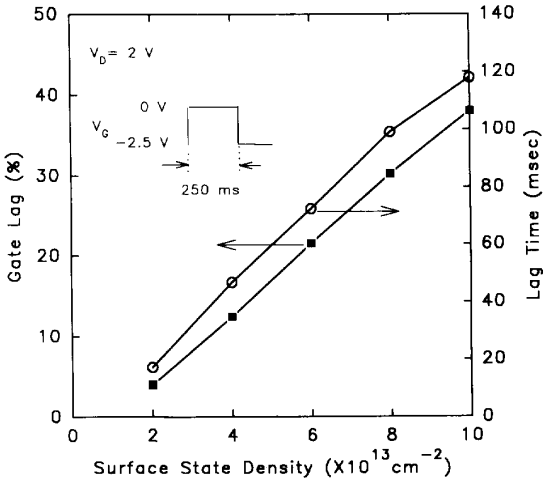

Fig. 10. Calculated lag percentage and lag time for devices with different total surface state densities. The densities used are 2×10^{13}, 4×10^{13}, 6×10^{13}, 8×10^{13}, 1×10^{14} cm^{-2}.

this effect with the device structure shown in Fig. 1(a) using different magnitudes of the gate pulses. Fig. 7 shows the lag percentage and the lag time when the gate voltage is changed from −2.5, −2, −1.5, −1, and −0.5 V, individually, to 0 V. The drain voltage is 2 V. From calculated results, the gate lag percentage and the lag time increase with the height of the gate pulse. For a pulse height of 0.5 V, the lag percentage and the lag time are reduced to 6.95% and 47 ms, respectively. To explain the dependence of the gate lag on pulse magnitude, the surface profiles for steady-state negative surface charge density at different gate voltages are shown in Fig. 8. For more negative gate voltages, the negative surface charge density at the ungated recess region near the gate edge is higher. Since at transient, the surface charge density changes between the values corresponding to the "low" state and the "high" state of the simulated FET, a larger change caused by a higher gate pulse gives rise to a stronger gate lag effect.

B. Different N^+-Gate Spacing

Yeats *et al.* found that for nonrecessed FET's, the gate lag effect depends on the spacing between the N^+ region and the gate. The effect is large unless the N^+-gate spacing is 0.5 μm or less. To confirm their results, we have simulated and compared devices with different N^+-gate spacings. The gate pulse used here is the same as before with a height of 2.5 V. The calculated gate lag percentage and lag time for five devices with spacing L_{GN^+} = 0.1, 0.2, 0.3, 0.4, and 0.5 μm are shown in Fig. 9. From this figure, the gate lag is significantly reduced for shorter N^+-gate spacings. With L_{GN^+} = 0.5 μm, the gate lag percentage and the lag time, respectively, are 30.2% and 104.3 ms. For a shorter spacing of 0.1 μm, the gate lag percentage is smaller than 9% and the lag time is reduced to 26.7 ms. Our calculated results are consistent with Yeats's experimental findings. The dependence of the gate lag effect on the N^+-gate spacing can be easily understood by the change in access resistance's, R_S and R_D, because of the change in spacing. The lower access resistance's caused by the reduced surface depletion due to the N^+ region result in lower gate lag effect.

C. Different Surface State Densities

According to reported experimental results, the gate lag effect and the frequency-dispersive transconductance seem somewhat sensitive to surface cleaning and passivation conditions [1], [2], [6]. Different surface passivation and cleaning condition can result in different surface state density. It is therefore worthwhile to study the dependence of the gate lag phenomenon on the surface state density. Devices with five surface state densities ($N_{TS,A} = N_{TS,D} = 2 \times 10^{13}$, 4×10^{13}, 6×10^{13}, 8×10^{13} and 1×10^{14} cm^{-2}) have been simulated. Fig. 10 shows our calculated results. When the surface state density decreases, both the gate lag percentage and the lag time decreases. For a device with a surface state density of

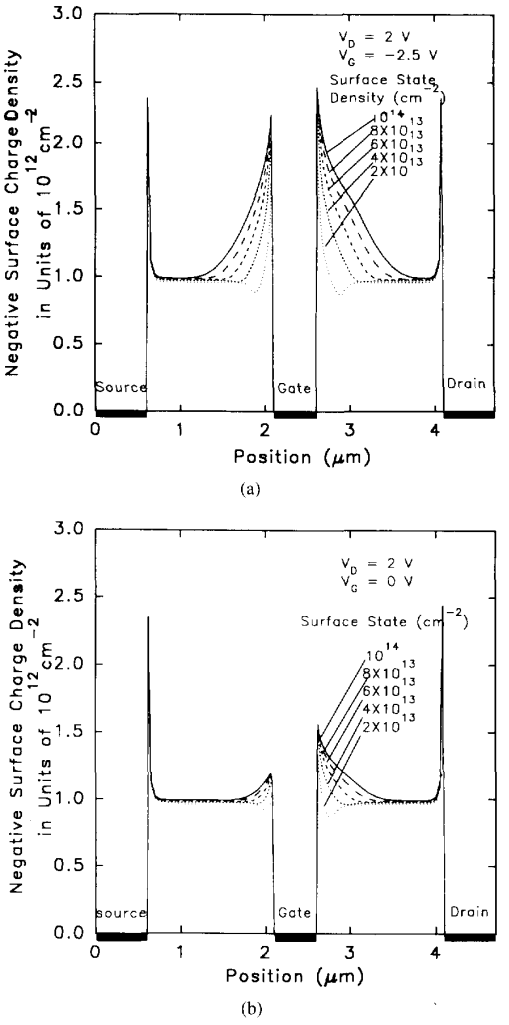

Fig. 11. Surface profiles for surface charge density for devices with different total surface state densities at (a) $V_G = -2.5$ and (b) 0 V. The densities used are the same as those in Fig. 10.

2×10^{13} cm^{-2}, the gate lag percentage and the lag time are only 4% and 17.3 ms, respectively. Both the lag parameters are approximately proportional to the surface state density.

Fig. 11(a) and 11(b), respectively, show the surface profiles of surface charge density at $V_G = -2.5$ and 0 V. Comparing devices with different surface state densities, we can see that the difference between the density profiles at $V_G = -2.5$ V and 0 V is more pronounced with a higher surface state density. This explains why the gate lag phenomenon is more serious for devices with worse surface cleaning and passivation conditions.

VI. Conclusion

A transient simulation of the gate lag phenomenon in GaAs MESFET's has been performed. It is found that the slow transient behaviors of the surface states existing at ungated access region are responsible for the gate lag effect. The bulk traps located at the channel-substrate interface have little effect on the transient process. The anomalous "hole-trap-like" signal for a MESFET in conductance DLTS measurement can be well explained by the re-emission of holes, which are captured during the positive filling pulse. The gate lag phenomenon is more pronounced when the magnitude of pulse increases. This is explained by the increased modulation of surface charge density at ungated access region near the gate edge. With extended N^+ region close to the gate, both the lag percentage and the lag time are reduced. This is because the modulation of the surface depletion region is less effective with the presence of the N^+ region. Both the lag percentage and the lag time are approximately proportional to the total surface state density. A good surface cleaning and passivation, which reduces the surface state density, should efficiently degrade the gate lag phenomenon and improve the device performance.

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