

## A Low-Power and Portable Spread Spectrum Clock Generator for SoC Applications

Duo Sheng, Ching-Che Chung, and Chen-Yi Lee

**Abstract**—In this paper, a novel portable and all-digital spread spectrum clock generator (ADSSCG) suitable for system-on-chip (SoC) applications with low-power consumption is presented. The proposed ADSSCG can provide flexible spreading ratios by the proposed rescheduling division triangular modulation (RDTM). Thus it can provide different EMI attenuation performance for various system applications. Furthermore, the proposed ADSSCG employs a low-power digitally controlled oscillator (DCO) to save overall power consumption significantly. Measurement results show that power consumption of the proposed ADSSCG is 1.2 mW (@54 MHz), and it provides 9.5 dB EMI reductions with 1% spreading ratio. Besides, the proposed ADSSCG has very small chip area as compared with conventional SSCGs which often required large on-chip loop filter capacitors. In addition, the proposed ADSSCG is implemented only with standard cells, making it easily portable to different processes and very suitable for SoC applications.

**Index Terms**—All digital spread spectrum clock generator (ADSSCG), digitally controlled oscillator (DCO), low power, portable, triangular modulation.

### I. INTRODUCTION

As the operating frequency of electronic systems increases, the electromagnetic interference (EMI) effect becomes a serious problem especially in consumer electronics, microprocessor ( $\mu$ P) based systems, and data transmission circuits [1]. The radiated emissions of system should be kept below an acceptable level to ensure the functionality and performance of system and adjacent devices [1], [2]. Many approaches have been proposed to reduce EMI, such as shielding box, skew-rate control, and spread spectrum clock generator (SSCG). However, the SSCG has lower hardware cost as compared with other approaches. As a result, the SSCG becomes the most popular solution among EMI reduction techniques for system-on-chip (SoC) applications [2]–[4].

Recently, different architectural solutions have been developed to implement SSCG. In [4], [5], a triangular modulation scheme which modulates the control voltage of a voltage-controlled oscillator (VCO) is proposed to provide good performance in EMI reduction. However, it requires a large loop filter capacitor to pass modulated signal in the phase-locked loop (PLL), resulting in increasing chip area or requirement for an off-chip capacitor. Modulation on PLL loop divider is another important SSCG type that utilizes a fractional-N PLL with delta-sigma modulator to spread output frequency changing the divider ratio in PLL [6], [7]. However, fractional-N type SSCG not only needs large loop capacitor to filter the quantization noise from the divider, but also induces the stability issue for the wide frequency spreading ratio applications, especially in PC related applications [7].

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In contrast, all-digital SSCG (ADSSCG) [8], [9] does not utilize any passive components and use digital design approaches, making it easily be integrated into digital systems. However, the delay line type ADSSCG [8] does not have the programmable spreading ratio functionality and needs an extra PLL to provide the frequency multiplication function. And the triangular modulation ADSSCG [9] has poor phase tracking capability resulting in loss of lock and stability issues. Moreover, it utilizes a delay non-monotonic digitally controlled oscillator (DCO) that is not suitable for SSCG application. Thus in this paper, a portable, low-power, and programmable spreading ratio ADSSCG with monotonic DCO is presented.

The proposed ADSSCG employs a novel rescheduling division triangular modulation (RDTM) to enhance the phase tracking capability and provide wide programmable spreading ratio. The proposed low-power DCO with auto-adjust algorithm saves the power consumption while keeping delay monotonic characteristic. This paper is organized as follows. Section II describes the proposed architecture and spread spectrum algorithm of ADSSCG. Section III focuses on the low-power DCO design and the auto-adjust algorithm for monotonic delay characteristic. In Section IV, the implementation and measurement results of the fabricated ADSSCG chip are presented. Finally, the conclusion is addressed in Section V.

### II. PROPOSED ADSSCG DESIGN

#### A. ADSSCG Architecture Overview

Fig. 1 illustrates the architecture of the proposed ADSSCG. It consists of five major functional blocks: a phase/frequency detector (PFD), an ADSSCG controller, a DCO, and two frequency dividers. The ADSSCG controller consists of a modulation controller, a loop filter, and a DCO code generator (DCG). The ADSSCG can provide the clock signal with or without spread-spectrum function based on the operation mode signal (MODE) setting. In the normal operation mode, the bang-bang PFD detects the phase and frequency difference between FIN\_M and DCO\_N. When the loop filter receives LEAD from the PFD, the DCG adds a current search step ( $S\_N[15:0]$ ) to the DCO control code, and this decreases the output frequency of the DCO. Oppositely, when the loop filter receives LAG from the PFD, the DCG subtracts the DCO control code to increase the output frequency of the DCO. When PFD output changes from LEAD to LAG or vice versa, the loop filter sends the code-loading signal (LOAD) to DCG to load the baseline code (BASELINE CODE[17:0]) which is averaged DCO control code by the loop filter. Before ADSSCG enters the spread spectrum operation mode, the baseline frequency will be stored as the center frequency. In the spread spectrum operation mode, the modulation controller uses two spreading control signals (SEC\_SEL[2:0] and STEP[2:0]) to generate the add/subtract signal ( $\pm\_SS$ ) and the spreading step ( $S\_SS[15:0]$ ) for the DCG, and then it modulates the DCO control code to spread out the DCO output frequency around the center frequency evenly.

The system clock of ADSSCG controller is FIN\_M whose operating frequency is limited by ADSSCG's closed-loop response time which is determined by the response time of the DCO, the delay time of the ADSSCG controller, and the frequency divider. Therefore, the period of FIN\_M should not be shorter than the shortest response time to ensure the ADSSCG functionality and performance. In addition, because the frequency of DCO\_N should be the same as FIN\_M after system locking, the frequency of FIN\_M can not be higher than the maximum frequency or lower than the minimum frequency of DCO\_N. As a result, the frequency range of FIN\_M is also limited by the DCO operating range and the divider ratio (N).

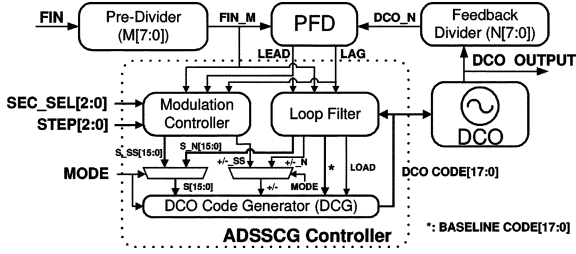


Fig. 1. Architecture of the proposed ADSSCG.

### B. Spread Spectrum Algorithm

Since triangular modulation is easy to be implemented and has good performance in reduction of radiated emissions, it becomes the major modulation method for SSCG [2], [4]. In triangular modulation, the EMI attenuation depends on the frequency-spreading ratio and center frequency, and it can be formulated as

$$A_{dB} = I + J \log \left( \frac{SR}{100} \right) + K \log(F_C) \quad (1)$$

where  $A_{dB}$  is the EMI attenuation,  $SR$  is the frequency spreading ratio,  $F_C$  is the center frequency, and  $I, J, K$  are modulation parameters [3]. Based on (1), under the same center frequency, EMI can be reduced further by increasing spreading ratio. In addition, under the same spreading ratio, the higher center frequency has better EMI attenuation performance.

Fig. 2(a) illustrates the conventional triangular modulation with digital approach [9]. Since the output frequency can be changed by the DCO control code, the output clock frequency can be spread by tuning DCO control codes with triangular modulation within one modulation cycle. In the beginning of the conventional spread spectrum, it will start at center frequency ( $T_c$ ) and take one-fourth of the modulation cycle time to reach the minimum frequency ( $T_{max}$ ), and then takes half of the modulation cycle time to reach the maximum frequency ( $T_{min}$ ). Finally, it will return to the center frequency in the last one-fourth modulation cycle time.

Because the upper half and lower half in the triangle have the same area, as shown in Fig. 2(a), the mean frequency of the spreading clock is equal to center frequency and the phase drift will be zero in the end of each modulation cycle. However, in the conventional triangular modulation, the ADSSCG controller can only perform phase and frequency maintenance based on the PFD's output in the end of each modulation cycle. Hence due to the frequency error between reference clock and output clock, reference clock jitter and supply noise, the phase error will be accumulated within one modulation cycle, leading to induce the loss of lock and stability problems.

Thus, in order to enhance phase tracking ability, the division triangular modulation (DTM) is proposed as shown in Fig. 2(b). DTM divides one modulation cycle into many subsections (for example in Fig. 2(b), modulation cycle divides into 16 subsections) and updates DCO control code for phase tracking in every 4 subsections. As a result, the ADSSCG controller can perform four times phase and frequency maintenance in one modulation cycle when modulation cycle divides into 16 subsections. Because DTM can provide the frequency spreading function and keep phase tracking at the same time, it is very suitable for ADSSCG in  $\mu P$ -based system applications. However the disadvantage of DTM is when the frequency changes to different sub-sections; it will induce large DCO control code fluctuations (7 S) as shown in Fig. 2(b), where  $S$  is the spreading step of DCO control code in spreading modulation.

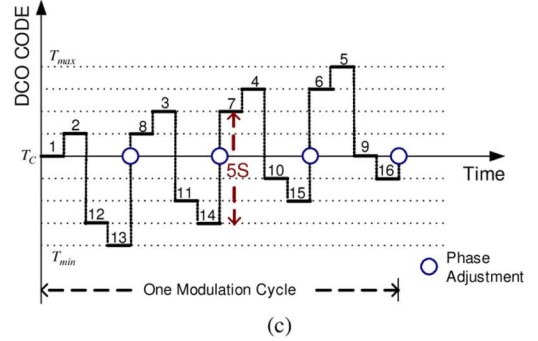
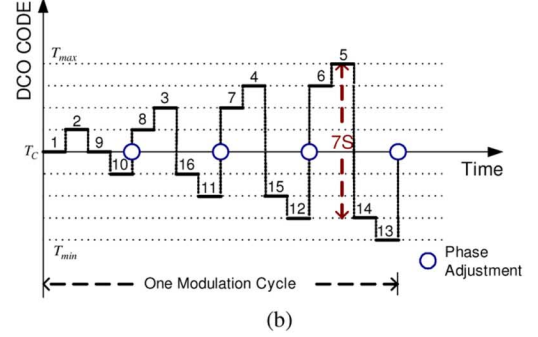
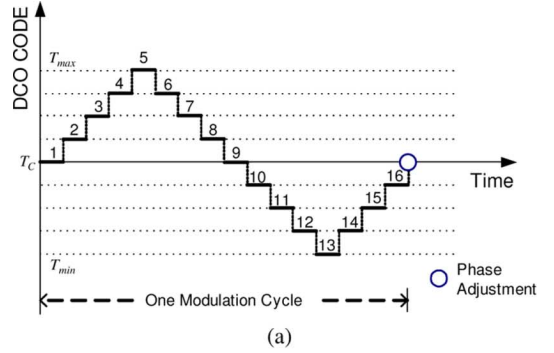


Fig. 2. (a) Conventional triangular modulation. (b) Division triangular modulation. (c) Rescheduling division triangular modulation.

In order to reduce the peak-to-peak value of DCO control code changing in DTM, the rescheduling DTM (RDTM) is proposed as shown in Fig. 2(c). By reordering the sub-sections in DTM, the peak-to-peak value of DCO control code changing can be reduced to 5 S. As a result, the peak-to-peak value of cycle-to-cycle jitter can be reduced while the period jitter is kept the same. Compared with DTM, the reduction ratio of peak-to-peak jitter by RDTM is related with number of subsection, and it can be formulated as

$$JR = \frac{\left( \left( \frac{\text{COUNT}}{2} \right) - 1 \right) - \left( \left( \frac{\text{COUNT}}{4} \right) + 1 \right)}{\left( \frac{\text{COUNT}}{2} - 1 \right)} \times 100\% \quad (2)$$

where  $JR$  is the jitter reduction ratio,  $\text{COUNT}$  is the number of sub-sections. For example, if there are 16 subsections, the jitter reduction ratio is 29% ( $(7-5)/7$ ), and if the number of subsection is 32, the jitter reduction ratio is 40% ( $(15-9)/15$ ). Although the order of subsections of DTM is rescheduled by RDTM to reduce the peak cycle-to-cycle jitter, the average cycle-to-cycle jitter still keeps the same as DTM. Besides, because the phase drift of the opposite direction in DTM and RDTM remains the same, the equivalent phase drift is zero. As a result, it will not induce an extra phase drift while the mean frequency remains the same. The results of frequency spread of DTM and RDTM

TABLE I  
JITTER AND TIMING COMPARISONS OF DTM AND RDTM

	DTM	RDTM
Positive Phase Drift: Upper Half Area (*)	1+3+5+7=16	1+3+5+7=16
Negative Phase Drift: Lower Half Area (*)	1+3+5+7=16	7+5+3+1=16
Average Cycle-to-Cycle Jitter (S)	$\frac{(1+1+1+2+1+3+1+4+1+5+1+6+1+7+1+4)/16}{40/16}=2.5$	$\frac{(1+4+1+5+1+4+1+5+1+4+1+5+1+4+1+1)/16}{40/16}=2.5$
Peak Cycle-to-Cycle Jitter (S)	7	5

\*: S times Period of Sub-Section

are the same as the conventional triangular modulation. Table I summarizes the jitter and timing comparisons of DTM and RDTM with 16 subsections within one modulation cycle.

With two control signals, spreading step ( $S$ ) and number of subsections (COUNT), the proposed RDTM can provide a flexible spreading ratio for different system requirements. Spreading step is the difference of DCO control code between two consecutive subsections. Number of subsections determines how many subsections in one modulation cycle. COUNT and  $S$  decoded from  $SEC\_SEL$  and  $STEP$  by the modulation controller, respectively. Based on the definitions, the frequency-spreading ratio equation can be given as

$$SR = \frac{\left(\frac{S \times RES \times COUNT}{2}\right)}{T_C} \times 100\% \quad (3)$$

where  $SR$  is the spreading ratio, RES is the finest time resolution of DCO, and  $T_C$  is the center period of DCO output clock. As a result, the frequency-spreading ratio of the proposed ADSSCG can be specified by the control signals easily.

### III. DIGITALLY CONTROLLED OSCILLATOR

#### A. The Proposed DCO Architecture

Because DCO occupies over 50% power consumption in all-digital clocking circuits, the proposed ADSSCG utilizes a low-power DCO structure to reduce overall power consumption [10]. To achieve the high portability of the proposed ADSSCG, all components in this ADSSCG including DCO are implemented with standard cells. Fig. 3(a) illustrates the architecture of the proposed low-power DCO which employs cascading structure for one coarse-tuning and three fine-tuning stages to achieve a fine frequency resolution and wide operation range. As the number of delay cell in the coarse-tuning stage increases, leading to have a longer propagation delay, the operating frequency of DCO becomes lower. The shortest delay path that consists of one NAND gate, one path MUX of coarse-tuning stage, and fine-tuning stage at the minimum delay determines the highest operation frequency of DCO. There are  $2^C$  different delay paths in the coarse-tuning stage and only one path is selected by the  $2^C$ -to-1 path selector MUX which controlled by C-bit DCO control code. The coarse-tuning delay cell utilizes a two-input AND gate which can be disabled when the DCO operates at high frequency to save power. In order to increase the frequency resolution of DCO, the three fine-tuning stages which are controlled by F-bit DCO control code are added into the DCO design. The first fine-tuning stage is composed of X hysteresis delay cells (HDC), and each of which contains one inverter and one tri-state inverter as shown in Fig. 3(b). When the tri-state inverter in HDC is enabled, the output signal of enabled tri-state inverter has the hysteresis phenomenon to increase delay [11]. Different digitally controlled varactors (DCVs) are exploited in the second and third fine-tuning stages to further improve

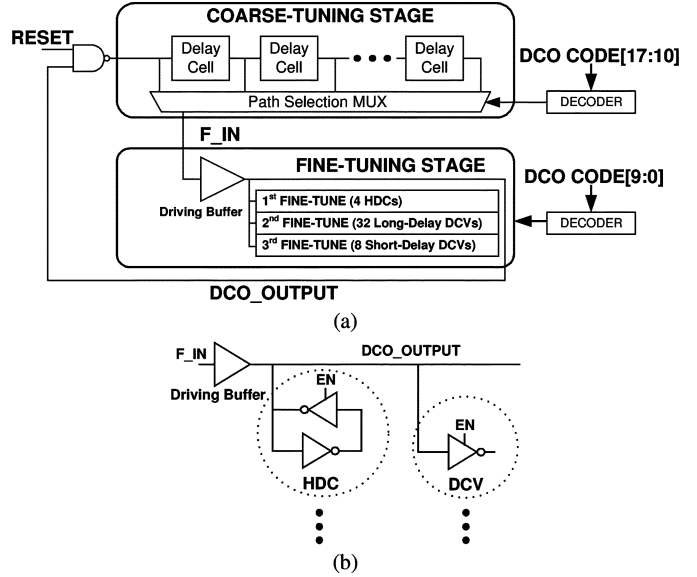


Fig. 3. (a) Architecture of the proposed DCO. (b) Fine-tuning cells of DCO.

TABLE II  
SIMULATION RESULTS OF DELAY OF TUNING STAGE

	Coarse-Tuning	1 <sup>st</sup> Fine-Tuning	2 <sup>nd</sup> Fine-Tuning	3 <sup>rd</sup> Fine-Tuning
Controllable Delay Range (ps)	61812	308.45	121.58	7.73
Finest Delay Step (ps)	242.41	102.82	3.92	1.1

the overall resolution of DCO as shown in Fig. 3(b). The operation concept of DCV is to control the gate capacitance of logic gate with enable signal state to adjust the delay time. The second and third fine-tuning stages employ Y long-delay DCV cells and Z short-delay DCV cells, respectively. Since the HDC can replace many DCV cells to obtain wider operation range, the number of delay cells connected with each driving buffer and loading capacitance can be reduced, leading to save power consumption and gate count as well.

Based on an in-house  $\mu P$ -based system for liquid crystal display (LCD) controller applications [12], the requested operating frequency is from 27 to 54 MHz. Thus the design parameters of the proposed DCO are determined as follows:  $C = 8$ ,  $F = 10$ ,  $X = 4$ ,  $Y = 32$ , and  $Z = 8$ . Table II shows controllable delay range and the finest delay step of different tuning stages in the proposed DCO under typical case (typical corner, 1.8 V, 25°C). It should be noted that the controllable delay range of each stage is larger than the finest delay step of the previous stage. As a result, the cascading DCO structure does not have any dead zone larger than the LSB resolution of DCO. Since the finest delay step of the third fine-tuning stage determines the overall resolution, the proposed DCO can achieve high resolution of 1.1 ps.

#### B. Auto-Adjust Algorithm for Monotonic DCO

As mentioned in the previous section, the DCO control code will be changed to obtain the different output periods in the spread spectrum applications, thus the monotonic characteristic of DCO is very important. Because the controllable delay range of each stage must be larger than the finest delay step of the previous stage, non-monotonic problem will occur when DCO code switches at the boundary of different tuning stages. To eliminate such non-ideal effects, an adjustable algorithm for boundary code switching is proposed. Fig. 4 is

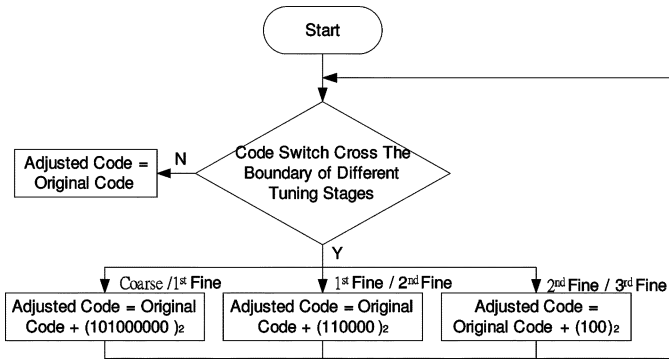


Fig. 4. Flowchart of auto-adjust algorithm.

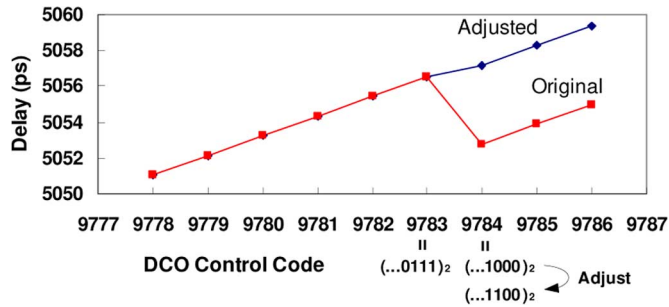


Fig. 5. Comparison between original and adjusted timing.

the flowchart of the proposed algorithm. When the DCO code crosses the boundary of different tuning stages, the DCO code will be adjusted by the ADSSCG controller to eliminate the non-monotonic issue automatically. If DCO code changes across boundary of different tuning stages, the original code will add or subtract the extra compensation code to reduce the delay difference caused by tuning stages switching. According to the simulation results of our proposed DCO under different process-voltage-temperature (PVT) conditions, the extra compensation code of across coarse/first fine, first/second fine, and second/third fine-tuning stage can be defined as 320, 48, and 4, respectively. For example, when the last four bits of DCO code (including one bit for second fine-tuning stage and last three bits for third fine-tuning stage) changes from  $(0111)_2$  to  $(1000)_2$ , the delay should increase 1.1 ps ideally, but it decreases 3.78 ps (from 7.7 to 3.92 ps which is the delay of one second fine-tuning cell) instead. Based on the auto-adjust algorithm, the code will adjust from  $(1000)_2$  to  $(1100)_2$ . As a result, the delay will increase 0.62 ps, leading to operate in a monotonic way as shown in Fig. 5.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

Based on the requested operating frequency for an in-house  $\mu P$ -based system and LCD controller [12] applications, the proposed ADSSCG should generate output clock ranges from 27 to 54 MHz. The proposed ADSSCG is designed and implemented by cell-based design flow, thus the proposed architecture and spread spectrum algorithm are modeled in Hardware Description Language (HDL) and functionally verified using NC-Verilog simulator. Moreover, we also use transistor-level simulator with Hspice to verify the DCO performance. Because the proposed ADSSCG is implemented with standard cells, the physical layout is generated by the auto placement and routing (APR) tool.

A test chip has been fabricated in 0.18- $\mu m$  1P6M CMOS process with area of 0.156 mm<sup>2</sup>, where the chip microphotograph is shown in Fig. 6. The ADSSCG output signal is measured using Agilent E4440A

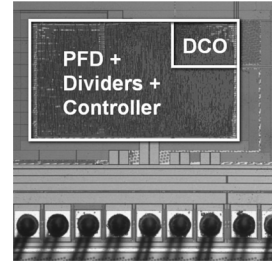


Fig. 6. Microphotograph of ADSSCG test chip.

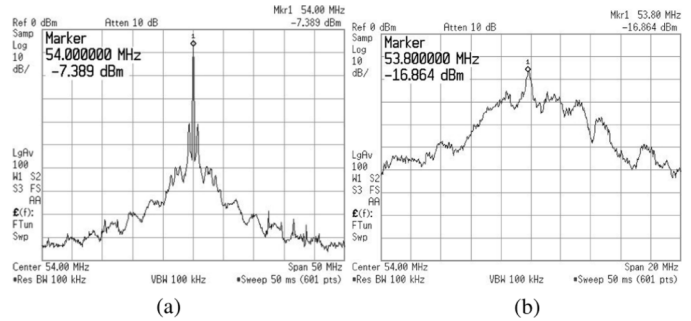


Fig. 7. Measurement spectrum of 54 MHz (a) without frequency spreading and (b) with 1% frequency spreading.

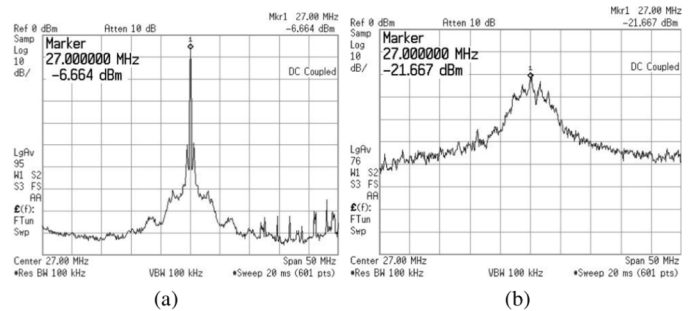


Fig. 8. Measurement spectrum of 27 MHz (a) without frequency spreading and (b) with 10% frequency spreading.

spectrum analyzer at 1.8 V/25 °C to test the performance. Fig. 7 shows the reduction of peak power is 9.5 dB at 54 MHz with 1% of spreading ratio, and the reduction of peak power is 15 dB at 27 MHz with 10% of spreading ratio is shown as Fig. 8. Figs. 7 and 8 shows the EMI can be reduced at the maximum and minimum operation frequency of the proposed design, respectively. Because RDTM is a kind of the triangular modulation, some peaks are happened in spectrum [1]. For the complex digital application in our system chip, ADSSCG operates under dirty power supply environment in the spread-spectrum operation mode, hence it increases noise floor of spread-spectrum operation mode as shown in Figs. 7(b) and 8(b), and the measured rms jitter is 94 ps at 54 MHz with frequency spreading. The total current consumption is 0.69 mA at frequency of 54 MHz.

Table III lists comparison results with the state-of-the-art SSCGs for clock generation applications. Based on the power index comparison, it is clear that the proposed ADSSCG can provide better power-to-frequency ratio, implying the proposed ADSSCG is more effective in power saving for a given operating frequency. In addition, since the proposed architecture is very simple and without passive components, it can achieve low-complexity and small-area compared with other SSCG designs. Although [8] occupies smaller area, it needs an extra PLL to provide the frequency multiplication function, and it can

TABLE III  
PERFORMANCE COMPARISONS

Performance Indices	Proposed	JSSC'03 [4]	TCASI'08 [5]	ISSCC'05 [6]	JSSC'07 [8]
Process	0.18 $\mu$ m CMOS	0.35 $\mu$ m CMOS	0.35 $\mu$ m CMOS	0.18 $\mu$ m CMOS	0.15 $\mu$ m CMOS
Design Approach	All-Digital	Analog	Analog	Analog	All-Digital
Modulation Type	Modulation on DCO	Modulation on VCO	Modulation on VCO	Modulation on Divider	Delay Line (2)
Application	$\mu$ P-based system/ LCD Controller	$\mu$ P-based system	$\mu$ P-based system	SATA I	DVD Player
Output Frequency (MHz)	27 ~ 54	66/133/266	50 ~ 480	1500	27
Spreading Ratio (%)	User-Defined (1)	0.5, 1, 1.5, 2, 2.5	0.5 ~ 2	0.5	3
EMI Reduction (dB)	15 @ 10%, 27MHz 9.5 @ 1%, 54MHz	4 @ 2.5%, 266MHz	16.6 @ 1.5%, 400MHz	9.8	13
Power Consumption (mW)	1.2 (@54MHz)	300 (@266MHz)	27.5 (@400MHz)	77 (@1.5GHz)	7.1 (@27MHz)
Power Index ( $\mu$ W/MHz)	22.2	1127.8	68.8	51.3	263
Area (mm <sup>2</sup> )	0.156	2.01 (Excluding loop filter)	0.66	0.31	0.06 (Excluding PLL)
Portability	Yes	No	No	No	No

(1) Based on timing constraint of system application (2) Needs an extra PLL

only provide the fixed frequency spreading ratio. Furthermore, since the proposed ADSSCG can be implemented with standard cells, it has a good portability and very suitable for SoC integration as compared with [4]–[6]. As a result the proposed ADSSCG has the benefits of better power consumption, programmable spreading ratio, area, and portability.

## V. CONCLUSION

In this paper, we proposed a portable, low power, and area-efficient ADSSCG with programmable spreading ratio for SoC applications. Based on the proposed RDTM, the spreading ratio can be specified flexibly by application demands while keeping the phase tracking capability. With the proposed low-power DCO, the overall power consumption can be saved. The proposed auto-adjust algorithm can maintain the monotonic characteristic of DCO. Measurement results show the proposed ADSSCG can achieve 9.5 dB EMI reductions with 1% frequency-spreading ratio and 1.2 mW at frequency of 54 MHz. As a result, our proposal achieves less power consumption and area with competitive EMI reductions. Moreover, because the proposed ADSSCG has a good portability as a soft intellectual property (IP), it is very suitable for SoC applications as well as system-level integration.

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