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Influences of SiO_x layer thickness on the characteristics of In–Zn–O/SiO_x/n-Si hetero-junction structure solar cells

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ABSTRACT

Indium zinc oxide (IZO) film was directly deposited on an n-type Si substrate by pulsed laser deposition (PLD) to form the IZO/SiO_x/n-Si hetero-junction solar cell. Analytical results indicated that the thickness and quality of the thermal SiO_x layer plays a prominent role in determining the conversion efficiency of the solar cell. The sample containing an about 1.78-nm-thick SiO_x layer exhibits an open-circuit voltage of 0.35 V, a short-circuit current density of 28.6 mA/cm^2, a fill factor of 34.3%, and an overall conversion efficiency of 3.4% under AM1.5 condition. The effects of the SiO_x layer thickness and the associated interface states on the carrier transport are discussed.

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1. Introduction

Photovoltaic devices based on the semiconductor-insulator-semiconductor (SIS) hetero-junction structures have attracted extensive research interests due to the advantages of a simple manufacturing process, relatively low cost and high efficiency [1–4]. In SIS devices, transparent conductive oxides (TCO) with a wide bandgap (E_g> 3 eV) serve as the transparent window of devices and the solar radiation is mainly absorbed by the Si substrate with E_g= 1.1 eV. There is a native SiO_x layer several nanometers in thickness that forms in between the TCO and Si substrate and it has been reported that such a thin insulator layer plays a key role in the performance of SIS devices [3].

Several SIS solar cells with high conversion efficiency (η) have been reported previously [1–4]. For instance, the devices containing indium tin oxide (In_2O_3 doped with 5 to 9 wt.% of SnO_2, ITO) [1–3] and tin oxide (SnO_2) [4] exhibited conversion efficiency (η) = 12% and 8%, respectively. However, the high deposition temperature of SnO_2 films (> 400 °C) and the high cost of ITO films severely hinder the development of these two PV device types. Recently, amorphous In–Zn–O (a-IZO) films with various In/Zn ratios have attracted considerable attention due to their low resistivity and high carrier mobility properties [5–9]. In particular, the relatively low In content in comparison with ITO and the low deposition temperature have made IZO a promising TCO alternative for the fabrication of SIS solar cells.

Our previous study employed the pulse laser deposition (PLD) method to fabricate the SIS solar cells by depositing an a-IZO film on n-type Si substrate clad with a thin SiO_x layer [10]. The SiO_x layer was grown by immersing the Si wafer in a hot H_2O_2 solution and the IZO film was deposited at the substrate temperature of 150 °C. The a-IZO/SiO_x/n-Si solar cell exhibited a η value of about 2.2% which is still remote from practical applications. Further, the open-circuit voltage (V_{oc}) of the device was about 0.24 V, only half of the reported value of 0.4–0.5 V [1–4]. In addition to the presence of interface states, the thickness and film quality of the SiO_x layer are the key factors affecting the performance of the SIS solar cells as suggested by Spitzer et al. [3]. This inspired us to form the SiO_x layer by means of a dry process instead of the wet process mentioned above.

In this study, we vary the substrate temperature to modulate the thickness of the SiO_x layer formed during PLD deposition which may serve as the tunneling layer of SIS devices. Systematic investigations were carried out to delineate the effects of the structure and properties of the top IZO layers as well as the thickness of the SiO_x layer on the characteristics of IZO/SiO_x/Si SIS devices. The microstructure, electrical and optical properties of the IZO films prepared at various PLD processing conditions were analyzed in conjunction with the morphology of the SiO_x layers grown on the Si substrates under various heating conditions and their correlations to the performance of SIS solar cells are discussed.

2. Experimental

The IZO targets for PLD deposition were prepared by using a mixture of In_2O_3 and ZnO (purity = 99.999% supplied by Gredmann) powders at the atomic ratio of In:Zn = 2:3. The mixed powders were homogenized by attrition milling, pre-calcinated at 600 °C in ambient air for 6 h, and then pressed at a pressure of 10 psi to form

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the pellets with diameters of one inch. Finally, the pellets were sintered at 1250 °C for 2 h to form the PLD targets.

Corning 1737 glass plates and *n*-type Si (100) wafers (resistivity = 2–5 Ω-cm) were adopted as the substrates for sample preparation. Before transferring to the PLD system, the glass and Si substrates were sequentially cleaned by immersion in deionized water, acetone and ethanol. For Si wafers, they were further immersed in a BOE solution for 3 min to remove the native oxide layer before PLD deposition. The thin-film deposition was carried out in a PLD system equipped with a KrF excimer laser (Compex 201; λ = 248 nm) and background pressure better than 2.7×10^{-4} Pa. The target-to-substrate distance was kept at 45–50 mm. During the deposition, the laser was operated at an energy density of 4.5 J/cm^2 per pulse with a repetition rate of 5 Hz. Prior to IZO deposition, the Si substrates were heated at temperatures of 100, 200, 300 or 400 °C for 5 min, respectively, so as to form the SiO_x layers with different thicknesses. Such insulating oxide layers were grown on the Si substrates via the dry thermal oxidization process by utilizing the residual oxygen in the PLD chamber as the reacting gas. Afterward, high purity argon (Ar; purity = 99.999%) was introduced into the vacuum chamber until reaching the working pressure of 0.57 Pa for the IZO deposition. The IZO films with thicknesses in the range of 45 to 55 nm were achieved as determined by the alpha-step profile meter (KOSAKA ET300). Subsequently, a layer of 100-nm thick aluminum (Al) was deposited by using *e*-beam evaporation to form the bottom electrode on the backside of the Si wafer and the finger electrodes on the top of the IZO layer.

The microstructures of the IZO films were separately analyzed by using an X-ray diffractometer (REGAKU; $\lambda_{Cu\text{-}K\alpha} = 0.15405$ nm, scan rate = 2 °/min) and a transmission electron microscope (JEOL JEM-2100 F). The electrical properties, including the resistivity, carrier concentration and Hall mobility, were measured by the van der Pauw method in the four-point probe system (All-real AHE-1000). The transmittance of IZO films was measured in the wavelength range of 200 to 1600 nm by an UV–vis-NIR spectrometer (JASCO, V-650). The density of the interface states (D_{it}) was calibrated by the photoresponsive *C-V* measurement [11] using a 20-W halogen lamp as a light source and a Wayne Kerr 6500B *C-V* meter at the frequency of 100 kHz. The open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and fill factor (FF) of the *a*-IZO/SiO_x/Si solar cells were characterized by the *J-V* measurements under AM 1.5 illumination in a solar cell efficiency measurement system equipped with a xenon lamp and a Keithley 2400 *I-V* source meter.

3. Results and discussion

Fig. 1 shows the XRD patterns of IZO films deposited at various substrate temperatures. The IZO film prepared at 100 °C is amorphous

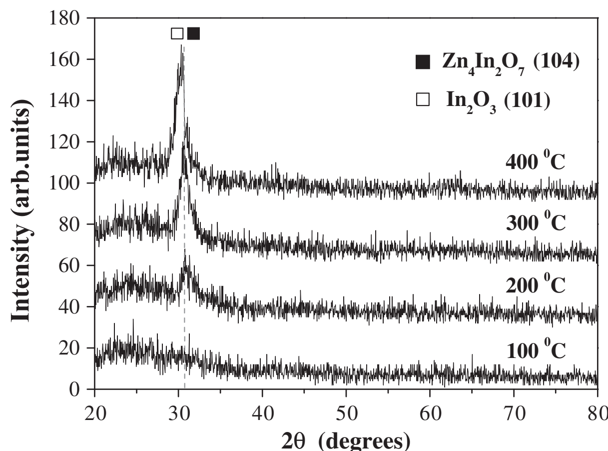

Fig. 1. XRD patterns of IZO films prepared on a glass substrate at various substrate temperatures.

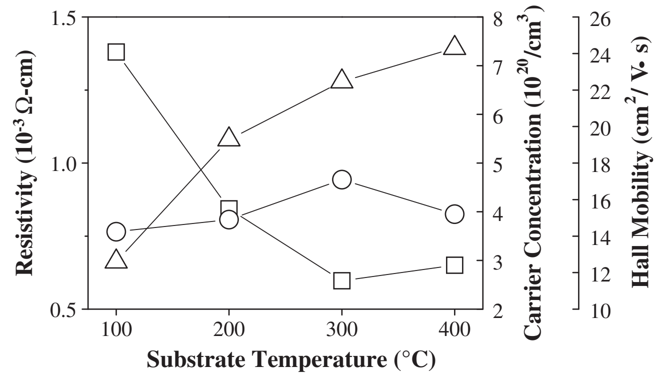

Fig. 2. Resistivity (□), carrier concentration (○), and mobility (△) as functions of the substrate temperature of IZO films deposited on a glass substrate.

whereas a broad peak at $2\theta = 30.9$ ° emerges for those obtained at substrate temperatures above 200 °C and its intensity increases progressively with the increase of substrate temperature. The diffraction peak possibly originates from the (222) diffraction of the bixbyite structure of In_2O_3 ($2\theta = 30.6$ °) or the (101) diffraction of the spinel structure of $Zn_4In_2O_7$ ($2\theta = 31.0$ °). According to the phase diagram of the binary In_2O_3–ZnO system reported by Moriga et al. [5], both of the In_2O_3 and $Zn_4In_2O_7$ phases might form in the IZO film when the $Zn_4In_2O_7$ homologous compound or the In_2O_3–ZnO ceramic target was used. Moreover, the XRD peak shifts toward the small diffraction angle side when the substrate temperature is increased. This is ascribed to the increase of mutual solubility of In_2O_3 and ZnO, which causes more In atoms to occupy the Zn sites and thus results in the lattice expansion [12].

The electrical characteristics of the IZO films deposited at various substrate temperatures are depicted in Fig. 2. It can be seen that the resistivity decreases with the increase of substrate temperature and reaches a value as low as 6.0×10^{-4} Ω-cm at the substrate temperature of 300 °C. The carrier concentration of IZO films, on the other hand, varies mildly in the range of 3.6×10^{20} to 4.6×10^{20} cm^{-3} and is relatively insensitive to the change of substrate temperature. The Hall mobility of IZO films, nevertheless, increases monotonically from 12 to 24 cm^2/V·s with the increase of temperature. The decrease of resistivity and increase of mobility with the increase of temperature is ascribed to the improvement of IZO crystallinity as indicated by the XRD analysis shown in Fig. 1. Consequently, it is conceived that IZO films with lower resistivity and higher mobility may be obtained when the processing temperature is high. Note that even though the crystallinity was improved by increasing the substrate temperature, the IZO layers prepared in this study should possess a relatively fine grain structure due to the wide full-width-

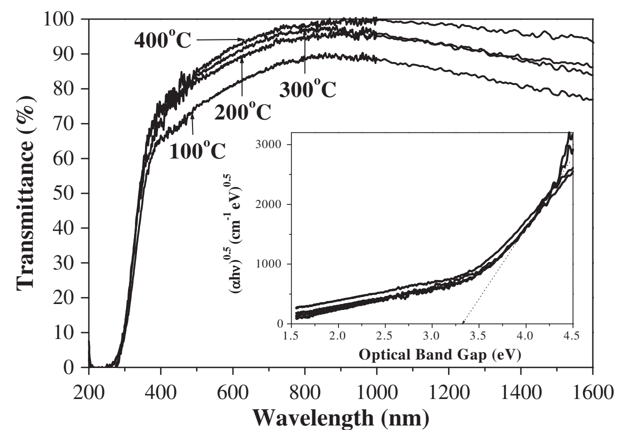

Fig. 3. Transmittance spectra of IZO films prepared at various substrate temperatures. The inset shows the determination of E_g by extrapolating the plot of $\sqrt{\alpha h\nu}$ against $h\nu$.

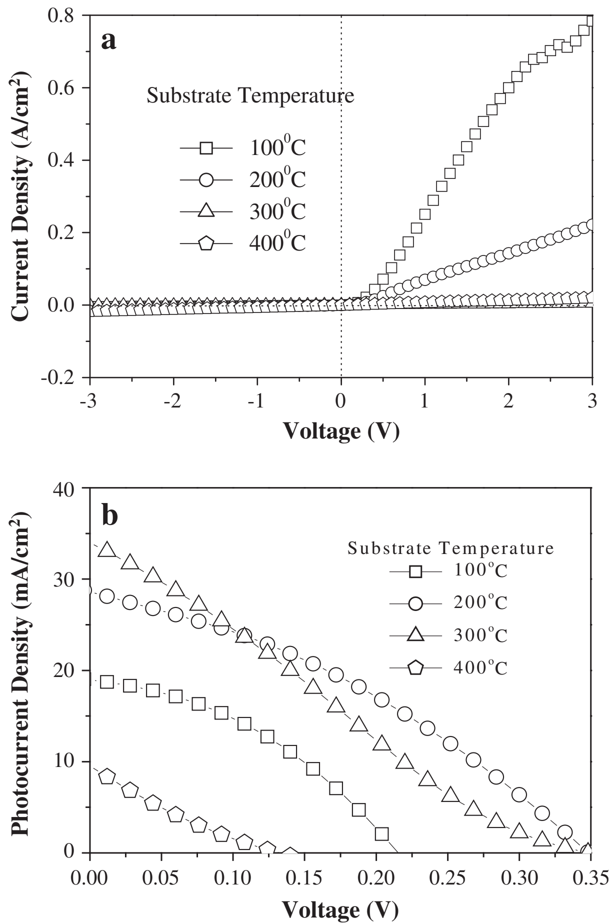

Fig. 4. *J-V* characteristic of SIS devices measured (a) in the dark and (b) at the AM1.5 illumination condition.

half-maximum of the XRD peak as depicted in Fig. 1. It is believed that the relatively high In_2O_3 content implies a mixture of amorphous and nano-scale grain structures in the IZO films, in contrast to the columnar structure observed in IZO films with low In_2O_3 contents.

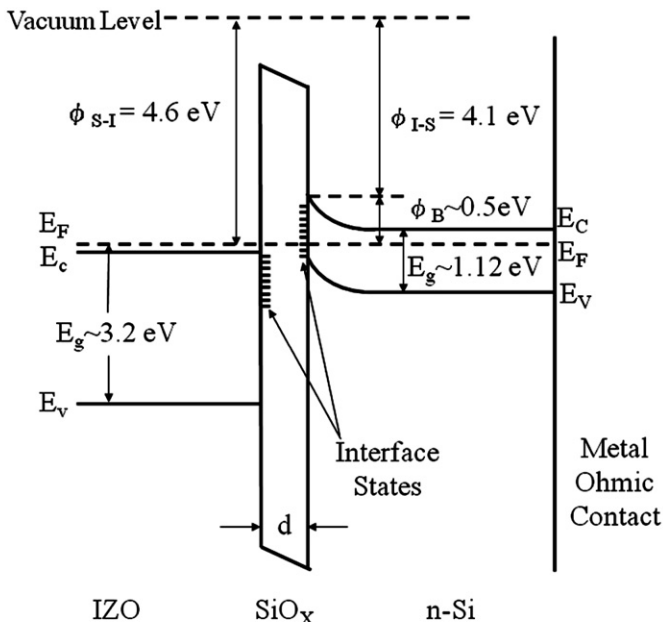

Fig. 5. Schematic energy band diagram of the IZO/SiO_x/*n*-Si hetero-junction structure.

Fig. 3 presents the transmittance of IZO films prepared at various substrate temperatures. Except for the IZO films deposited at 100 °C, all films exhibit high transparency (80%) in visible-light wavelength range. Furthermore, it is evident that the increase of substrate temperature, hence improved crystallinity of IZO films, results in a shift of the absorption edge toward the shorter wavelength region. The E_g values of the samples can be obtained by the Tauc relationship [13]:

$$\alpha = A\left(h\nu - E_g\right)^r \tag{1}$$

where α is the absorption coefficient, A is a constant, h is the Plank's constant, ν is the frequency of the incident light, and $r = 2$ for an indirect band-gap semiconductor. As revealed by the inset in Fig. 3, the values of E_g of the IZO films are in the range of 3.20–3.35 eV as determined by extrapolating the plot of $\sqrt{\alpha h\nu}$ against $h\nu$.

Fig. 4(a) shows the current density-voltage (*J-V*) characteristics of the SIS devices measured in a dark environment. The rectifying behavior of the samples deposited at 100 and 200 °C suggests that these devices are of the SIS type [14]. Based on the E_g values obtained in Fig. 3 and the *J-V* characteristics, the devices are believed to consist of the IZO/SiO_x/*n*-Si tri-layer structure and the corresponding energy band diagram is depicted schematically in Fig. 5. In the diagram, $\phi_{\text{S-I}}$ and $\phi_{\text{I-S}}$ are the work functions of IZO and Si, respectively. The theoretical upper limit of the barrier height, ϕ_B, i.e., the difference between ϕ_{S-I} and ϕ_{I-S} would be 0.5 eV as indicated in Fig. 5 [15]. Thus, when a forward bias is applied to the device, the current is dominated by the electrons tunneling from *n*-Si into IZO because of the relatively

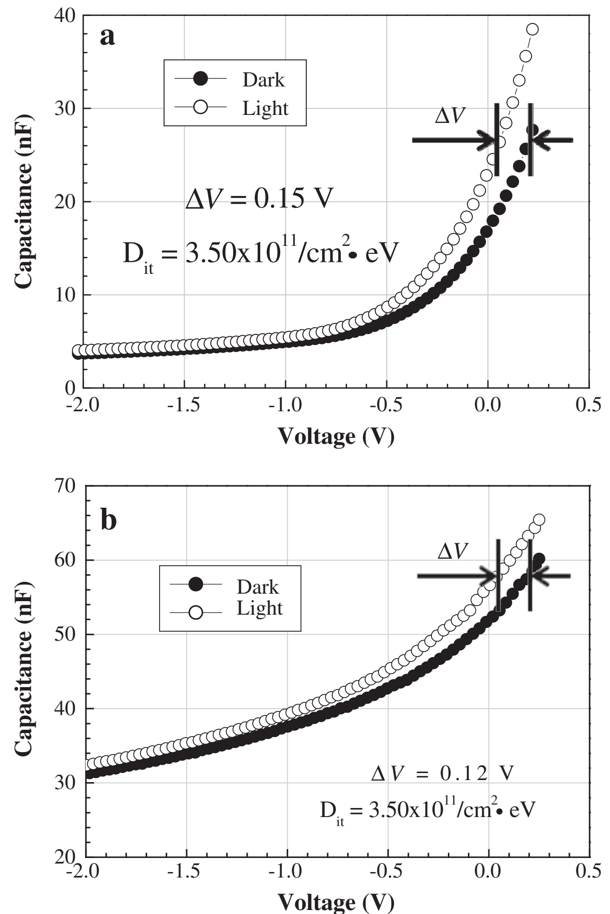

Fig. 6. Photoresponsive *C-V* characteristics of SIS devices prepared at substrate temperatures of (a) 200 and (b) 400 °C.

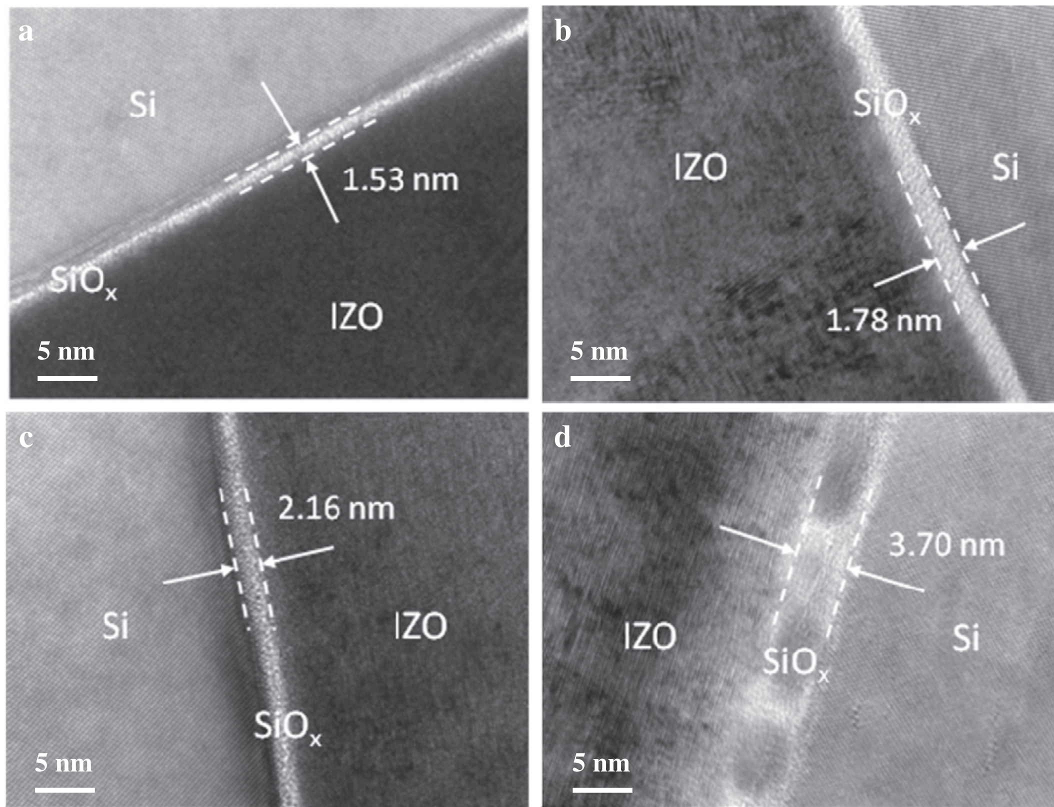

Fig. 7. Cross-sectional TEM micrographs of SIS devices prepared at substrate temperatures of (a) 100, (b) 200, (c) 300 and (d) 400 °C.

higher $\phi_{S\text{-}I}$ in the devices. In principle, the tunneling current would decrease rapidly with increasing SiO_x layer thickness. Hence, the results displayed in Fig. 4(a) indicate that the thickness of the SiO_x layer might vary markedly with the substrate temperature.

Moreover, the value of ϕ_B is intimately correlated with the V_{oc} of the devices in accord with the theoretical model proposed by Shewchun et al. [1–3]. The interface traps at the IZO/SiO_x interfaces and SiO_x/Si interfaces (denoted as interface states in Fig. 5) may also restrict the carrier tunneling process and result in the suppression of V_{oc} of the SIS devices. In order to obtain the interface properties of SIS structures, a photoresponsive *C-V* measurement was carried out. The value of D_{it} can be estimated by using the equation [11]:

$$D_{it} = \frac{C_i \Delta V}{q E_g} \tag{2}$$

where C_i is the capacitance of the insulator layer, ΔV is the voltage shift caused by the change in charges at the Si surface states, q is the charge of the electron, and E_g is the bandgap of the insulator layer. Fig. 6(a) and (b) presents the photoresponsive *C-V* characteristics of the SIS devices prepared at substrate temperatures of 200 and 400 °C, respectively. According to Eq. (2), the D_{it} of the SIS solar cell samples prepared at 200 and 400 °C were found to be 3.50×10^{11} and $1.35 \times 10^{11}\,\text{cm}^{-2}\text{eV}^{-1}$, respectively. According to the numerical solution of transport equations reported by Spitzer et al. [3], the V_{oc}, FF and η of the SIS solar cell can be improved by the decrease of D_{it} since it would result in a decrease in the interface state recombination current density and a decrease in the charge capture or trapping. As to a J_{sc} property, their calculation revealed it is insensitive to the change of D_{it}. Spizter et al. also reported that the effective fixed insulator charges at SiO_x/Si interface may be dependent on the insulator growth procedure. The fixed insulator charge decreases with the increase of substrate temperature, implying the increase of V_{oc} and J_{sc} of SIS device. Our analysis indicated that the SIS sample prepared at 400 °C in fact exhibited the lowest η value although the increase of the substrate temperature suppressed the D_{it}. The irrelevance of cell performance to the change of D_{it} might be ascribed to the comparatively low D_{it} values in our samples which are about two orders of magnitude lower than the results reported previously [16,17]. Since the D_{it} decrement did not imply the improvement of η, the thickness of the SiO_x layer is hence the dominant factor on the performance of SIS solar cells prepared in this study. This is illustrated by the *J-V* characteristics of SIS devices measured under the AM1.5 illumination condition shown in Fig. 4(b) and the TEM characterization presented in Fig. 7. Table 1 lists the V_{oc}, J_{sc}, FF, and η deduced from the *J-V* profiles of the devices shown in Fig. 4(b). As shown in Table 1, the J_{sc} decreases with increasing substrate temperature for IZO film deposition, presumably due to the increasing thickness of SiO_x layers deposited at high temperatures.

Fig. 7(a)–(d) shows the cross-sectional TEM images of the SIS devices prepared at various substrate temperatures. According to the lattice fringe emerging in the IZO portion, the crystallinity of the IZO films is progressively improved with the increase of substrate temperature, which is consistent with the XRD results presented in Fig. 1. Furthermore, it is also apparent that an ultra-thin thermal oxide layer presents between the IZO layer and Si substrates in all the samples prepared in this study. The thicknesses of the SiO_x layers deposited at 100, 200, 300, and 400 °C are found to be about 1.53,

Table 1
PV characteristics of IZO/SiO_x/*n*-Si solar cells prepared at various substrate temperatures.

Substrate temperature (°C)	SiO_x thickness (nm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
100	1.53	0.22	18.79	38.66	3.16
200	1.78	0.35	28.60	34.28	3.42
300	2.16	0.35	34.01	23.73	3.01
400	3.70	0.13	9.52	19.75	0.25

1.78, 2.16, and 3.70 nm, respectively. The influence of the thickness variation of the SiO_x layer on the performance of the SIS devices can be understood as follows. For instance, the device fabricated at 400 °C exhibited a low J_{sc} of 9.5 mA/cm^2 and a relatively low η of 0.25%, which might have resulted from the thick SiO_x layer (about 3.70 nm) as seen in Fig. 7(d). It resulted in the increase in the series resistance of the SIS device, leading to the decrease of J_{sc} and consequently the degradation of carrier tunneling efficiency. On the other hand, the IZO/SiO_x/*n*-Si devices fabricated at 200 °C exhibits the highest η of 3.4% with the corresponding V_{oc}, J_{sc} and FF of 0.35 V, 28.6 mA/cm^2 and 34.3%, respectively. The substantial improvement on J_{sc} illustrates that an adequate thickness (1.8–2.0 nm) of the interfacial SiO_x layer is essential to the performance of SIS solar cells, which is in agreement with the theoretical prediction [18].

Finally, we note that the utilization of dry thermal oxidization in forming the SiO_x layer benefits the performance of the SIS sample in comparison with the sample prepared by using the wet process [10]. It is well known that the dry method is able to produce the SiO_x layer with a dense structure and less crystalline defects. Hence, the quality of the SiO_x layer is also a decisive factor affecting the SIS solar cell performance.

4. Conclusions

This work demonstrates a simple fabrication process of IZO/SiO_x/*n*-Si SIS solar cells by directly depositing IZO films on the *n*-type Si substrates. Prior to the IZO deposition, the thin SiO_x layers were formed on Si wafers via the dry thermal oxidization method in the temperature range of 100–400 °C to serve as the carrier tunneling layer. Analytical results indicated that an adequate thickness of the interfacial oxide layer is essential to optimize the electrical properties of the SIS devices. The SiO_x layer formed at 200–300 °C with a thickness of about 1.8–2.0 nm was found to imply the best device performance with V_{oc}, J_{sc}, FF and η of 0.35 V, 28.6 mA/cm^2, 34.3% and 3.4%, respectively.

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