Surface & Coatings Technology 231 (2013) 281–284

Contents lists available at ScienceDirect

Surface & Coatings Technology

journal homepage: www.elsevier.com/locate/surfcoat

N_2O plasma treatment suppressed temperature-dependent sub-threshold leakage current of amorphous indium–gallium–zinc-oxide thin film transistors

Geng-Wei Chang [a], Ting-Chang Chang [b,*], Jhe-Ciou Jhu [b], Tsung-Ming Tsai [c], Yong-En Syu [b], Kuan-Chang Chang [c], Fu-Yen Jian [b], Ya-Chi Hung [c], Ya-Hsiang Tai [a]

[a] Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsin-Chu, 300, Taiwan, ROC
[b] Department of Physics and Center for Nanoscience & Nanotechnology, National Sun Yat-sen University, 70 Lien-hai Road, Kaohsiung, Taiwan, ROC
[c] Institute of Materials Science and Engineering, National Sun Yat-Sen University, Kaohsiung, 70 Lien-hai Road, Kaohsiung, 804, Taiwan, ROC

ARTICLE INFO

Available online 4 May 2012

Keywords:
Indium gallium zinc oxide (IGZO)
Thin film transistors (TFTs)
N_2O plasma treatment

ABSTRACT

N_2O plasma treatment suppressed the temperature-dependent sub-threshold leakage current of amorphous indium–gallium–zinc-oxide thin film transistors (a-IGZO TFTs). For untreated devices, the transfer curve exhibited abnormal electrical properties at high temperature. The abnormal electrical properties are explained by the energy band diagrams for both forward and reverse sweep. Above 400 K, holes can be generated from trap-assisted transition, and drift to the source side which induces source barrier lowering. The source side barrier lowering enhances electron injection from the source to channel and causes an apparent sub-threshold leakage current. This phenomenon, which is experimentally verified, only appears in the device without N_2O plasma treatment, but not in the device with N_2O plasma treatment. The results suggested that the density of states for a-IGZO with N_2O plasma treatment is much lower than that without plasma treatment.

1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) represented by amorphous-In–Ga–Zn–O (a-IGZO) are widely accepted as channel layers of thin-film transistors (TFTs) in next generation flat-panel displays because their TFTs have better characteristics than those of hydrogenated amorphous silicon (a-Si:H) TFTs. For example, a-IGZO TFTs exhibit large filed-effect mobility ~10 cm^2/V s [1,2], large on/off current ratio $>10^8$ [3], and good stability against electrical stress [4–8]. Furthermore, the low process temperature and low cost are desirable for large flat panel display applications [9–13]. Therefore, several applications such as active-matrix liquid-crystal displays (AMLCDs), active-matrix organic light-emitting-diode (AMOLED) displays, and electronic paper (e-paper) have been demonstrated using a-IGZO TFTs as driving/switching TFT arrays. These mobile displays are often used in harsh environments such as on hot dashboards in cars. Therefore, it is important to determine to what extent the performance and reliability of a-IGZO TFTs depend on temperature. In this paper, we investigate the temperature dependence of the a-IGZO TFT and explain it with energy band diagrams. Also, the device further was given negative bias stress under the different temperatures to confirm that the holes are induced by thermal-generation. In addition, we propose the fabrication of high-performance a-IGZO TFTs with a post treatment of N_2O-plasma. The stability of the untreated and the N_2O-plasma treated a-IGZO TFTs are examined by negative gate-bias stress as well as at different temperature to realize the influence of N_2O-plasma treatment on the device properties.

2. Experiment

Bottom gate coplanar a-IGZO TFTs were produced on glass substrate in this work. The plasma enhanced chemical vapor deposition (PECVD)-derived SiOx (300 nm) film as gate insulator was grown at 370 °C, over the patterned Ti/Al/Ti (50/200/50 nm) trilayer gate electrodes. The Ti/Al/Ti (50/200/50 nm) source/drain electrodes were formed by sputtering and then patterned into the dimension of channel width/length (W/L) = 5–30 μm/10 μm. A 30 nm thick a-IGZO film was deposited by dc magnetron sputtering system at room temperature, using a target of In:Ga:Zn = 1:1:1 in atomic ratio, a plasma discharge power of 300 W, and an ambient gas mixture ratio of $O_2/Ar = 6.7\%$ with a working pressure of 5 mTorr. To investigate the effects of the fabrication conditions on the electrical stability of a-IGZO TFTs, the fabricated TFTs were divided into two groups. After defining the active region, one group of TFTs was treated with N_2O plasma to passivate the defects in a-IGZO film. Finally, all of the devices were capped with a 200 nm SiOx layer by PECVD at 170 °C, and sequentially annealed in an oven at 330 °C for 2 h. The electrical properties of a-IGZO TFTs with

* Corresponding author.
E-mail address: tcchang@mail.phys.nsysu.edu.tw (T-C. Chang).

0257-8972/$ – see front matter © 2012 Elsevier B.V. All rights reserved.
doi:10.1016/j.surfcoat.2012.04.086

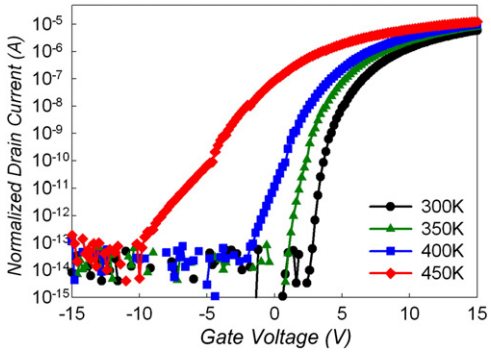

Fig. 1. Transfer characteristics for the untreated a-IGZO TFTs at different temperatures.

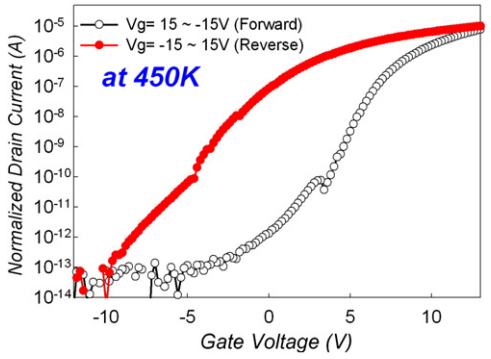

Fig. 2. Transfer characteristics of a-IGZO TFTs without N_2O plasma treatment on active layer. Measurements were done in dark with forward ($V_g = -15$–15 V, $V_d = 5$ V) and reverse ($V_g = 15$ to -15 V, $V_d = 5$ V) sweep.

$L = 10\,\mu m$ and $W = 25\,\mu m$ were analyzed using Agilent B1500A Semiconductor Device Analyzer in dark.

3. Results and discussion

The transfer characteristics of a-IGZO TFTs at different temperatures are shown in Fig. 1. As seen in this figure, the curves shift to the left with increase temperature. Also, the drain current in the entire Vg region increases with increasing temperature. The threshold voltage (V_T) is determined when the normalized drain current ($NI_D = I_D \times L/W$) reaches 10^{-9} A. Below 400 K, the V_T decreases proportionally with the rising temperature. It is well known for oxide semiconductors that the free electrons in the materials are mainly generated by oxygen vacancies [14,15]. Thermal excited oxygen atoms that can leave their original sites induce vacancies with remaining free electrons at the sites. The excited oxygen atoms that have left their original sites then move into the interstitial sites. The lower V_T observed at the higher temperature can be attributed to these free electrons generated along with the oxygen vacancies [16,17]. Therefore, the threshold voltage substantially shifts toward the negative Vg direction with increasing temperature. Moreover, the transfer curves display an abnormal phenomenon above 400 k. The transfer curve exhibits an apparent subthreshold leakage current stretch-out phenomenon at high temperatures. The stretch-out phenomenon becomes more serious with increase temperatures. Moreover, we measured the devices with forward sweeping (gate voltage sweeps from -15 V to 15 V) and reverse sweeping (gate voltage sweeps from 15 V to -15 V). An obvious hysteresis phenomenon ($\triangle V_H = 8.2$ V) appears in untreated a-IGZO TFTs as shown in Fig. 2. The shift of transfer curve in hysteresis loops is attributed to the interface states. For forward sweeping, the interface states discharge the trapped carriers initially and then begin trapping carriers while gate bias sweeps into the subthreshold region. In addition, it should be noted that the transfer characteristics at room temperature (300 K) were reproducible after the measurements at high temperatures, implying that the change in the transfer characteristics due to increasing temperature is reversible.

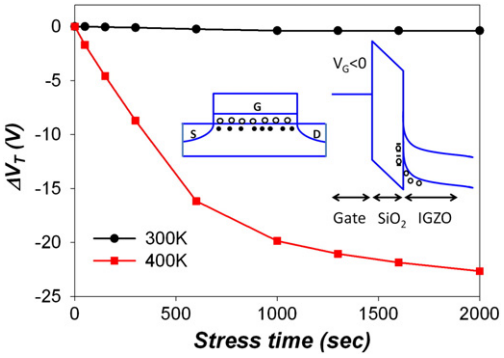

Fig. 4. Dependence between stress time and V_t shift (ΔV_T) during negative bias stress for untreated device at 300 K and 400 K.

Next, we discuss the unique behavior of the subthreshold leakage current for a-IGZO TFTs at high temperatures. There are two distinctive regions in the transfer characteristics. We expediently define the critical voltage, Vc, which separates the stretch-out and above-critical regions, as a gate voltage when the NI_D reaches 10^{-10} A. When the gate voltage is below Vc, the thermal-induced hole moves to the source side due to the transverse electric field. Then, the holes accumulate at the source region that leads to the source side barrier lowering. The source side barrier lowering enhances electron injection from the source and causes an apparent subthreshold leakage current as shown in Fig. 3(a). Once the gate voltage over Vc, as shown in Fig. 3(b), the transfer characteristics are dominated by the barrier between the a-IGZO and source. The barrier height becomes

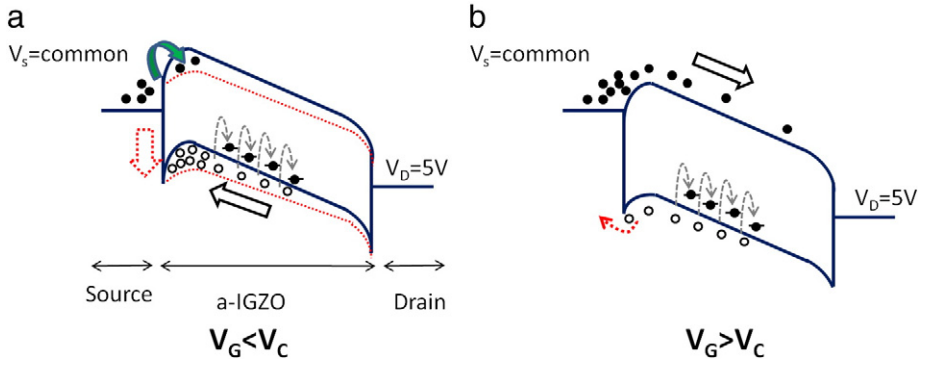

Fig. 3. Schematic energy band diagram operated in (a) off-state ($V_g < 0$ V, $V_d > 0$ V) and (b) on-state.

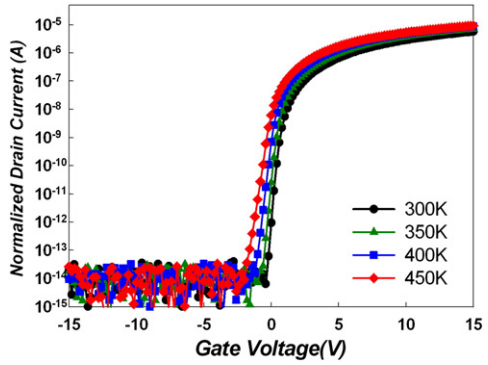

Fig. 5. Transfer characteristics for the N_2O-plasma treated a-IGZO TFTs at different temperatures.

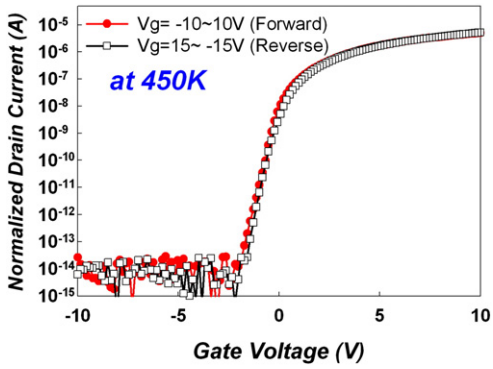

Fig. 6. Transfer characteristics of a-IGZO TFTs with N_2O plasma treatment on active layer. Measurements were done in dark with forward ($V_g = -15$–15 V, $V_d = 5$ V) and reverse ($V_g = 15$ to -15 V, $V_d = 5$ V) sweep.

much lower with the increase of gate voltage. Holes could not accumulate at the source region because of the lower barrier height. Thus, for above critical region, the electron injection from the source depends on the gate voltage. Therefore, the transfer curve separates into two regions with increasing gate voltage.

In order to further confirm that the hole is induced thermally, the device was stressed with negative gate bias ($Vg = -30$ V) at 300 K and 400 K, respectively. The V_T was measured before and after the application of the stress and the shift in V_T is plotted in Fig. 4. At 300 K, the ΔV_T almost has no shift under negative gate bias stress, where $\Delta V_T = V_T(t) - V_T(t=0)$. Negative gate bias stress is often reported to result in negligible changes in V_T [18–21]. The invariability of V_T with a negative bias on the gate can be explained by the lack of holes in channel. However, the V_T value was shifted significantly to the negative direction by 22.6 V after 2000 s stress

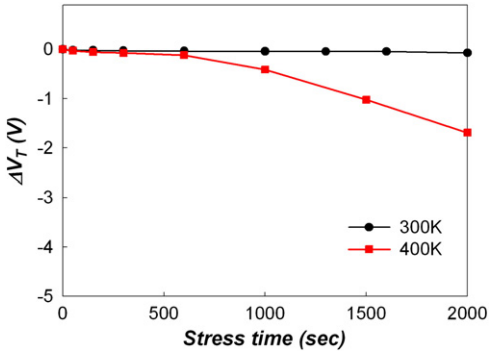

Fig. 8. Dependence between stress time and V_t shift (ΔV_T) during negative bias stress for N_2O plasma treated device at 300 K and 400 K.

time at the 400 K. It is suggested that the thermal-induced hole carriers are attracted to the gate dielectric layer by the negative gate voltage and become trapped in the gate dielectric or at the dielectric/channel interface. The trapped hole could induce more electrons to the channel to turn on the TFT more easily. Therefore, at 400 K, the negative bias stress causes a significant negative threshold voltage shift.

The transfer characteristics of the N_2O-plasma treated a-IGZO TFTs at different temperatures are shown in Fig. 5. Comparing with the untreated devices, the N_2O-plasma treated a-IGZO TFTs exhibit superior electrical properties. As seen in this figure, the curves shift to left direction slightly with increase temperature. Also, the drain current in the entire Vg region increases with the increase temperature. The improvement in the transfer characteristic indicates the termination of defects at the a-IGZO/dielectric interface and in the a-IGZO bulk. This can be ascribed to the reduction in oxygen vacancy by N_2O-plasma. Moreover, N_2O plasma treatment can significantly suppress the temperature-dependent sub-threshold leakage current stretch-out phenomenon of a-IGZO TFTs. In addition, in Fig. 6, the hysteresis phenomenon was suppressed for N_2O plasma treatment at 450 K. The stability of transfer curve in hysteresis loops indicates that the interface states reduce significantly after N_2O plasma treatment. Therefore, the N_2O-plasma treated a-IGZO TFTs have superior electrical properties.

In addition, Fig. 7(a) and (b) shows the transfer characteristics of untreated and N_2O plasma treatment devices at 300 K, respectively. The untreated devices exhibits an apparent hysteresis phenomenon of $\Delta V_T = 1.85$ V. On the contrary, the N_2O plasma treatment devices show an insignificant hysteresis phenomenon of $\Delta V_T = 0.02$ V. For the untreated devices, the apparent hysteresis phenomenon can be attributed to the extra trap states generated during the deposition of SiO_2 passivation layer by PECVD [22]. For N_2O-plasma treatment devices, N_2O-plasma treatment is applied to a-IGZO active layer and

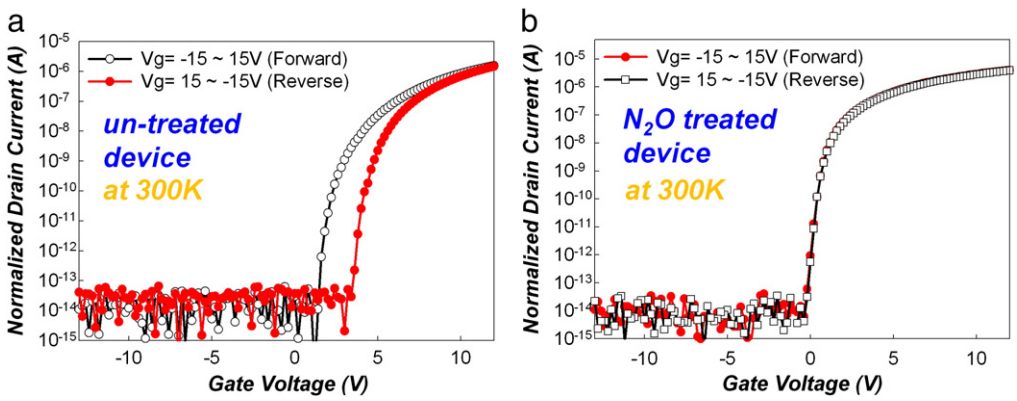

Fig. 7. Transfer characteristics of untreated and N_2O plasma treatment devices at 300 K, respectively.

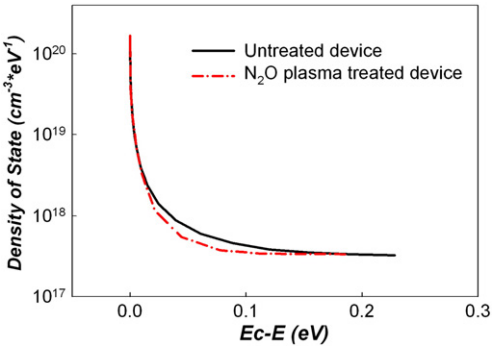

Fig. 9. Calculated DOS distribution as a function of the energy (Ec-E) for the untreated device and the N_2O plasma treated device.

oxygen-rich region is formed near the back channel by the N_2O-plasma treatment which effectively prevents the damage during SiO_2 deposition process [23]. Therefore, the N_2O treated devices have better electrical properties when compared to the untreated devices.

In order to confirm the N_2O-plasma treated a-IGZO TFTs have superior reliability, the bias stability test is carried out with stress condition of $V_G = -30$ V and $V_{S,D} = 0$ V at different temperature. Fig. 8 shows the shift of threshold voltage for N_2O-plasma treated device during bias stress at 300 K and 400 K. At 300 K, negative gate bias stress is often reported to result in negligible changes in V_T. The invariability of V_T with a negative bias on the gate can be explained by the lack of holes in channel. However, comparing with the untreated devices, the V_T value of the N_2O-plasma treated a-IGZO TFTs was slightly shifted to the negative direction after 2000 s stress time at the 400 K. It is suggested that the hole is still lack in channel at high temperature due to the less interface states.

Fig. 9 shows the DOS distribution as a function of energy for the untreated and N_2O-plasma treated a-IGZO TFTs. The DOS extracted reported in the previous work [24]. The total DOS for N_2O-plasma treated device was much smaller than that of the untreated device over the entire tailing energy range extracted. This further suggests that N_2O-plasma treated devices have superior performance. The total DOS value at a specific energy is the summation of the interfacial trap density (N_{it}) and the semiconductor film (N_{ss}) because both trap states hinder the rise of the E_F level at the interface with increasing V_{GS} ($>V_{FB}$). Considering that the IGZO channel layers for both devices were formed under identical deposition conditions, the difference in the total distribution can be explained by the N_2O plasma treatment. This suggests that the N_{it} for untreated device is larger than that of the N_2O-plasma treated device. Therefore, the better performance for N_2O-plasma treated device can be attributed to the reduced N_{it} at the IGZO interface.

4. Conclusion

In conclusion, the N_2O-plasma treatment for a-IGZO TFTs was discussed in this study. For the untreated a-IGZO TFTs, the transfer curve exhibits an apparent subthreshold current stretch-out phenomenon at 400 K. The stretch-out phenomenon becomes serious with increasing temperatures. The devices after N_2O-plasma treatment exhibit superior electrical properties. Comparing with the untreated devices, the N_2O-plasma treated device can significantly suppress the temperature-dependent subthreshold leakage current stretch-out phenomenon of a-IGZO TFTs. The apparent hysteresis phenomenon for the untreated devices can be attributed to the extra trap states generated during the deposition of SiO_2 passivation layer by PECVD, but these trap states did not appear in the N_2O-plasma treated devices. Moreover, the hysteresis phenomenon was suppressed at 450 K. The stability of transfer curve in hysteresis loops indicates that the interface states reduced significantly after N_2O plasma treatment.

Acknowledgment

This work was performed at the National Science Council Core Facilities Laboratory for Nano-Science and Nano-Technology in Kaohsiung-Pingtung area and was supported by the National Science Council of the Republic of China under Contract Nos. NSC100-2120-M-110-003, NSC97-2112-M-110-009-MY3 and NSC 99-2221-E-009-121.

References

[1] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, K. Nomura, T. Kamiya, H. Hosono, Appl. Phys. Lett. 89 (2006) 112123.
[2] Y.H. Yang, S.S. Yang, K.S. Chou, IEEE Electron Device Lett. 31 (9) (2010) 969.
[3] A. Suresh, P. Wellenius, V. Baliga, H. Luo, L.M. Lunardu, J.F. Muth, IEEE Electron Device Lett. 31 (4) (2010) 317.
[4] Y. Jeong, C. Bae, D. Kim, K. Song, K. Woo, H. Shin, G. Cao, J. Moon, ACS Appl. Mater. Interfaces 3 (2) (2010) 611.
[5] C.T. Tsai, T.C. Chang, S.C. Chen, I. Lo, S.W. Tsao, M.C. Hung, J.J. Chang, C.Y. Wu, C.Y. Huang, Appl. Phys. Lett. 96 (2010) 242105.
[6] T.C. Chen, T.C. Chang, C.T. Tsai, T.Y. Hsieh, S.C. Chen, C.S. Lin, M.C. Hung, C.H. Tu, J.J. Chang, P.L. Chen, Appl. Phys. Lett. 97 (2010) 112104.
[7] T.C. Chen, T.C. Chang, T.Y. Hsieh, W.S. Lu, F.Y. Jian, C.T. Tsai, S.Y. Huang, C.S. Lin, Appl. Phys. Lett. 99 (2011) 022104.
[8] S.Y. Huang, T.C. Chang, M.C. Chen, S.C. Chen, C.T. Tsai, M.C. Hung, C.H. Tu, C.H. Chen, J.J. Chang, W.L. Liau, Electrochem. Solid-State Lett. 14 (4) (2011) H177.
[9] Y.C. Chen, T.C. Chang, H.W. Li, S.C. Chen, J. Lu, W.F. Chung, Y.H. Tai, T.Y. Tseng, Appl. Phys. Lett. 96 (2010) 262104.
[10] W.F. Chung, T.C. Chang, H.W. Li, S.C. Chen, Y.C. Chen, T.Y. Tseng, Y.H. Tai, Appl. Phys. Lett. 98 (2011) 152109.
[11] W.F. Chung, T.C. Chang, H.W. Li, C.W. Chen, Y.C. Chen, S.C. Chen, T.Y. Tseng, Y.H. Tai, Electrochem. Solid-State Lett. 14 (3) (2011) H114.
[12] W.F. Chung, T.C. Chang, H.W. Li, S.C. Chen, Y.C. Chen, T.Y. Tseng, Y.H. Tai, Electrochem. Solid-State Lett. 14 (6) (2011) H235.
[13] G.W. Chang, T.C. Chang, Y.E. Syu, T.M. Tsai, K.C. Chang, C.H. Tu, F.Y. Jian, Y.C. Hung, Y.H. Tai, Thin Solid Films 520 (2011) 1608.
[14] P. Kofstad, J. Phys. Chem. Solids 23 (1962) 1571.
[15] P. Bonasewicz, W. Hirschwald, G. Neumann, Phys. Status Solidi 97 (1986) 593.
[16] V. Gavryushin, G. Raciukaitis, D. Juodzbalis, A. Kazlauskas, V. Kubertavicius, J. Cryst. Growth. 138 (1994) 924.
[17] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, S. Kaneko, J. Appl. Phys. 48 (2009) 011301.
[18] J.M. Lee, I.T. Cho, J.H. Lee, H.I. Kwon, Appl. Phys. Lett. 93 (2008) 093504.
[19] A. Suresh, J.F. Muth, Appl. Phys. Lett. 92 (2008) 033502.
[20] S.J. Seo, C.G. Choi, Y.H. Hwang, B.S. Bae, J. Phys. D: Appl. Phys. 42 (2009) 035106.
[21] J.J. Shin, J.S. Lee, C.S. Hwang, S.H.K. Park, W.S. Cheong, M. Ryu, C.W. Byun, J.I. Lee, H.Y. Chu, ETRI J. 31 (2009) 62.
[22] H. Ohara, T. Sasaki, K. Noda, S. Ito, M. Sasaki, Y. Endo, S. Yoshitomi, J. Sakata, T. Serikawa, S. Yamazaki, Jpn. J. Appl. Phys. Lett. 49 (2010) 03CD02.
[23] J. Park, S. Kim, C. Kim, S. Kim, I. Song, H. Yin, K. Kim, S. Lee, K. Hong, J. Lee, J. Jung, E. Lee, K.W. Kwon, Y. Park, Appl. Phys. Lett. 93 (2008) 053505.
[24] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, H. Hosono, Appl. Phys. Lett. 92 (2008) 133512.