Effects of Hot Carrier Induced Interface State Generation in Submicron LDD MOSFET's

Tahui Wang, Chimoon Huang, P. C. Chou, Steve S.-S. Chung, *Member, IEEE,* and Tse-En Chang

***Abstract*— A two-dimensional numerical simulation including a new interface state generation model has been developed to study the performance variation of a LDD MOSFET after a dc voltage stress. The spatial distribution of hot carrier induced interface states is calculated with a breaking silicon-hydrogen bond model. Mobility degradation and reduction of conduction charge due to interface traps are considered. A $0.6\,\mu$m LDD MOSFET was fabricated. The drain current degradation and the substrate current variation after a stress were characterized to compare the simulation. A reduction of the substrate current at $V_g \simeq 0.5V_d$ in a stressed device was observed from both the measurement and the simulation. Our study reveals that the reduction is attributed to a distance between a maximum channel electric field and generated interface states.**

I. Introduction

As the Si MOSFET technology is moving rapidly into deep submicron domain, hot carrier induced phenomena have spurred great research interest because of their important role in device reliability and characterization [1]–[3]. Recently, it has been recognized that a drain current degradation due to interface state generation is a dominant factor in determination of the device lifetime [2], [4]. Extensive studies have been conducted not only on the degradation of device characteristics in the presence of interface states, but also on the physical mechanisms that lie behind the interface state generation [5]–[7]. Among these studies, much effort has been devoted to the experimental characterization of the interface state effects. Numerical analysis of interface state generation and its significance to the device characteristics are rarely reported in the literature.

Currently, the lucky electron model and the electron temperature model are two commonly used methods to simulate hot electron induced degradation in submicron MOSFET's. However, the validity of these two model, which are based on assumptions of either a constant mean free path or a Maxwellian type distribution function, is often questioned especially in the simulation of the degradation mechanisms involving extremely high electron energy. Despite the validity of the basic assumptions, a threshold energy of 8.7 eV has to be used for interface state generation in the electron temperature model to fit experimental data [8]. This value is unreasonably large because the electron affinity in Si is only 4.05 eV [9]. On the other side, the lucky electron model also yields a doubtful position of interface state generation because the model inherently lacks the nonlocal transport nature. Since the device characteristics are very sensitive to the position of interface states, these two models may lead to an erroneous conclusion or interpretation about the effects of the interface state generation. In this work, we developed a more rigorous window Monte Carlo processor in combination with a breaking Si-H bond model [1] to simulate the interface state profile. Our model has been employed in a general-purpose two-dimensional device simulator, Silvaco PISCES-IIB [10]. The reduction of channel conduction charge and the degradation of electron mobility due to interface charge are also taken into account in the simulation.

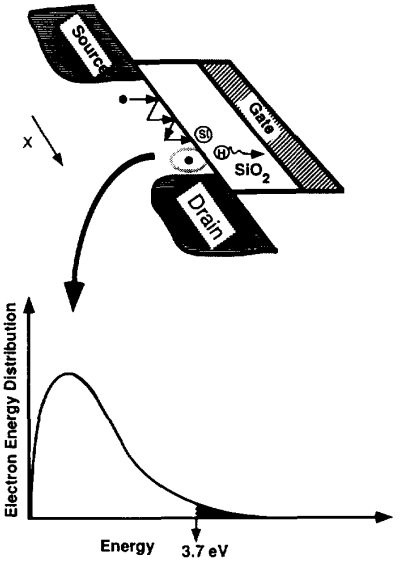

Fig. 1. Illustration of interface state generation. The full circle represents a channel electron. The shaded area under the electron energy distribution represents electrons with energy above the threshold for interface state generation.

A $0.6\,\mu$m LDD MOSFET was fabricated to compare the simulation. The drain and the substrate currents before and after a dc voltage stress were characterized. The importance of the position of the interface states to the substrate current characteristics is evaluated through a comparative analysis of the present model and the lucky electron interface state model.

II. Device Fabrication

A sample n-channel LDD device was fabricated using a polysilicon gate technology. The effective channel length is

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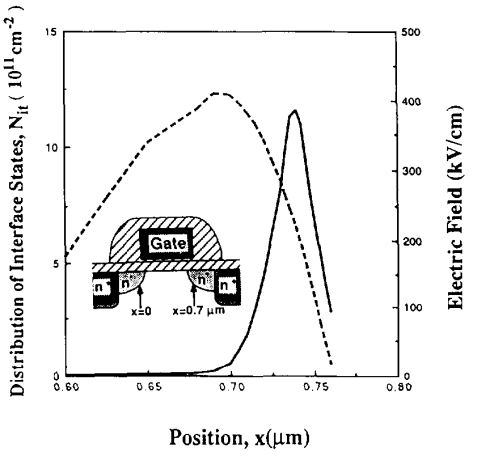


Fig. 2. The solid line shows the simulated distribution of interface states after a stress. The dashed line represents the channel electric field before a stress. Stress voltages are $V_{ds} = 7$ V and $V_{gs} = 3$ V. In the inset of the figure is the device configuration.

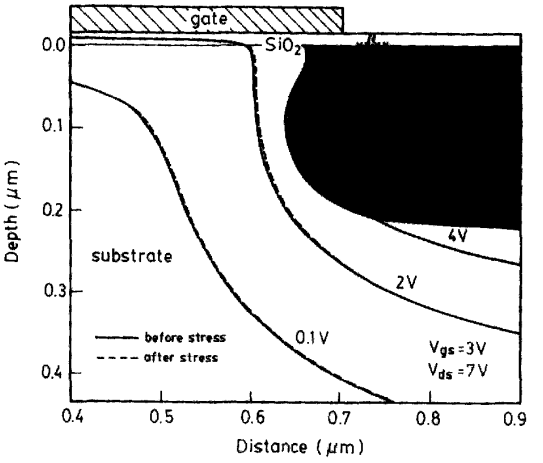


Fig. 3. Two-dimensional equipotential contours before and after a hot carrier stress. The shaded area is the n^- LDD region. Interface states are represented by crosses in the figure.

0.6 μm. The gate oxide thickness, spacer width, and channel width are 140 Å, 0.25 μm and 20 μm, respectively. The threshold voltage adjustment was performed by 70 keV BF_2 ions with a dose of 10^{12} cm^{-2}. The LDD n^- dose and implant energy are 2.0×10^{13} cm^{-2} and 80 keV phosphorus. The overlap between the gate and the n^- region is about 0.05 μm. The 80 keV arsenic was implanted in the source/drain n^+ region at a dose of 3.0×10^{15} cm^{-2}.

The device was stressed at a drain bias of 7 V and a gate bias of 3 V for 10^4 s. Under the stress condition, a roughly maximum hot carrier induced degradation rate was obtained.

III. Numerical Simulation and Physical Models

Analysis of the interface state effects caused by hot carrier injection requires a complicated set of physical models including an interface state generation mechanism, hot carrier injection and nonuniform reduction of conducting electron density and mobility. The physical models employed in the current simulation for the above mechanisms are described in the following.

A. Interface State Generation

The interface state generation is illustrated in Fig. 1 in which channel electrons (represented by full circles) acquire sufficient energy from the large channel field. A fraction of these hot electrons (represented by the shaded area under the energy distribution curve) may have a chance to impinge on the Si/SiO_2 interface and to create interface states. Various theories have been proposed to explain the interface state generation mechanism [1], [5], [11]. Here, we adopt a breaking Si-H bond model developed by C. Hu *et al.* [1]. In their model, it is hot electron injection rather than hot hole injection to be responsible for breaking of the Si-H bond. Subsequently, hydrogen diffusion takes place in the silicon dioxide. Assuming a time-independent hot electron injection current $J_{ch}(x)$, one can derive the interface state generation rate as follows:

$$N_{it}(x,t) = CJ_{ch}(x)t^n + N_{it}(x,0) \tag{1}$$

where x is along the channel direction, $N_{\rm it}(x,0)$ is the initial interface state density, and n is the time-dependence factor of interface state generation. According to the experimental result in [1], n is chosen to be 0.65 in the simulation. C is a fitting parameter to best fit the experimental I-V characteristics. Since $N_{\rm it}(x,0)$ is usually much smaller than the hot electron induced interface state density, it can be neglected in this work.

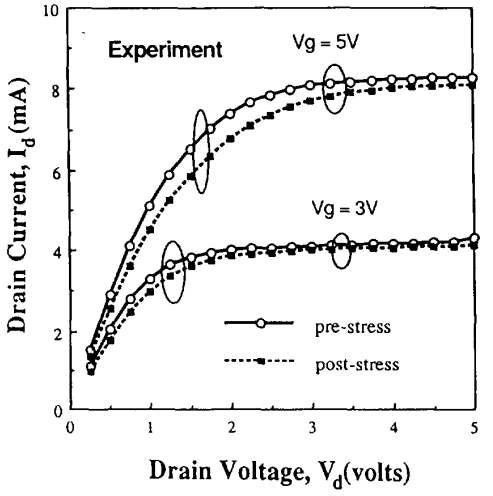
B. Hot Electron Injection Current

The hot electron current density $J_{ch}(x)$ across the interface is expressed by

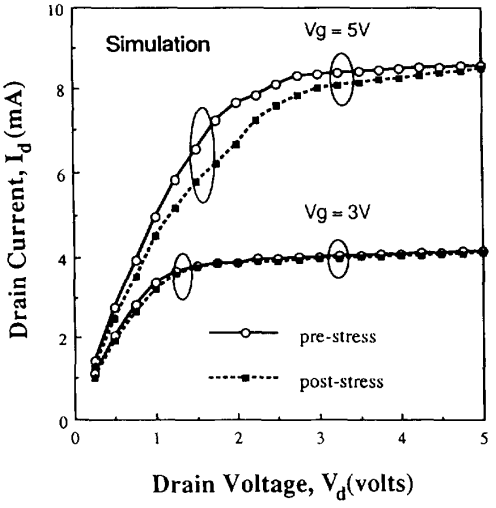
$$J_{ch}(x) = I_d \int_{E_{\rm it}}^{\infty} Pc(x)D(E)f(x,E)dE \tag{2}$$

where $E_{\rm it}(= 3.7$ eV) is the threshold energy for interface state generation. I_d is the drain current. $D(E)$ is the electron density of states of a realistic Si pseudopotential band structure. $P_c(x)$ denotes the probability that electrons impinge on the Si/SiO_2 interface when they travel in the channel and $f(x,E)$ is the electron distribution function. Both $P_c(x)$ and $f(x,E)$ are evaluated from a Monte Carlo simulation with a particular hot electron temperature extraction technique. Details of the simulation of $J_{ch}(x)$ can be found in our previous publication [12].

The simulated spatial distribution of the hot electron induced interface states is shown in Fig. 2 (solid line). The stress voltages are $V_{ds} = 7$ V and $V_{gs} = 3$ V. In the inset of the figure is the device configuration. The generated interface states have a sharp distribution in space and are positioned in the n^- LDD region. The full width at half-maximum (FWHM) of the distribution is about 300 Å, which is consistent with the experimental result obtained from the charge pumping technique [6]. The channel field distribution is also plotted as a reference (dashed line). It should be noted that there exists



(a)



(b)

Fig. 4. (a) Measured I_d versus V_d characteristics before and after a stress, and (b) simulated I_d versus V_d characteristics before and after a stress.

a distance of about 400 Å between the maximum electric field and the peak of the interface state distribution. This distance is required to transform the acquired kinetic energy into thermal energy via phonon scattering. The equipotential contours before and after a stress in Fig. 3 show the interface trap effect on the potential distribution in the device. The position of interface states is indicated by crosses in the figure. It is found that the electric field distribution in the high field region tends to spread more widely after a stress.

C. Mobility Degradation and Conduction Charge Reduction

Because of the presence of acceptor-type interface states, channel electrons may be trapped at the interface to form negative interface charge. As a result, the threshold voltage has a positive shift and the quantity of conduction charge reduces.

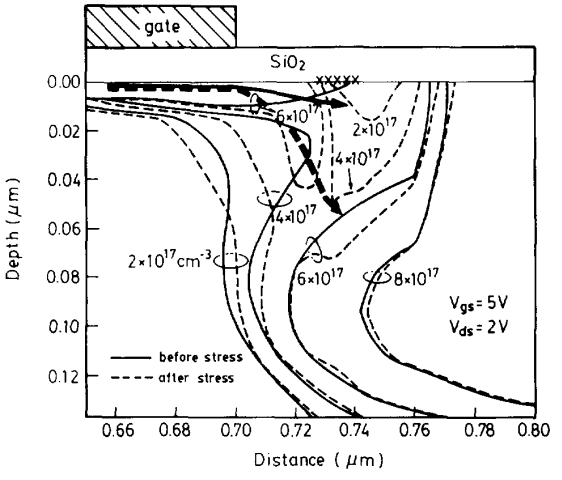


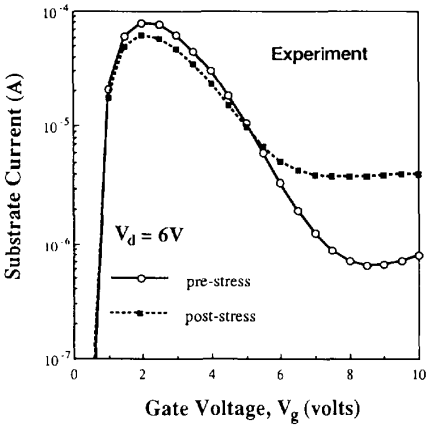
Fig. 5. Simulated two-dimensional distributions of electron concentration before and after a stress. The unit for electron concentration is cm^{-3}. Current flows are shown by the thick solid line (before stress) and the thick dashed line (after stress). The position of interface charge is marked by crosses.

The amount of charge trapped at the interface depends on the position of the quasi-Fermi level with respect to the band edge.

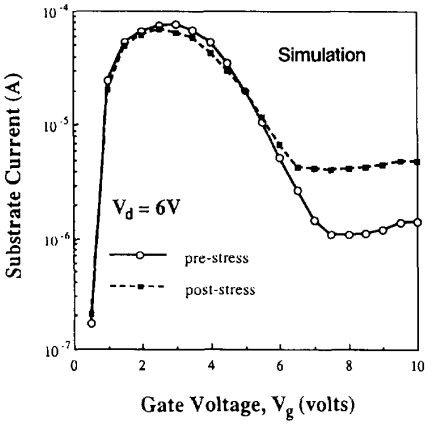
In addition, an empirical mobility degradation formula [13] arising from Coulomb scattering due to interface charge is incorporated in the two-dimensional device simulation. Now, once interface charge is calculated, its influence on the reduction of conduction charge and the mobility degradation can be immediately evaluated.

IV. Result and Discussion

The experimental and simulated drain currents before and after the hot electron stress are shown in Fig. 4(a) and Fig. 4(b). Good agreement between experiment and simulation has been achieved with a maximum interface state density of $1.2 \times 10^{12}/cm^2$ in the simulation. The drain current degradation in the saturation region is much smaller than in the linear region. The reason is that a channel depletion exists in the n^- region, where the generated interface states are located, due to a large drain voltage in the saturation region. The low electron quasi Fermi level in the depletion region results in minimal electron occupation of interface states. Thus the effects of mobility degradation and conduction charge reduction are smaller in the saturation region and so is the drain current degradation. It should be pointed out that no oxide charge incurred threshold voltage shift is observed from the drain current characteristics. In the linear region, the amount of trapped interface charge becomes significant. An appreciable drain current degradation appears. The degradation can be well explained by Fig. 5 where the two-dimensional distributions of electron concentration with a current flow before and after a stress are plotted. Apparently, interface charge (marked by crosses in the figure) results in a decrease of electron concentration underneath and accordingly the current flows deeper in the interface state region. A drop in the slope of the stressed $I_d - V_d$ characteristics actually reflects the interface state effects.



(a)



(b)

Fig. 6. (a) Measured substrate current before and after a stress, and (b) simulated substrate current before and after a stress.

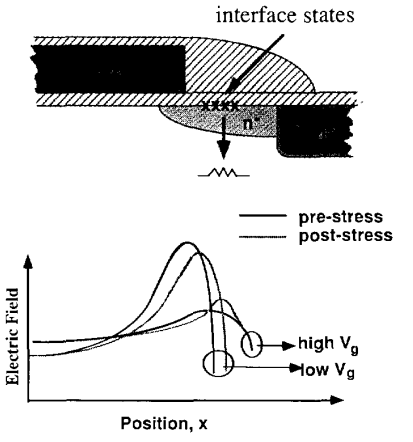


Fig. 7. Schematic representation of the variation of the channel electric field due to interface states.

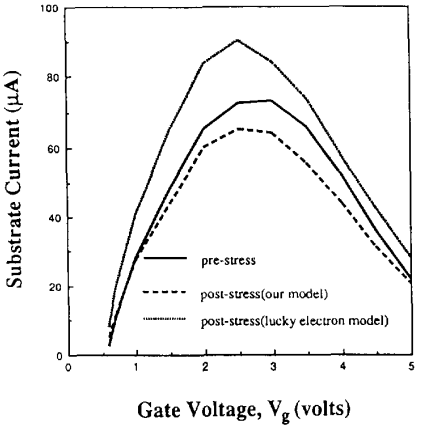


Fig. 8. The calculated substrate currents from our model and from the lucky electron model. The solid line represents the substrate current before a stress.

The measured and simulated substrate currents at a drain bias of 6 V are presented in Fig. 6(a) and Fig. 6(b). Except for a small deviation at a large gate bias caused by an overestimate of the impact ionization rate in a Monte Carlo model, the simulated substrate current is quite consistent with the experimental result. Both the simulation and the measurement show a reduction of the substrate current at a low gate bias (for example, $V_g = 3$ V) and an enhancement at a high gate bias (for example, $V_g = 6$ V) after the stress. In order to explain the variation of the substrate current, the electric field distributions at a low gate bias and at a high gate bias are depicted in Fig. 7. At a low gate bias, the interface states are about a few hundred Å behind the maximum electric field as mentioned previously. Since the interface state generation can be treated as an increase of the channel resistance, a larger voltage drop develops in the interface state region to compensate for the increased channel resistance. Consequently, the maximum electric field, which is outside the interface state region, declines after the stress and so does the substrate current. As the gate bias increases, the maximum channel field shifts toward the interface state region. While the maximum field and the interface states occupy almost the same region, a larger voltage drop in the interface state region implies an increase of the maximum field. Thus the substrate current shows an enhancement instead at a larger gate bias.

In order to further evaluate the significance of the interface state position to the substrate current, we make a comparison between the present model and the lucky electron interface state model. The reader should be reminded that the interface state generation rate in the lucky electron model is a function of only a channel electric field. The peak of the interface state density occurs at the same position as the maximum electric field. For the purpose of a comparison, the same density of interface states is used in both models. The calculated substrate currents versus gate bias are shown in Fig. 8. As expected, the lucky electron model predicts a higher maximum electric field and an enhancement of the substrate current. This result is obviously opposite to the measured characteristics due to the small deviation in the location of the interface states.

V. Conclusion

A combined Monte Carlo method and the breaking Si-H bond model has been developed to simulate the effects of interface state generation. Good agreement between experiment and simulation is achieved. The implications of a distance between the maximum electric field and the hot electron induced interface states have been discussed.

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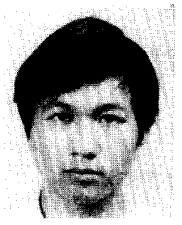

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