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Investigation of gate-bias stress and hot-carrier stress-induced instability of InGaZnO thin-film transistors under different environments

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ABSTRACT

This paper investigates the temperature and ambiance effects on various reliability issues for InGaZnO thin film transistors with an organic passivation layer. Hot-carrier stress and gate-bias stress are carried out under different environmental temperatures and ambient gases. The device exhibits relatively good stability under room temperture, whereas high temperature enhances degradation. Futhermore, different degradation behaviors after gate-bias stress in atmosphere and in vacuum can be attributed to gas adsorption/desorption-induced instability. Moreover, capacitance-voltage measurement techinique is utilized to analyze the degradation mechanism and to extract the density of state (DOS). The result reveals that the threshold voltage shift after both hot-carrier and gate-bias stress originates from the charge-trapping effect at the interface of gate insulator and active layer, with the extra trap states generated during stress responsible for C-V curve distortion. In addition, the asymmetric degradation behavior of gate-to-drain capacitance (Cgd) and gate-to-source capacitance (Cgs) indicates that trap states are generated near the drain side.

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1. Introduction

Metal-oxide thin-film transistors (TFTs) such as ZnO and amorphous InGaZnO (*a*-IGZO) have attracted much attention in industry for applications in next generation displays owing to their high mobility, superior uniformity, good transparency to visible light and low process temperature [1–4]. For the OLED application, the IGZO TFT is used as a driving device and is operated under gate bias and drain bias simultaneously. In previous studies, the instability of IGZO TFT under gate bias stress has been attributed to the charge-trapping in the gate insulator/IGZO interface or gate bias-induced gas adsorption/desorption near the back channel of IGZO [5–8]. However, further analysis of other considerations such as drain bias and temperature effect are required for better understanding of the degradation behaviors in practical operation conditions. Therefore, in this paper, gate bias stress and hot-carrier stress are carried out in various gas environments and at different temperatures to investigate the effect of environmental conditions on stress-induced instability of IGZO TFTs. Since capacitance-voltage (C-V) measurement is beneficial to analyze the trap-state generation, it is utilized to inspect the degradation behavior and extract density-of-state (DOS).

2. Experiment

Fig. 1 shows the cross-section of TFT used in this work. The n-type a-IGZO TFTs were prepared with a bottom gate and back-channel-etching (BCE) structure. The gate metal and insulator layer were Ti/Al/Ti and SiN_x, respectively. An a-IGZO active layer was deposited by a DC-type sputtering system with a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 in atomic ratio and then patterned. The S/D electrode Mo/Al/Ti was formed and then patterned. No post-annealing was performed. Finally, the device was coated with non-acryl-based photosensitive organic material as a passivation layer. In this work, the I-V and C-V measurements were performed by an Agilent B1500A semiconductor device analyzer. Furthermore, the vacuum measurement environment of 1×10^{-3} torr atmosphere pressure was controlled by a vacuum pump. All measurements in this work were carried out in a darkened environment.

3. Result and Discussion

Fig. 1(a) shows the evolution of I_d-V_g characteristic transfer curves after positive gate bias stress performed with $V_g = 15$ V and

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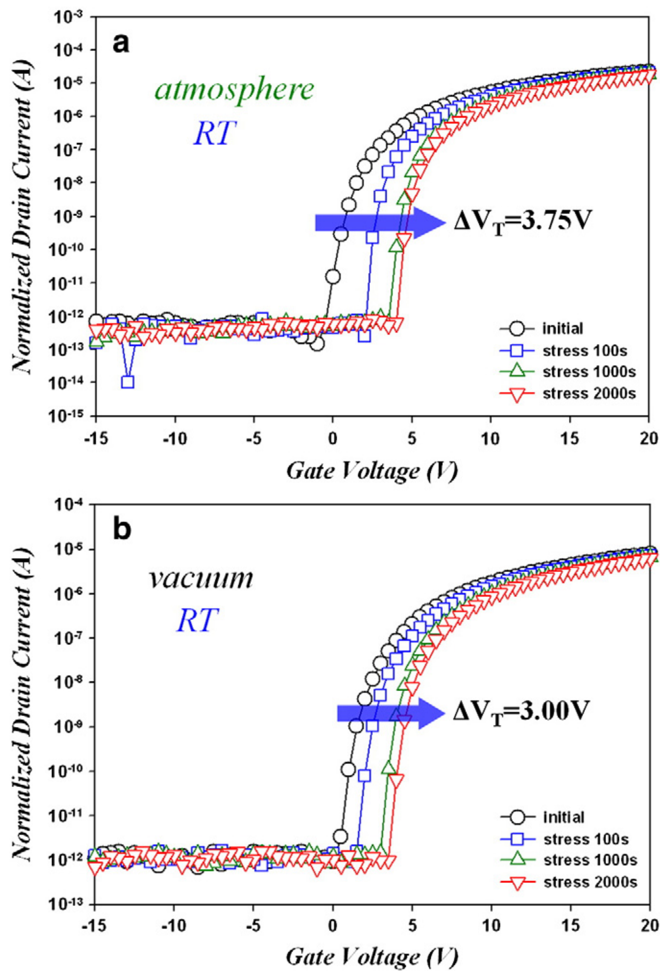

Fig. 1. Evolution of I_d-V_g characteristic transfer curves after positive gate bias stress performed with $V_g = 15$ V and $V_s = V_d = 0$ V in (a) atmosphere and (b) vacuum at room temperature for 2000 seconds.

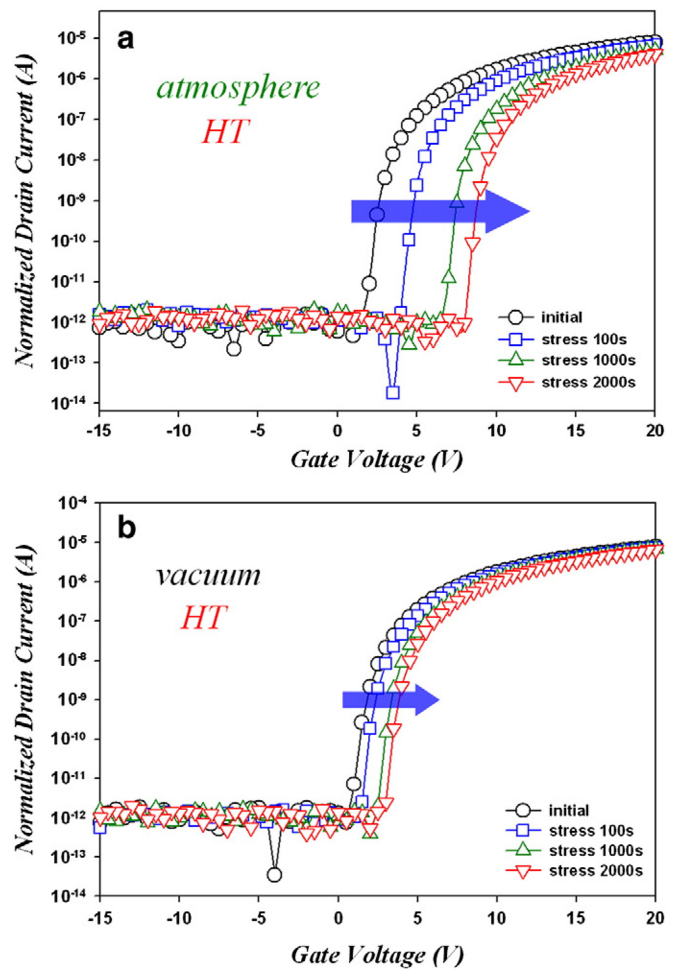

Fig. 2. Evolution of I_d-V_g characteristic transfer curves after positive gate bias stress performed with $V_g = 15$ V and $V_s = V_d = 0$ V in (a) atmosphere and (b) vacuum at 50 °C for 2000 seconds.

$V_s = V_d = 0$ V in atmosphere and at room temperature for 2000 seconds. The more apparent V_T shift of 3.75 V after stress performed in atmosphere than that of 3.00 V in vacuum shown in Fig. 1(b) suggests the degradation results from not only charge-trapping effect but also ambient gas adsorption/desorption [5–8]. Since gas adsorption/desorption will not occur in a vacuum environment, the V_T shift is dominated by charge-trapping effect. On the other hand, both the charge-trapping effect and gas adsorption/desorption can influence V_T instability in atmosphere. Moreover, the environment-dependent V_T shift difference is more obvious at high temperature, as shown in Fig. 2. This phenomenon indicates that gate bias-induced gas adsorption/desorption is enhanced at high temperature. As previous studies have reported, the positive V_T shift under positive gate bias can be attributed to oxygen adsorption near the back channel [5,6]. Therefore, the effects of charge-trapping and oxygen adsorption can be separated from different V_T shifts after stress in different environments, and more severe V_T instability after stress performed at high temperature demonstrates oxygen adsorption is enhanced by heat.

In contrast, device characteristics are much more stable under negative bias stress when compared to positive gate bias stress even in atmosphere and at high temperature (I-V curves not shown here). I-V curves are almost unchanged after stress carried out in vacuum, which means hole-trapping is insignificant under such conditions, since IGZO is an n-type semiconductor material. Although the device's characteristic degradation is not apparent under negative bias stress observed in I-V measurement, distortion of C-V curves, shown in Fig. 3, reveals that trap states are generated during the stress. Fig. 3 shows the C-V curves under negative bias stress at room temperature in vacuum and in atmosphere. In vacuum, neither hole-trapping nor gas adsorption occurs, thus C-V curves are not altered after stress. Nevertheless, the C-V curve distortion showing increased capacitance at the off-state after negative gate bias stress is carried out in atmosphere indicates that trap states are generated and affect the device characteristics at off-state. In a previous report, water adsorbed at the back channel of IGZO active layer can act as an electron donor and trap state as well [6]. Water molecules donate electrons and increase the electron concentration in the IGZO layer, results in a V_T decrease. In addition, trap states induced by water adsorption can lead to C-V curve distortion. Therefore, the negative shift and distortion of C-V curve at the off-state can be attributed to water adsorption induced by negative gate bias stress.

Further analysis of other considerations, such as drain bias, are required for a better understanding of the degradation behavior in practical operation conditions. Therefore, the hot-carrier effect is investigated with stress carried out with $V_g = V_d = 15$ V at different temperatures in vacuum. As shown in the inset of Fig. 4(a), the observed I-V curve positively shifts after hot-carrier stress. In addition to Cgc (gate-to-channel capacitance), Cgd (gate-to-drain capacitance) and Cgs (gate-to-source capacitance) are measured

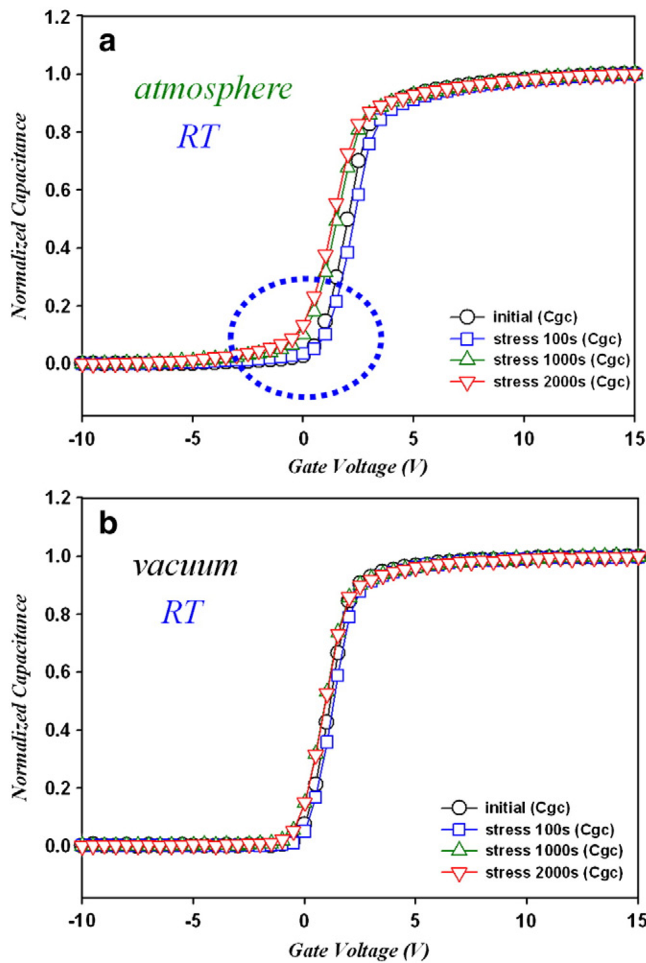

Fig. 3. C-V curves after negative gate bias stress with $V_g = -15$ V and $V_s = V_d = 0$ V in (a) atmosphere and (b) vacuum at room temperature.

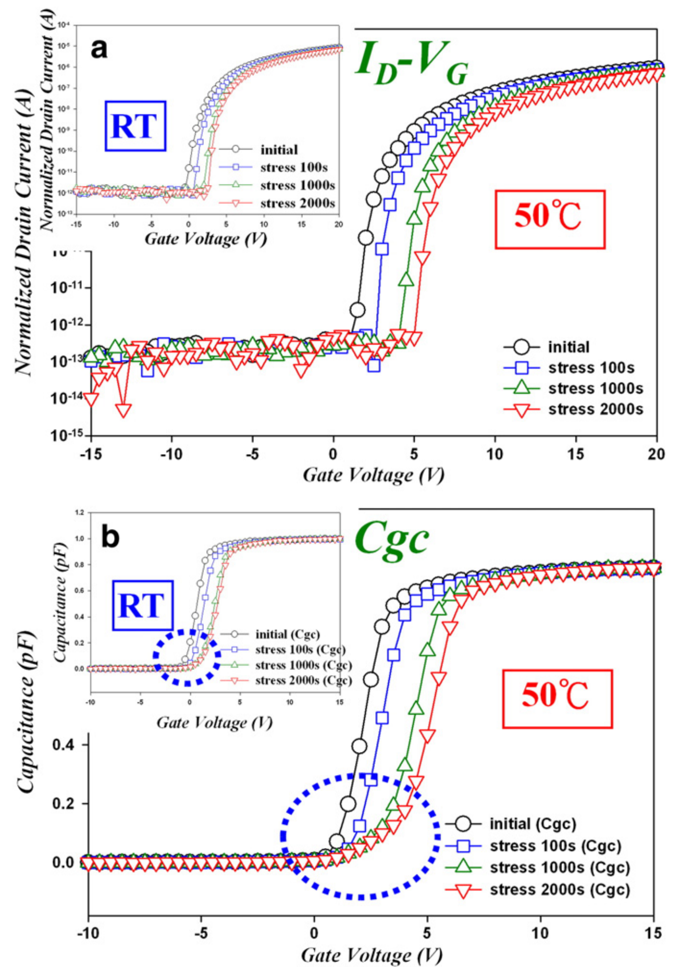

Fig. 4. (a) I_D-V_G characteristic transfer curves and (b) Cgc curves after hot-carrier stress performed with $V_g = V_d = 15$ V and $V_S = 0$ V in vacuum at 50 °C; insets show the corresponding characteristic curves after identical stress performed at room temperature.

as well to locate the degradation area, shown in Figs. 4(b) and 5. In Cgc, the parallel positive shift indicates the V_T shift of the I-V curve is dominated by electron-trapping at the IGZO/gate insulator interface, and the slight distortion at off-state suggests trap states are generated under hot-carrier stress. Moreover, from the result of Cgd and Cgs, it is observed that the alteration of Cgd is like Cgc, but Cgs monotonically shifts toward positive direction without distortion after stress. This phenomenon demonstrates that degradation is asymmetric under hot-carrier stress operation, and trap states are generated mainly near the drain side, causing Cgd distortion at the off-state. Thus, the degradation behavior of Cgs curve is dominated by electron-trapping-induced parallel shift without distortion.

Furthermore, the characteristics after hot-carrier stress is performed at 50 °C, shown in Figs. 4 and 5, exhibit an enhanced degradation compared to that at room temperature, indicating the hot-carrier effect is more pronounced at high temperature. Both V_T shift and distortion are enhanced under high temperature hot-carrier stress, demonstrating the electron-trapping effect and trap state generation are both heat-accelerated at high temperature. In addition, to profile the trap state distribution with regard to energy, DOS (density of state) is extracted from C-V characteristic curve [9], shown in Fig. 6. After hot-carrier stress, deep states are increased, and are responsible for C-V distortion at the off-state.

4. Conclusion

Reliabilities of gate-bias induced instability and hot-carrier effects are investigated under various environmental conditions for InGaZnO thin-film transistors. Different levels of V_T shift after gate bias stress carried out in vacuum and atmosphere demonstrate that not only electron-trapping but also oxygen-adsorption effect can influence the device instability in atmosphere. Temperature-enhanced degradation under gate bias stress suggests both electron-trapping and gas-adsorption are heat activated. In negative gate bias stress, even though degradation is not observed in transfer curves, distortions at the off-state of C-V curves take place. Hot-carrier effect leads to a positive shift and an asymmetric trap-state generation. Trap-states are mainly generated near the drain side, and the DOS distribution extracted from C-V curve indicates those traps are located at a deep level in the energy gap and are responsible for C-V curve distortion.

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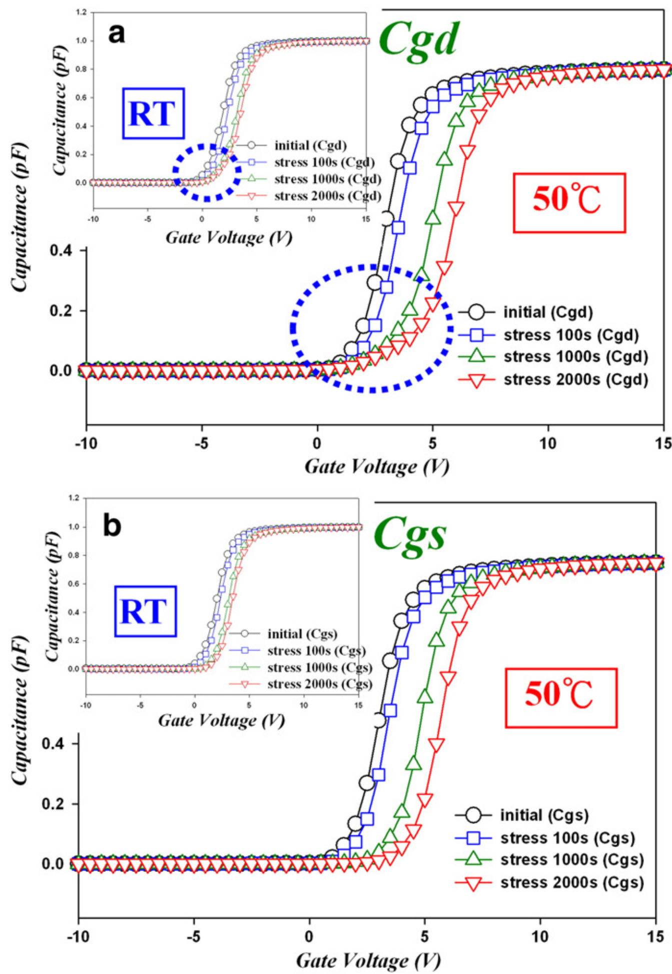

Fig. 5. (a) Cgd and (b) Cgs curves after hot-carrier stress in vacuum at 50 °C; insets show the corresponding characteristic curves after identical stress performed at room temperature.

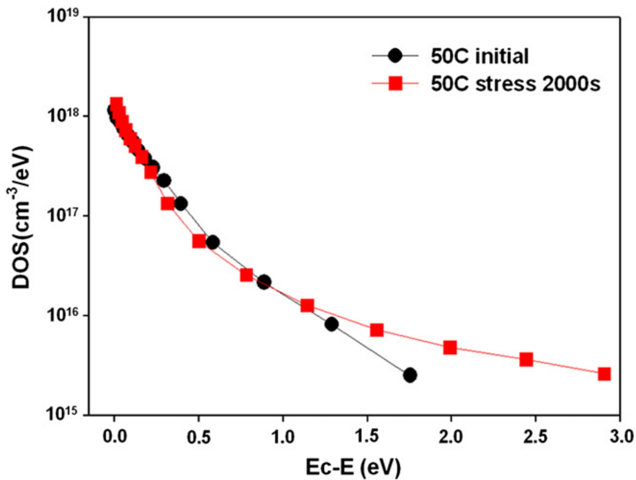

Fig. 6. DOS distribution with regard to energy at initial state and after hot-carrier stress at 50 °C.

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