A Novel Pixel Design for AM-OLED Displays Using Nanocrystalline Silicon TFTs

Chen-Wei Lin, Mango C.-T. Chao, *Member, IEEE*, and Yen-Shih Huang

***Abstract*—This paper presents a novel pixel design for active matrix organic light emitting diode (AM-OLED) displays using nanocrystalline silicon thin-film transistors (TFTs). The proposed pixel design can effectively reduce the variation of its stored display data caused by the leakage current of nanocrystalline silicon TFTs, which can in turn increase the contrast resolution of AM-OLED displays. With a proper setting of its capacitors, the proposed pixel design can achieve a 5.55× reduction on its display-data variation while requiring only a 1.15× write time when compared to the typical pixel design. The aperture ratio resulting from the layout of the proposed pixel design can also be maintained above 40%, which satisfies the specification of most AM-OLED displays. A series of simulations as well as measurement results are provided to validate the effectiveness of the proposed pixel design.**

***Index Terms*—Active Matrix Organic Light Emitting Diode (AM-OLED), coupling effect, microcrystalline thin-film transistor (TFT), nanocrystalline TFT.**

I. Introduction

DURING the past few years, major display manufacturers have put a lot research efforts into the area of active matrix organic light emitting diode (AM-OLED) displays, which use self-light-emitting devices, require no backlight elements, and in turn are lighter, thinner, and less power-consumed compared to the current display mainstream, active matrix liquid crystal display (AM-LCD displays) [1], [2]. AM-OLED display can also provide faster response time, wider viewing angle, and better front-of-screen (FOS) quality, and hence is considered as the best candidate for next-generation displays [1], [2]. In order to build a robust backplane which can reliably control OLED's current and thus its lightness, a stable and high-quality thin-film transistor (TFT) technology is required. However, the available TFT technologies in current industry are not yet cost-effective or stable enough, which has been the biggest barrier for developing quality AM-OLED displays today [1], [3].

Table I compares the three major prospects of the TFT technology used for building the backplane of AM-OLED displays, which are: 1) amorphous silicon (α-Si) TFT; 2) polycrystalline silicon (poly-Si) TFT; and 3) nanocrystalline silicon (nc-Si) TFT (or microcrystalline silicon TFT). The first prospect α-Si TFT, which is currently used for building the backplane of AM-LCD displays, has the advantages of low leakage, low process temperature, better electric uniformity, and easy deposition, resulting a relatively low manufacturing cost [1], [2], [4]. However, α-Si TFT suffers from its low mobility, which may result in a low aperture ratio and in turn low illumination efficiency. α-Si TFT also suffers from its large threshold-voltage shift over time, which significantly reduces the reliability of AM-OLED displays since a large current needs to pass through the TFTs which drive the OLEDs. Such an OLED-driving TFT is not required in AM-LCD displays, whose light source comes from a stable backlight element.

TABLE I
Comparison of Silicon-Based TFTs

Materials	α-Si	poly-Si	nc-Si
Effective Mobility	Low	High	Medium
Reliability	Poor	Excellent	Good
Process Temperature	$< 300°C$	$450°C$	$< 300°C$
Electric Uniformity	Excellent	Poor	Good
Leakage Current	Low	High	Medium

In contrast with α-Si TFT, the second prospect poly-Si TFT, which is also a mature technology in current industry, can provide stable threshold voltage over time and high mobility for driving OLED due to its larger silicon grain size [1], [2]. However, by using the technique of excimer laser annealing for crystallization, poly-Si TFT has the disadvantages of low electric uniformity, which limits the application of poly-Si TFT only on small-size panels [1], [2]. Also, the overall manufacturing cost of poly-Si TFT is high because of its high process complexity, the required laser equipments, and its high process temperature.

The third prospect nc-Si TFT, whose silicon grain size is between the other two TFT technologies, can overcome the drawbacks of low mobility and poor reliability when compared to α-Si TFT, and at the same time overcome the drawbacks of high manufacturing cost and poor electric uniformity when compared to poly-Si TFT. As in [1], [4]–[6], nc-Si TFT can be manufactured by using the conventional 13.56 MHz plasma-enhanced chemical vapor deposition (PECVD), whose manufacturing infrastructures are already well established in current industry for α-Si TFT technologies. Furthermore, if the nc-Si TFT is constructed by using the *bottom-gate* structure [1], [3] instead of the *top-gate* structure [5], [6], the process flow can match the one used for the current manufacturing of AM-LCD displays. In this condition, the technology of nc-Si TFT can reuse the current production lines of AM-LCD displays and, thus, can be brought to mass production sooner and more economically.

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Overall, the nc-Si TFT combines several advantages of both poly-Si and α-Si TFTs, is cost-effective in manufacturing, and hence emerges as a promising TFT technology for AM-OLED displays. However, the biggest barrier preventing the nc-Si TFT from production is its high drain-source turn-off current (leakage current). When the typical pixel design is used, this high leakage current may result in either a low contrast resolution or the lose of a stored display data before an image frame is refreshed. A high leakage current is a common drawback of using the PECVD [1], [5] and may become worse when the bottom-gate structure is used [1], [3], [5]. Several previous works attempted to reduce this leakage current from the aspects of changing TFT's structures [5], [6], material [1], or deposition mechanisms [7], but yet the current progress along this research line is still not sufficient enough to reach the standard for production.

In this paper, we attempt to push the use of nc-Si TFTs into production by proposing a novel pixel design of AM-OLED displays. The proposed pixel design can effectively reduce the degree of display-data variation caused by nc-Si TFT's leakage. Also, its write-time overhead and area overhead can be properly limited by the choice of its capacitance setting and layout techniques, respectively. The analysis and simulation for both display-data variation and data write time will then be provided. An optimal configuration of the proposed pixel design can be obtained through proper simulation. The measurement result based on a nc-Si TFT technology developed by ITRI [8] further confirms our analysis and simulation for the proposed pixel design. In general, the contrast resolution saved by the proposed pixel design can be up to more 2 digital bits, which significantly ease the pressure of finding a new low-leakage material or deposition mechanism, and in turn speed up the production of AM-OLED displays using nc-Si TFTs.

II. Background of AM-OLED Displays and the Typical Pixel Design

Unlike AM-LCD panels, which need a backlight element to be its light source, AM-OLED panels use the OLED thin film embedded in its multilayer structure for illumination and hence requires no backlight element. Fig. 1 illustrates the typical multilayer structure used for an AM-OLED panel, which consists of the following five layers listed from bottom to top: 1) substrate layer; 2) control-circuit layer; 3) illuminant layer; 4) cathode layer; and 5) cover layer. The substrate layer and cover layer are usually made by glass, which allows the light passing through, isolates the other inner layers from water and oxygen, and hence prevents the aging of its organic material as well as the change of TFT's electrical characteristics. The control-circuits layer utilizes TFTs and capacitors to form a pixel array, which can control the degree of illumination of each OLED, which is evaporated on the illuminant layer accordingly. The cathode layer is made by metal Al and used as the ground signal connected to OLED.

As a result of the multilayer structure shown in Fig. 1, the panel's images are observed from the bottom of the panel since the layer on top of the illuminant layer (made by aluminum) is opaque. Thus, the light generated by the OLEDs needs to pass through the control-circuit layer, and which in turn needs to provide a transparent region on each pixel design as a channel for

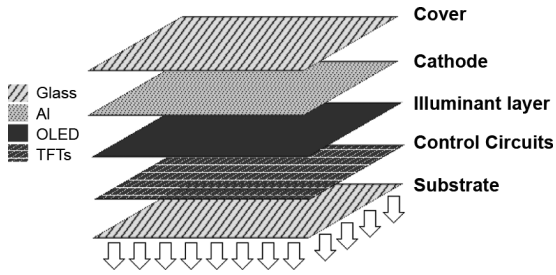

Fig. 1. Typical multilayer structure of an AM-OLED panel.

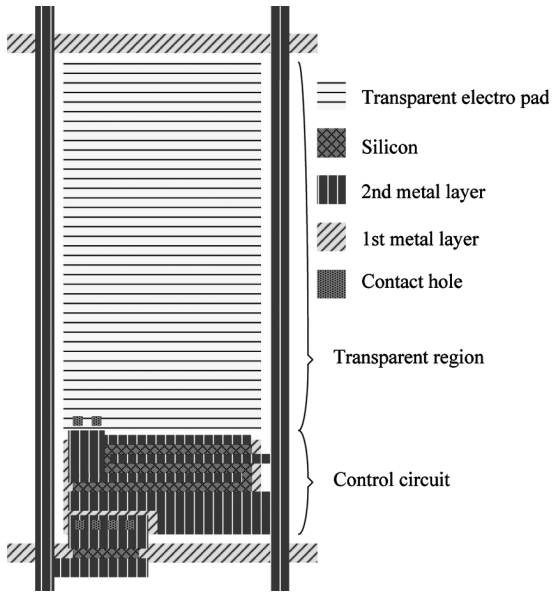

Fig. 2. Layout of a typical pixel design and its resulting transparent region.

light. The transparent region is made by a transparent electrical conductor, indium tin oxide (ITO), and is used as an electropad connecting to the OLED. Fig. 2 shows a typical pixel layout with the corresponding transparent region. Based on the OLED technologies used in our design, the ratio of the transparent region in a pixel design (defined as *aperture ratio*) have to be more than 40% of the pixel's total area to provide sufficient luminance under the constraint of current density.

Following is the calculation of the minimum aperture ratio. First, we use (1) to calculate the required current passing through the OLED (denoted as I_{OLED}) such that the desired luminance of a panel (denoted as Lum) can be provided. In (1), the luminance of the panel (Lum) is set to 200 nits $(1\ \mathrm{nit}\ =\ 1\ \mathrm{Cd/m^2})$, which accords to the specification of a quality AM-OLED panel [9]. The pixel area (denoted as $Area$) in a 4.1" QVGA AM-OLED panel is 86.78 $\times$260.35 $\mu\mathrm{m}^2$. The luminance efficiency (denoted as LE) of the OLED in use is set to 4 Cd/A, which is a relatively weak OLED in current OLED market. The panel transmittance (denoted as PT) is set to 0.8, which is determined by the transmittance of the transparent electropad (ITO) and the substrate (glass). By solving (1) with the above parameters, the required current (I_{OLED}) is equal to 1.4 μA

$$\mathrm{Lum} \cdot \mathrm{Area} = I_{\mathrm{OLED}} \cdot LE \cdot PT. \tag{1}$$

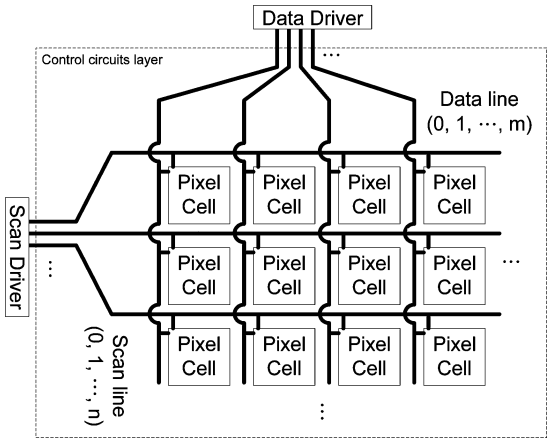

Fig. 3. Overview of a pixel array.

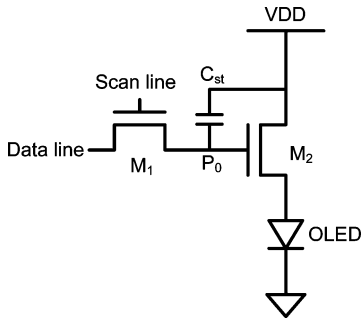

Fig. 4. Schematic of the typical pixel design.

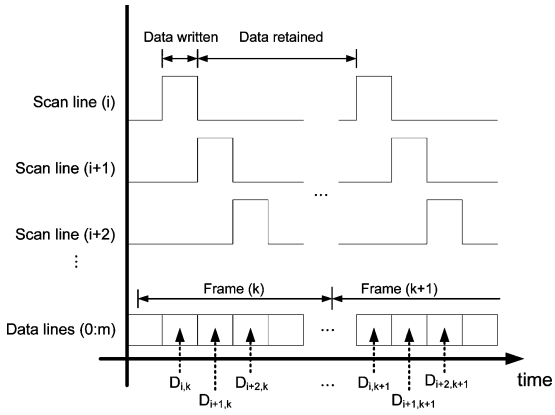

Fig. 5. Exemplary timing diagram of $Scan\_line$ and $Data\_line$ for an AM-OLED pixel array.

The aperture ratio of a pixel design (denoted as AR) determines the area of the transparent electropad, i.e., the area of the evaporated OLED. The area of the evaporated OLED further determines the current density of the OLED [10], [11]. An excessive current density may significantly degrade the reliability and lifetime of the OLED. In the following calculation, we set the upper bound of the current density (denoted as CDen) to 20 $\mathrm{mA/cm^2}$ as suggested by [10], [11]. By solving (2), the aperture ratio needs to be larger than 31%. Thus, setting the minimum aperture ratio to 40% is actually a high standard for current panels and can already cover a significant range of design margins

$$\frac{I_{\mathrm{OLED}}}{\mathrm{Area} \cdot AR} \leq \mathrm{CDen}. \tag{2}$$

Fig. 3 shows an overview of an $m \times n$ AM-OLED pixel array locating on the control-circuit layer, where the lightness of a pixel is controlled by the data stored in a pixel cell. In this pixel array, a row of pixel cells is selected by the signal $Scan\_line$. The data of pixel cells on a selected row is fed through the signal $Data\_line$. The signal $Scan\_line$ and $Data\_line$ are controlled by an outside driving IC through a runner, respectively. Such an AM-OLED pixel array is similar to a DRAM array except the following differences: 1) the data stored in each AM-OLED pixel cell is an analog signal rather than a digital signal; 2) an AM-OLED array only performs write operations while a DRAM array performs both read and write operations; and 3) the write operation of an AM-OLED pixel array is performed in a row basis serially and ceaselessly while DRAM cells can be accessed randomly.

Fig. 4 illustrates the typical pixel design used in current AM-OLED displays, which consists of two TFTs, one capacitor, and one OLED. As shown in Fig. 4, the lightness of an OLED is determined by the current flowing through the TFT M_2, which is further controlled by the display data stored in the capacitor C_{st}. The TFT M_1 functions as a switch for determining whether the data from $Data\_line$ should be written in the capacitor C_{st} according to signal of $Scan\_line$. With this pixel design, the electric signal stored in the capacitor C_{st} can be transformed into an optical signal displaying on an OLED.

Fig. 5 shows an exemplary timing diagram of $Scan\_line$ and $Data\_line$ on an AM-OLED pixel array. The signals on $Scan\_line$ are sequential and non-overlapped pulses. The signal on $Data\_line$ represents the image data to be displayed on a pixel row and is notated by $D_{i,k}$, where i and k represent the index of the corresponding pixel row and time frame, respectively. When $Scan\_line$ on a row is turned on, the corresponding pixel cells enter the "data-written" phase and their display data is written in. When $Scan\_line$ on the row is turned off, the corresponding pixel cells enter the "data-retained" phase and the pixel cells need to maintain the stored data until the next write operation on the current row. Thus, the time of an image frame is equal to the total time of a data-written phase and a data-retained phase, which is actually equal to the total number of rows times the time of a data-written phase.

Therefore, the quality of a proposed pixel design can be determined by its required time of writing in a display data and its capability of retaining a display data. The time of an image frame is fixed and usually set to 16.7 ms (reciprocal of 60 Hz) according to the sensitivity of human's vision. Thus, the time of a data-written phase determines the number of pixel rows to be supported in a display, i.e., the size of the display. The capability of retaining a display data affects the degree of display-data variation during the data-retained phase, and in turn determines the contrast resolution represented by its least significant bit. Also, the proposed pixel design has to be subject to the pixel-area limit of a display panel and the required aperture ratio.

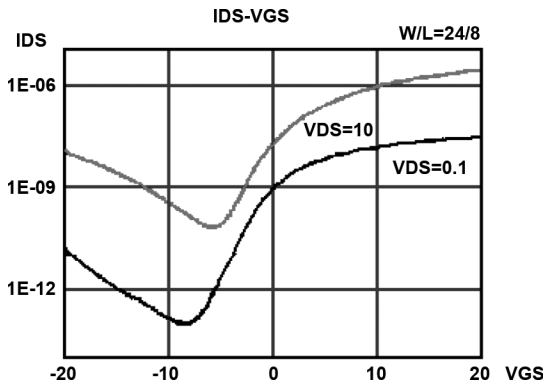

Fig. 6. I_{ds} versus V_{gs} of a nc-Si TFT [1].

III. Challenge of Using nc-Si TFTs in AM-OLED Displays

A. Problem: High Leakage Current of nc-Si TFTs

Despite of providing several advantages on its mobility, reliability, and manufacturing cost, the nc-Si TFTs suffers from its large turn-off leakage current [1], [3], [5], [12], which does not exist for α-Si TFTs or can be solved by using lightly-doped-drain (LDD) technique for low-temperature-polysilicon TFTs, which is a poly-Si TFT technology [2]. Fig. 6 shows the drain-source current I_{ds} of a nc-Si TFT versus gate-source voltage V_{gs} in condition of different drain-source voltage V_{ds} [1]. As Fig. 6 shows, I_{ds} of a nc-Si TFT may significantly increase when V_{gs} is smaller than a certain amount. This characteristic of large turn-off leakage current (I_{off}) results in that the switch TFT M_1 may not be able to cut off the connection between P_0 and $Data\_line$ (as shown in Fig. 4) during the data-retained phase. Thus, the data stored on C_{st} would be interfered by the data at $Data\_line$ writing into the other pixel cells in the same column, which may result in significant display-data variation during the data-retained phase.

B. Straightforward Solutions

For the engineers who cannot acquire better TFT devices at present, the following two straightforward solutions can be applied to the typical pixel design to minimize the display-data variation resulting from nc-Si TFT's large leakage current. The first solution is to increase the refresh rate. The second one is to increase the size of the capacitor C_{st} or the channel length of the TFT M_1.

1) Higher Refresh Rate: The objective of increasing refresh rate is to reduce the time of the data-retained phase such that the variation of the stored voltage of C_{st} can also be reduced before the new display data is written in. However, increasing the refresh rate may result in the following three drawbacks. First, increasing the refresh rate needs a stricter specification to both the data-driver IC and the scan-driver IC, which may in turn increase the design efforts and the cost of both driver ICs. Second, increasing the refresh rate requires a higher power consumption of the display, which may prevent the AM-OLED displays from mobile applications. Last and most importantly, the time for writing in display data to a pixel cell needs to be reduced since a frame period is equal to the total number of pixel rows times the time of the data-written phase. Otherwise, the number of affordable pixel rows become smaller. The time of writing in a display data is determined by the mobility and the channel width of the switch TFT M_1. However, increasing the mobility of a TFT may not be always achievable and increasing the channel width of the switch TFT may increase its leakage at the same time, which contradicts with our original objective of using a higher refresh rate.

2) Larger C_{st} or Longer Channel Length of M_1: This circuit-level solution focuses on increasing the RC time constant between C_{st} and M_1, where C and R represent the capacitance of C_{st} and the drain-source resistance of M_1 during the data-retained phase (which is also denoted as $R_{M_1\_off}$). Usually, increasing C_{st} is not preferable because the layout area of C_{st} already occupies a significant portion of the whole pixel design. Doubling the size of C_{st} may significantly decrease the aperture ratio of the pixel design. Also, increasing the size of C_{st} will increase the time of writing in a display data. On the other hand, increasing the channel length of M_1 is more affordable since the original size of M_1 is relatively small. For current typical pixel designs, the channel length of M_1 can be increased by multiple times and its aperture ratio can still be higher than the minimum requirement. Also, increasing the channel length of M_1 will increase the time of writing in a display data as well. Thus, when increasing the channel length of M_1, both aperture ratio and the capability of writing in a display data should be maintained higher than their minimum requirement.

IV. Proposed Pixel Design for Minimizing Display-Data Variation

A. Design Overview and Design Constraints

In this section, we propose a novel pixel design to minimize the display-data variation resulting from the large leakage current of nc-Si TFTs. Fig. 7 shows the schematic of the proposed pixel design, which consists of three TFTs (M_3, M_4, and M_5), three capacitors (C_1, C_2, and C_3), and one OLED. Compared to the typical design shown in Fig. 4, TFT M_5 in the proposed pixel design plays the same role as TFT M_2 in the typical design, which connects a voltage source to the OLED. Instead of using only one capacitor (C_{st}) in the typical pixel design, the proposed pixel design uses three capacitors (C_1, C_2, and C_3) to store the display data. Also, the proposed pixel design utilizes two TFTs (M_3 and M_4) as switches to determines whether the display data can be written in. The voltage at P_2 determines the lightness of the OLED.

The proposed pixel design can effectively minimize the display-data variation by adding an extra TFT in between the stored display data (voltage at P_2) and $Data\_line$ during the data-written phase. Also, the proposed pixel design requires no extra control signal other than $Scan\_line$ and $Data\_line$, and thus can be easily applied to current AM-OLED displays using nc-Si TFTs. However, in order to limit the area overhead and provide an enough aperture ratio, two design constraints need to be followed for the proposed design. First, the total capacitance of C_1, C_2, and C_3 is the same as C_{st}. Second, the size of each TFT used in the proposed design is the same as that used in

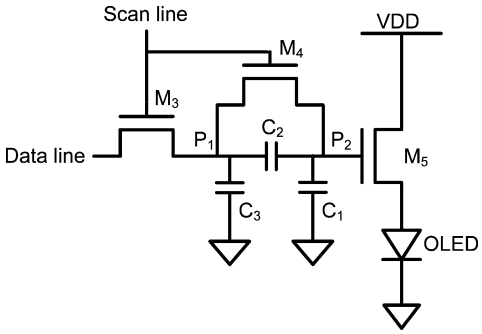

Fig. 7. Schematic of the proposed pixel design.

the typical design. With these two constraints, the area overhead of the proposed pixel design is around one TFT more compared to the typical design, which is within the affordable range based on the aperture ratio of our current pixel design. Actually, this 1-TFT area overhead can be further minimized using proper layout techniques. Note that we strictly limit the size of the total capacitance because the capacitor in the typical pixel design already occupies a big portion of the pixel-cell layout. Any further significant increase of the capacitance may result in large area overhead and in turn an unacceptably low aperture ratio.

In the following Sections IV-B and IV-C, we will first detail the behavior of the proposed pixel design during the data-written phase and the data-retained phase, respectively. Next, we will compare the proposed pixel design with the typical pixel design based on the result of analysis, simulation, and measurement. Also, we will discuss the impact of using different combinations of the sizes of C_1, C_2, and C_3 on the display-data variation and the data-written time.

B. Circuit Behavior During Data-Written Phase

During the data-written phase, $Scan\_line$ is set to high and both M_3 and M_4 are turned on. Once M_4 is turned on, the voltages at the two terminals of C_2, P_1, and P_2, are about the same. Then similar data voltage will be written into C_3 through one TFT (M_3) and be written into C_1 through two TFTs (M_3 and M_4). As a result, the discharge of C_2 is relatively small during the data-written phase. Since writing data into C_1 needs to pass a larger resistance (one more TFT) than writing data into C_3, a smaller ratio of C_1 over C_{st} can reduce the write time of the proposed pixel design.

C. Circuit Behavior During Data-Retained Phase

At the beginning of the data-retained phase (right after the data-written phase ends), the voltages at P_1 and P_2 should be the same and represent the display data (the impact of the parasitic capacitance of M_3 and M_4 is ignored here). At the same time, $Scan\_line$ is set to low and both M_3 and M_4 are turned off. Due to the leakage of M_3 and M_4, the data at P_1 and P_2 may be changed. The amount of the leakage current is strongly determined by the TFT's drain-source voltage. As shown in Fig. 6, the leakage current when $V_{ds} = 10$ volt could be 3-order larger than the leakage current when $V_{ds} = 0.1$ volt. Thus, the leakage of M_3 can be much larger than that of M_4 since the voltage between $Data\_line$ and P_1 is significant larger than the voltage between P_1 and P_2 (almost 0 at the beginning of the data-retained phase).

Compared to the typical pixel design shown in Fig. 4, the data variation at P_1 is larger than that at P_0 since the capacitance of C_3 is smaller than that of C_{st}. However, the data variation at P_2 is significantly smaller than that at P_1 due to a smaller leakage current of M_4. Note that the voltage at P_2 represents the display data during the data-retained phase. Thus, the key idea of the proposed design is to protect the data at P_2 by creating a smaller drain-source voltage of M_4 while allowing a larger but proper data variation at P_1. In our later analysis, we will discuss how the setup of the size of C_1, C_2, and C_3 affects the data variation at P_2 for the proposed pixel design.

In fact, the voltage between P_1 and P_2 will increase with time, and in turn may degrade the capability of the proposed pixel for protecting its display data after a certain period of time. Fortunately, this situation only occurs after the time passes the period of the data-retained phase. Thus, the proposed pixel design can still effectively protect its display data for current applications of display panels.

V. Worst-Case Analysis for the Proposed Pixel Design

In this section, we theoretically analyze the degree of display-data variation and the time of writing in a display data for the proposed pixel design, respectively. Also, the analysis for both data variation and write time is performed under their worst case.

A. Worst-Case Display-Data Variation

The leakage current of a transistor is directly proportional to its drain-source voltage. Thus, the worst case of display-data variation of a pixel occurs when the display data of the pixel stores the maximum voltage (denoted as $V_{\max}$) and its $Data\_line$ stays constantly at the minimum voltage (0 volt) during the data-retained phase. Based on this worst-case setting, we then analyze the display-data variation for both the typical and proposed pixel designs, i.e., to calculate the voltage at P_0 in Fig. 4 and the voltage at P_2 in Fig. 7 with respective to time t, respectively.

1) Display-Data Variation of the Typical Pixel Design: The current flowing in the transistor M_1 is equal to the current flowing out of the capacitor C_{st} during its discharging. Thus, the voltage at node P_0 (denoted as V_{P_0}) can be determined by (3), where $R_{M_1\_off}$ represents the resistance of M_1 when M_1 turns off

$$\frac{V_{P_0}}{R_{M_1\_off}} = -C_{st} \cdot \frac{dV_{P_0}}{dt}. \tag{3}$$

By solving the differential equation of (3), we can obtain V_{P_0} versus time as shown in (4). Note that the boundary condition is $V_{P_0} = V_{\max}$ when $t = 0$

$$V_{P_0} = V_{\max} \cdot e^{\frac{-t}{R_{M_1\_off} \cdot C_{st}}}. \tag{4}$$

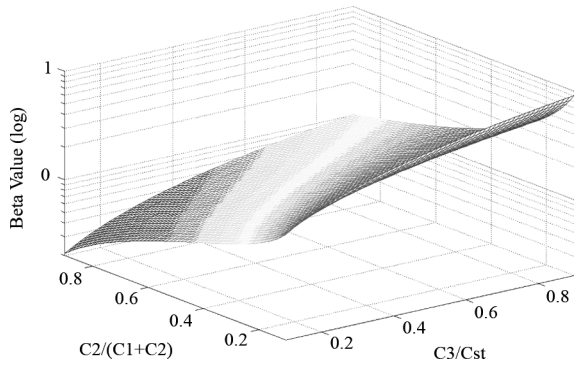

Fig. 8. Beta value associated with different settings of C_1, C_2, and C_3 when $t = 0.01 * R_{\text{off}} * C_{st}$.

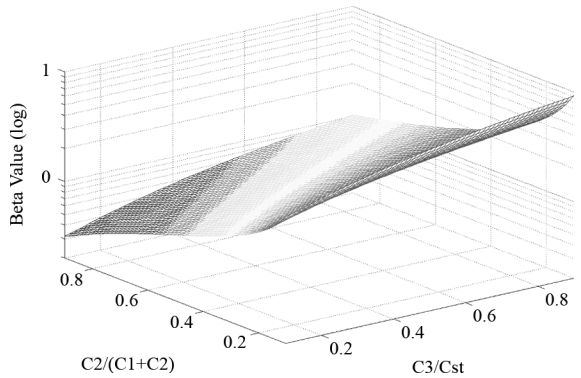

Fig. 9. Beta value associated with different settings of C_1, C_2, and C_3 when $t = 0.1 * R_{\text{off}} * C_{st}$.

Based on (4), we can then derive the derivative of V_{P_0} with respect to time t as listed in (5)

$$\left|\frac{dV_{P_0}}{dt}\right| = \left(\frac{V_{\max}}{R_{M_1\_off} \cdot C_{st}}\right) \cdot e^{\frac{-t}{R_{M_1\_off} \cdot C_{st}}}. \quad (5)$$

2) Display-Data Variation of the Proposed Pixel Design: To analyze the voltage at P_2 (denoted as V_{P_2}) for the proposed pixel design, we need to analyze the voltage at P_1 (denoted by V_{P_1}) first. During the data-retained phase, the turn-off resistance of M_4 (denoted as $R_{M_4\_off}$) can be viewed as infinite since its V_{ds} is low and the leakage current is much smaller than that of M_3. As a result, the equivalent capacitance at P_1 is $[C_3 + (C_2||C_1)]$ during the data-retained phase, where $(C_2||C_1)$ represents the equivalent capacitance when C_2 is connected to C_1 in serial. Thus, by substituting C_{st} with $[C_3 + (C_2||C_1)]$ and $R_{M_1\_off}$ with $R_{M_3\_off}$ in (5), we can obtain the derivative of V_{P_1} with respect to time t as listed in (6)

$$\left|\frac{dV_{P_1}}{dt}\right| = \left(\frac{V_{\max}}{R_{M_3\_off} \cdot [C_3 + (C_2||C_1)]}\right) \cdot e^{\frac{-t}{R_{M_3\_off} \cdot [C_3 + (C_2||C_1)]}}. \quad (6)$$

Because of the charge sharing between C_1 and C_2, the relation between dV_{P_1}/dt and dV_{P_2}/dt can be obtained as in (7)

$$\frac{dV_{P_2}}{dt} \cong \frac{dV_{P_1}}{dt} \cdot \left(\frac{C_2}{C_1 + C_2}\right). \quad (7)$$

By substituting dV_{P_1}/dt with (6), we obtain the derivative of V_{P_2} with respect to time as shown in (8)

$$\left|\frac{dV_{P_2}}{dt}\right| \cong \left(\frac{V_{\max}}{R_{M_3\_off} \cdot [C_3 + (C_2||C_1)]}\right) \cdot e^{\frac{-t}{R_{M_3\_off} \cdot [C_3 + (C_2||C_1)]}} \cdot \left(\frac{C_2}{C_1 + C_2}\right). \quad (8)$$

3) Comparison Between the Proposed and Typical Pixel Designs: To evaluate the effectiveness of the proposed pixel deign on reducing the display-data variation, we first define the factor β as the ratio of dV_{P_0}/dt over dV_{P_2}/dt. A larger value of β means that the proposed pixel design can protect its display data better from the transistor's leakage compared the typical pixel design. Equation (9) shows the calculation of β by combining (5) and (8). Note that $R_{\text{off}} = R_{M_1\_off} = R_{M_3\_off}$ since the transistors used in both designs have the same device size

$$\beta = \left|\frac{\frac{dV_{P_0}}{dt}}{\frac{dV_{P_2}}{dt}}\right| \cong \left(\frac{C_1 + C_2}{C_2}\right) \frac{[C_3 + (C_2||C_1)]}{C_{st}} \cdot e^{\frac{t}{R_{off}} \cdot \{1/[C_3 + (C_2||C_1)] - 1/C_{st}\}}. \quad (9)$$

Equation (9) shows that the value of β is affected by the following factors: 1) the turn-off resistance of the transistor; 2) the size of each capacitor (C_1, C_2, C_3, and C_{st}); and 3) the time t. Figs. 8 and 9 show the logarithm of β associated with C_3/C_{st} and $C_2/(C_1 + C_2)$ when $t = 0.01 * R_{\text{off}} * C_{st}$ and $t = 0.1 * R_{\text{off}} * C_{st}$, respectively. From Figs. 8 and 9, we find the following two trends about the value of β. Note that $C_1 + C_2 + C_3 = C_{st}$.

- A larger C_3 out of the total capacitance C_{st} leads to a higher β.
- A smaller C_2 out of $C_1 + C_2$ leads to a higher β.

The reason for the first trend is that a larger C_3 can minimize the voltage variation at P_1, which in turn can minimize the voltage variation at P_2 as shown in (7). The reason for the second trend is that a smaller $C_2/(C_1 + C_2)$ can minimize the voltage variation at P_2 caused by the charge sharing between the serially connected C_1 and C_2.

Fig. 10 shows the value of β over time for three different settings of C_1, C_2, and C_3. Note that the turn-off resistance R_{off} of a TFT varies along with its V_{ds} as shown Fig. 6, where R_{off} ranges from 10 volt/10^{-10} A to 0.1 volt/10^{-13}A, i.e., 10^{11} Ω to 10^{12} Ω. With C_{st} = 200 fF, the time represented by $1 * R_{\text{off}} * C_{st}$ here should be between 20 and 200 ms (average 110 ms). Since the period of the data-retained phase defined in the specification is 16.7 ms (corresponding to 60 Hz), we care only the value of β before $0.2 * R_{\text{off}} * C_{st}$. During this period (0 to $0.2 * R_{\text{off}} * C_{st}$) in Fig. 10, the value of β is almost a constant for all capacitance settings.

However, the above analysis is only an approximation since the TFT transistor M_4 is assumed to be fully turned off during the data-retained phase. In reality, a smaller C_2 may not always lead to a higher β because a larger C_2 can help to reduce the variation of V_{ds} of M_4 and in turn limit the leakage current of M_4. Fig. 11 shows the V_{ds} of M_4 over time with different values of

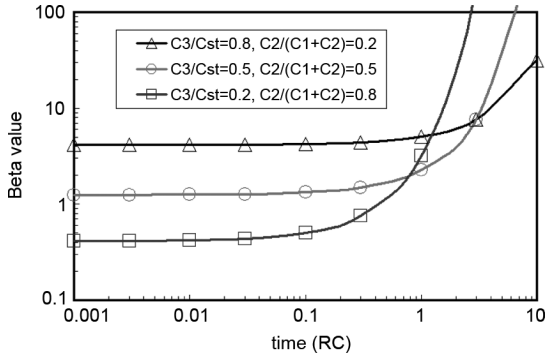

Fig. 10. β over time for three capacitance settings.

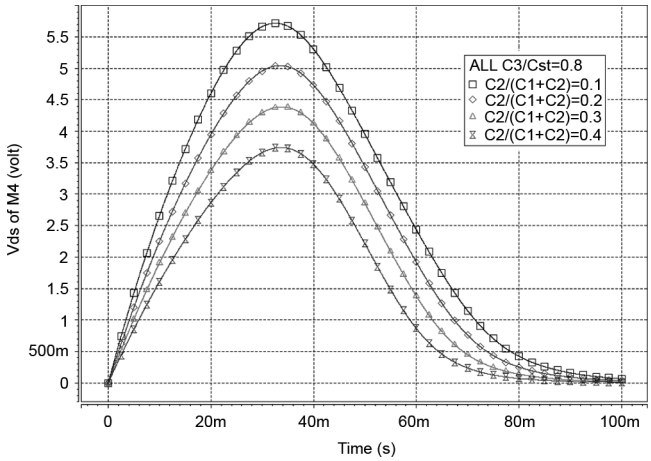

Fig. 11. V_{ds} of M_4 over time associated with different values of C_2 given $C_3/C_{st} = 0.8$.

C_2, where the V_{ds} of M_4 increases while C_2 decreases. If a too small C_2 is used, the leakage of M_4 will significantly increase, which will then speed up the voltage variation at P_2. Thus, the size of C_2 should be controlled within a proper range to minimize the display-data variation. This constraint also implies that the size of C_3 cannot be too large since the total capacitance of C_1, C_2, and C_3 is a constant (C_{st}). A too large C_3 will limit the size of C_2.

Since the V_{ds} of M_4 is originally 0 at the beginning and then gradually becomes larger, the leakage of M_4 becomes larger along with the time, meaning that the proposed pixel design can only protect its display data effectively at the early stage and may gradually lose its capability of data protection later on. Fortunately, the increase of the V_{ds} of M_4 in our proposed pixel design is not significant enough during the data-retained phase defined in our specification (16.7 ms, reciprocal of 60 Hz). Thus, compared to the typical design, the proposed pixel design can still effectively protect the display data with a proper setting of its three capacitors. We will show the simulation result to validate this phenomenon in the next section.

B. Worst-Case Write Time

In this subsection, we analyze the worst-case write time, i.e., writing a $V_{\max}$ into a pixel whose original value is 0 volt, for both typical and proposed pixel designs. The write time of a pixel design is determined by its equivalent RC time constant.

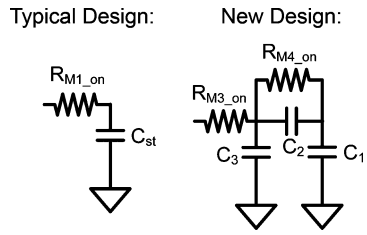

Fig. 12. Illustration of the RC model during the data-written phase for both the typical and proposed designs.

Fig. 12 illustrates the simplified RC model for both the typical and the proposed new pixel design, where $R_{M_x\_on}$ represent the resistance of the transistor M_x when M_x turns on.

Based on the RC model of Fig. 12, (10) and (11) shows the worst-case write time for the typical design (denoted as WT_{typ}) and the proposed design (denoted as WT_{pro1}), respectively. Note that the transistors on both designs have the same device size and hence $R_{\text{on}} = R_{M_1\_on} = R_{M_3\_on} = R_{M_4\_on}$

$$WT_{\text{typ}} \propto R_{M_1\_on} \cdot C_{st} = R_{\text{on}} \cdot C_{st} \tag{10}$$

$$\begin{aligned} WT_{\text{pro1}} &\propto (R_{M_3\_on} + R_{M_4\_on}) \cdot C_1 \\ &\quad + R_{M_4\_on} \cdot C_2 + R_{M_3\_on} \cdot C_3 \\ &= R_{on} \cdot (2C_1 + C_2 + C_3) \\ &= R_{on} \cdot (C_{st} + C_1). \end{aligned} \tag{11}$$

In fact, the WT_{pro1} in (11) represents the upper bound of the worst-case write time of the proposed design. The term $R_{M_4\_on} \cdot C_2$ is overestimated since the voltage between P_1 and P_2 is small during the data-written phase (small $R_{M_4\_on}$) and C_2 is not fully discharged. If we completely ignore the impact of C_2 and eliminate the term $R_{M_4\_on} \cdot C_2$ from (11), a lower bound of the worst-case write time can be obtained as in (12)

$$\begin{aligned} WT_{\text{pro2}} &\propto (R_{M_3\_on} + R_{M_4\_on}) \cdot C_1 + R_{M_3\_on} \cdot C_3 \\ &= R_{\text{on}} \cdot (C_{st} + C_1 - C_2). \end{aligned} \tag{12}$$

As (11) shows, the upper bound of the worst-case write time of the proposed design is $R_{\text{on}}C_1$ more than that of the typical design. As (12) shows, the lower-bound of the worst-case write time is $R_{\text{on}}C_2$ less than the upper bound. Thus, to reduce the write time for the proposed design, C_1 needs to be smaller and C_2 needs to be larger. However, a smaller C_1 and a larger C_2 may decrease pixel's capability of protecting the display data. In Section VI, we discuss how to find a proper setting of all capacitors used in the proposed pixel design through simulation.

VI. Simulation Results

In this section, we will discuss the following issues through the simulation results, which are performed based on the PECVD-based bottom-gate nc-Si-TFT technology developed by ITRI [8].

A. Worst-Case Display-Data Variation

In the following experiment, we simulate the display-data variation of the proposed design by using different settings of its capacitors (C_1, C_2, and C_3), and then compare it to that of the typical design. The display-data variation is defined by the

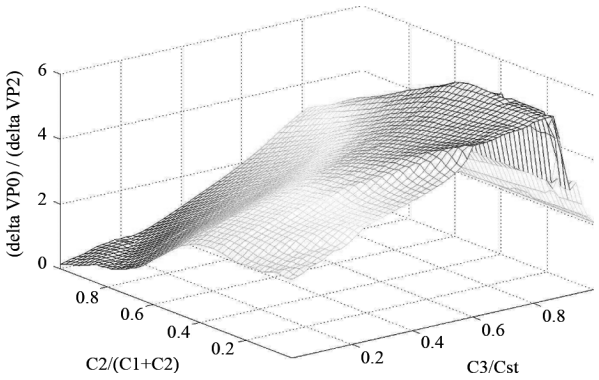

Fig. 13. $\Delta V_{P_0}/\Delta V_{P_2}$ associated with different capacitance settings.

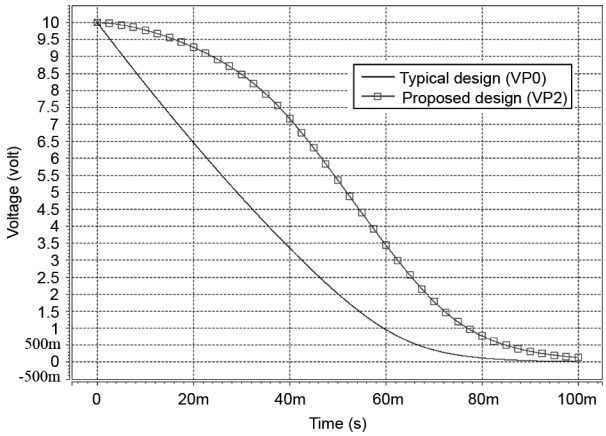

Fig. 14. Stored display data over time for both the typical and proposed designs.

biggest voltage difference to its original stored voltage (at P_2 or P_0) caused during a whole data-retained phase. We use ΔV_{P_0} and ΔV_{P_2} to denote this display-data variation for the typical and the proposed designs, respectively. The stored display data here is set to $V_{\max}$, i.e., 10 volt in our specification, and its $Data\_line$ is enforced to stay at 0 volt such that the leakage current of the pixel can be the worst. The total capacitor in use (C_{st}) is 200 fF. The channel length and width of a TFT transistor are both 8 μm. The period of a data-retained phase is 16.7 ms (reciprocal of 60 Hz). Fig. 13 shows the ratio of ΔV_{P_0} over ΔV_{P_2} for different combination of C_3/C_{st} and $C_2/(C_1+C_2)$, where $C_1+C_2+C_3=C_{st}$.

As the result shows, Fig. 13 confirms our inferences about display-data variation in Section V-A. First, $\Delta V_{P_0}/\Delta V_{P_2}$ increases when C_3 increases initially but then starts to drop after C_3 is larger than a certain value. Second, $\Delta V_{P_0}/\Delta V_{P_2}$ also increases when C_2 decreases initially but then starts to drop after C_2 is smaller than a certain value. The peak of $\Delta V_{P_0}/\Delta V_{P_2}$ occurs when $C_3/C_{st}=0.86$ and $C_2/(C_1+C_2)=0.32$. Also, the peak value of $\Delta V_{P_0}/\Delta V_{P_2}$ is more than 5.65, meaning that the proposed design can effectively reduce the data variation by 5.65 times compared to the typical design.

Next, Fig. 14 shows the V_{P_0} and V_{P_2} versus time, given that $C_{st}=200$ fF, $C_3/C_{st}=0.86$, and $C_2/(C_1+C_2)=0.32$. The rest experiment setting is the same as that used for Fig. 13. As the result shows, the display data of the proposed design (V_{P_2}) drops much slower than the typical design at the beginning but then drops faster after a certain period of time. In this experiment, V_{P_2} starts to drop faster than V_{P_0} when t is larger than 37.5 ms, which is much longer than the normal specification of the data-retained phase, 16.7 ms. This result further demonstrates the effectiveness of the proposed pixel design on reducing the display-data variation for practical applications of display panels.

B. Worst-Case Write Time

Fig. 15 shows the ratio of the worst-case write time of the proposed design (denoted as $WT_{\rm pro}$) over that of the typical design (denoted as $WT_{\rm typ}$) for different capacitance settings. As the result shows, the write time of the proposed design decrease when C_2 increases or C_1 decreases, which fits the conclusion of our analysis in Section V-B.

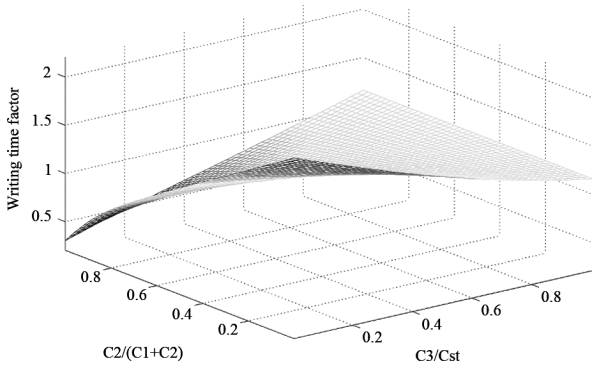

Fig. 15. $WT_{\rm pro}/WT_{\rm typ}$ associated with different capacitance settings.

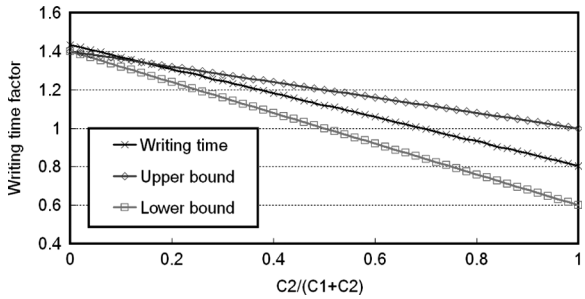

Fig. 16. $WT_{\rm pro}/WT_{\rm typ}$ versus $C_2/(C_1+C_2)$ when $C_3/C_{st}=0.6$.

Fig. 16 further shows the $WT_{\rm pro}/WT_{\rm typ}$ obtained by the simulation, the upper bound in (11), and the lower bound in (12) when C_3/C_{st} is set to 0.6 and $C_2/(C_1+C_2)$ varies. The result again confirms our analysis on the write time for the proposed design.

C. Finding a Proper Capacitance Setting

In general, the write time of the pixel design is usually a constraint instead of a factor to be minimized. Thus, in this subsection, we attempt to find a capacitance setting for the proposed design which can result in the largest $\Delta V_{P_0}/\Delta V_{P_2}$ under the constraint that its $WT_{\rm pro}/WT_{\rm typ}$ is not more than 1.15. We first find the capacitance setting with the largest $\Delta V_{P_0}/\Delta V_{P_2}$,

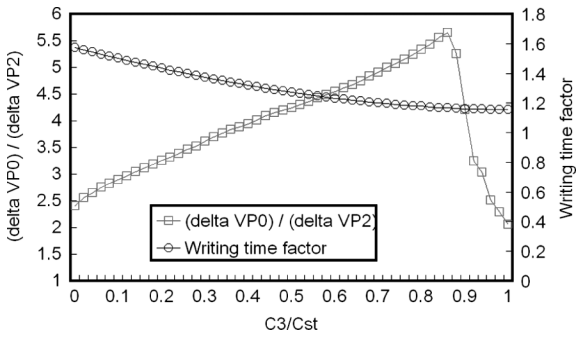

Fig. 17. $\Delta V_{P_0}/\Delta V_{P_2}$ and $WT_{\rm pro}/WT_{\rm typ}$ versus C_3/C_{st} when $C_2/(C_1+C_2)=0.32$.

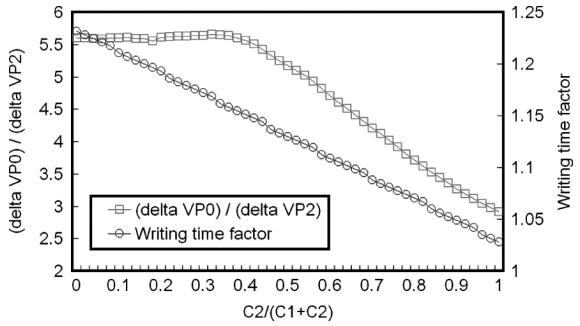

Fig. 18. $\Delta V_{P_0}/\Delta V_{P_2}$ and $WT_{\rm pro}/WT_{\rm typ}$ versus $C_2/(C_1+C_2)$ when $C_3/C_{st}=0.86$.

i.e., $C_3/C_{st}=0.86$ and $C_2/(C_1+C_2)=0.32$ as shown in Fig. 13. For $C_3/C_{st}=0.86$ and $C_2/(C_1+C_2)=0.32$, its $\Delta V_{P_0}/\Delta V_{P_2}$ is 5.65 but its $WT_{\rm pro}/WT_{\rm typ}$ is 1.17, which exceeds the constraint of 1.15. We then search around the capacitance setting around the peak point, $C_3/C_{st}=0.86$ and $C_2/(C_1+C_2)=0.32$. Fig. 17 shows both $\Delta V_{P_0}/\Delta V_{P_2}$ and $WT_{\rm pro}/WT_{\rm typ}$ when $C_2/(C_1+C_2)$ is fixed at 0.32 and C_3/C_{st} varies. As the result shows, the improvement of the proposed design on the display-data variation drops rapidly when C_3/C_{st} is over 0.86 but the corresponding write time does not drop significantly. Thus, $C_3/C_{st}=0.86$ appears to be the best setting.

Next, Fig. 18 shows $\Delta V_{P_0}/\Delta V_{P_2}$ and $WT_{\rm pro}/WT_{\rm typ}$ when C_3/C_{st} is set to 0.86 but $C_2/(C_1+C_2)$ varies. As the result shows, the improvement on the display-data variation stays around the same level when $C_2/(C_1+C_2)$ is near the peak point 0.32. Thus, we can then choose the capacitance setting in Fig. 18 which results in the largest $\Delta V_{P_0}/\Delta V_{P_2}$ with $WT_{\rm pro}/WT_{\rm typ}<1.15$, i.e., $C_2/(C_1+C_2)=0.4$ and $C_3/C_{st}=0.86$. Its improvement on display-data variation can be 5.55× and its $WT_{\rm pro}/WT_{\rm typ}$ is exactly 1.15.

Note that designers may need to consider more design parameters other than the write time and the display-data variation, such as layout area or aperture ratio. The capacitance setting for the proposed design should be chosen based on the corresponding objective and design constraints in use. In fact, several capacitance settings in Fig. 13 can achieve a $\Delta V_{P_0}/\Delta V_{P_2}$ close to the maximum. The designers could utilize those settings for optimizing other design parameters.

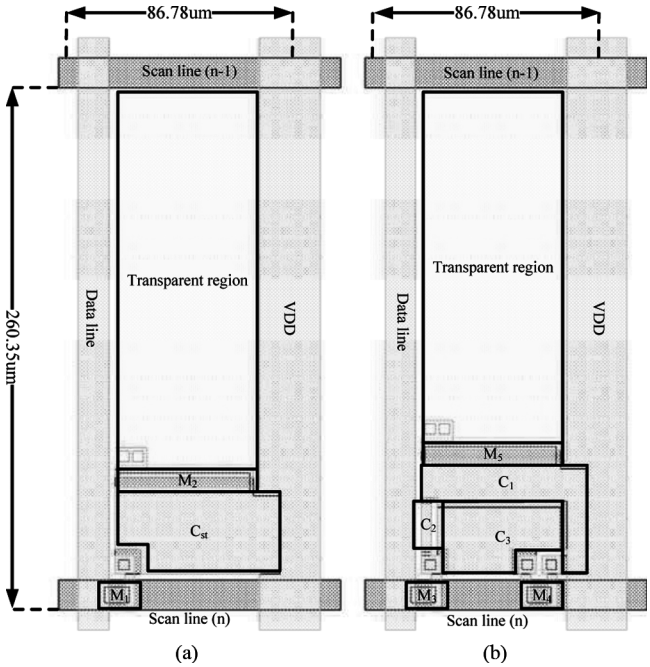

Fig. 19. Layout of the typical and proposed designs for a 4.1" QVGA color AM-OLED panel. (a) Typical design. (b) Proposed design.

D. Area Overhead and Aperture Ratio

Fig. 19(a) and (b) illustrate the layout of the typical pixel design and the the proposed pixel design, respectively. Both pixel designs follows the specification of 4.1" QVGA color AM-OLED backplanes. Its resolution is 320xRGBx240 and its pixel size is 86.78 μm × 260.35 μm for each of the red, green, and blue pixels. For our application, we utilize a white-light OLED along with a corresponding color filter to generate each of RGB colors instead of using an individual OLED which can directly generate the corresponding color. Thus, the pixel sizes as well as their required aperture ratios are the same for all red, green, and blue pixels.

Compared to the typical design, the area overhead of the proposed pixel design is an extra transistor (M_4). The total capacitances for both designs are the same. However, as shown in the bottom-right of Fig. 19(b), this transistor (M_4) can be placed above the metal of $Scan\_line$, and hence its resulting area overhead for the control design can be reduced, which in turn limits the decrease of the aperture ratio for the proposed design. Overall, the aperture ratios of the the proposed design is 41.4%, which is 3.2% lower than that of the typical design (44.6%) and is still higher than the minimum requirement of the aperture ratio (40%) for most AM-OLED displays. This 3.2% lose on the aperture ratio results from the extra contact holes and the spacing around the two more capacitors enforced by the design rules.

Note that, for both typical and proposed designs, the area occupied by the capacitors is much more than that occupied by the transistors. That is why we are only willing to spend extra area for transistors to reduce the display-data variation, but not extra area for capacitors. The same percent increase in the total capacitance can result in a significant lose in its aperture ratio.

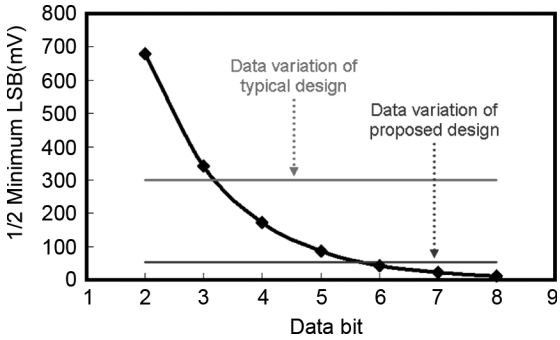

Fig. 20. Improvement of the contrast resolution achieved by using the proposed pixel.

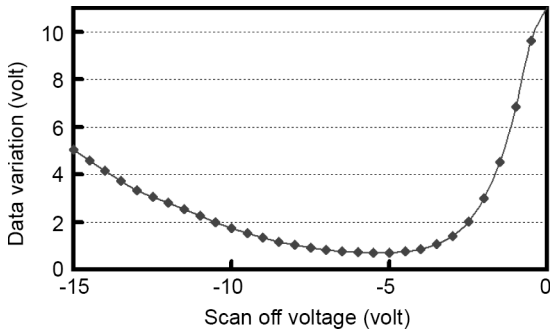

Fig. 21. Worst-case display-data variation versus V_{SL}.

In addition, for the AM-OLED applications which require a higher requirement of the aperture ratio, we can further eliminate the V_{DD} metal line with other signal metal lines [13]. Also, top-emission scheme can be used to provide a higher aperture ratio [14], [15].

E. Improvement on Contrast Resolution

In this subsection, we attempt to identify the contrast resolution which can be achieved by our current nc-Si-TFT technology [8] with and without applying the proposed pixel design. The supportable contrast resolution for a nc-Si-TFT technology is determined by its display-data variation during the data-retained phase and the voltage of its LSB (least-significant-bit) after Γ-correction. As long as the corresponding display-data variation is less than one half of the LSB voltage, this contrast resolution is supportable.

Fig. 20 shows one half of the LSB voltage required by different numbers of resolution bits. Also, Fig. 20 shows the display-data variation caused by the typical design and the proposed design, respectively. As the result shows, the typical design can only support a 3-bit contrast resolution with our current nc-Si-TFT technology while the proposed design can support a 5-bit contrast resolution. For general display applications, the number of resolution bits is 8.

VII. Other Issues for the Proposed Pixel Design

A. Turn-Off Voltage at Scan Line

As Fig. 6 shows, I_{ds} does not always decrease when V_{gs} decreases, meaning that decreasing the turn-off voltage at $Scan\_line$ may not be always able to decrease the leakage current. Also, the V_{gs} leading to the minimum I_{ds} also varies with different V_{ds}. Thus, in this subsection, we attempt to find an appropriate turn-off voltage at $Scan\_line$ (denoted as V_{SL}) such that the display-data variation for a pixel can be minimized. We first denote the V_{gs} leading to the minimum I_{ds} given $V_{ds} = x$ as $ML\_V_{gs}|_{V_{ds}=x}$. In Fig. 6, $ML\_V_{gs}|_{V_{ds}=10\text{volt}}$ is -6.41 volt and $ML\_V_{gs}|_{V_{ds}=0.1\text{volt}}$ is -8.48 volt, where $V_{\max} = 10$ volt and $V_{\min} = 0$ volt.

The ideal case for a good setting of V_{SL} is that its resulting V_{gs} can be close to $ML\_V_{gs}|_{V_{ds}}$ for each V_{ds}. However, V_{ds} is determined by the voltage at $Data\_line$, which may vary randomly and hard to predict. Also, V_{ds} is determined by the voltage of the stored data, which further determines the corresponding $ML\_V_{gs}|_{V_{ds}}$. It makes the analysis for the best V_{SL} even harder. Thus, we can only know that the best V_{SL} should be around $ML\_V_{gs}|_{V_{ds}=V_{\max}}$ since the scale of I_{ds} when $V_{ds} = V_{\max}$ is several orders larger than that when $V_{ds} = V_{\min}$.

Fig. 21 shows the display-data variation with different settings of V_{SL}, where the store data is set as $V_{\max}$ to create a worst case and the voltage at $Data\_line$ is a full-range triangle wave to approximate the random data in real applications. As the result shows, the display-data variation can be minimized when setting the turn-off voltage at $Scan\_line$ to -5.5 volt, which is $ML\_V_{gs}|_{V_{ds}=10\text{volt}}$(-6.41 volt) plus a small constant.

B. Coupling Effect

The *coupling effect* of a pixel design is referred to the transient voltage drop of the stored data caused by the signal transition at $Scan\_line$ (from 1 to 0) interacting with the parasitic capacitors of switch transistors. As a result, at the beginning of the data-retained phase, the stored value first drops by the coupling effect and then varies by switch transistor's leakage (discussed as data variation previously). This coupling effect has been existed on the pixel designs of AM-LCD and AM-OLED displays. Fig. 22(a) illustrates the coupling effect on the typical pixel design of AM-OLED displays. Fortunately, on the typical pixel design, the voltage drop caused by the coupling effect is almost a constant value for different stored data voltages. It means that by elevating every stored data voltage with a fixed constant, the displayed lightness can remain almost the same as if no coupling effect exists. This solution to the coupling effect can be implemented easily without significant overhead [16] and has already been used for AM-LCD displays.

For the proposed pixel design, the coupling effect becomes larger since the impact of two more parasitic capacitors (C_{gd} and C_{gs}) of M_4 is taken into account other than the C_{gs} of M_3 [as shown in Fig. 22(b)]. Fig. 23 shows the voltage drop caused by the coupling effect corresponding to each stored data voltage on the typical design (denoted by Typ) and the proposed designs with 3 arbitrary capacitance settings (denoted by P_1, P_2, and P_3). The capacitance settings are $(P1)$ $C_3/C_{st} = 0.4$, $C_2/(C_1 + C_2) = 0.3$; $(P2)$ $C_3/C_{st} = 0.5$, $C_2/(C_1 + C_2) = 0.2$; and $(P3)$ $C_3/C_{st} = 0.6$, $C_2/(C_1 + C_2) = 0.1$. As the result shows, the voltage drop of the proposed design is around the same for each stored data voltage just like the typical design, and the same trend can be observed on different capacitance

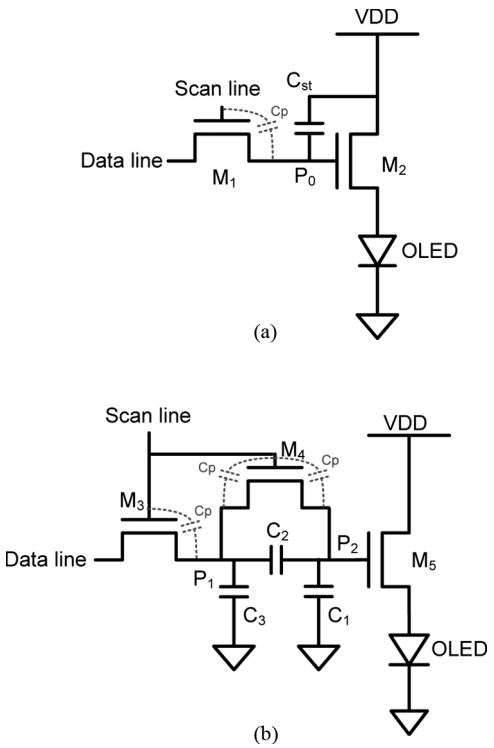

Fig. 22. Parasitic capacitance of the switch TFTs for both the typical and the proposed pixel design. (a) Typical design. (b) Proposed design.

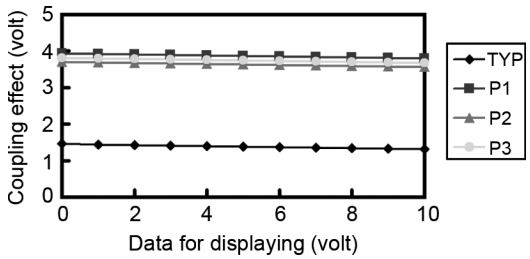

Fig. 23. Coupling effect associated with different stored data for the typical and proposed designs.

settings of the proposed design. It means that the coupling effect can also be solved for the proposed design with the same simple solution described above.

VIII. Measurement of Fabricated TFT Circuits

A. Measurement Procedure

We have fabricated both the typical and the proposed pixel design using the PECVD-based bottom-gate nc-Si-TFT technology developed by ITRI [8]. Fig. 24 shows the photo of a fabricated die, which contains several single pixel designs with different configurations. If we directly probe the voltage of the stored data (V_{P_0} or V_{P_2}), the prober of the oscilloscope will impose a 10 pF capacitance and a 1 MΩ resistance to the pixel design. Thus, we need to measure the voltage at the source of the transistor driving the OLED through an IO pad and then infer the voltage of the corresponding stored data. Fig. 25 illustrates the measurement setting for both the typical and the proposed designs. Note that the fabricated pixel designs are not connected

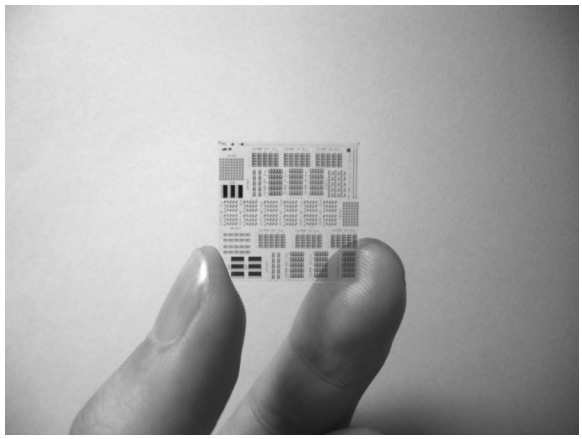

Fig. 24. Photo of the fabricated die.

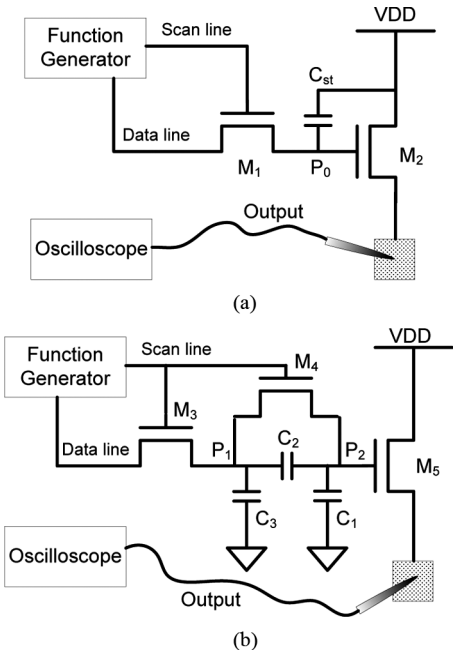

Fig. 25. Measurement setting for both the typical and proposed designs. (a) Typical design. (b) Proposed design.

to any OLED. The OLED is replaced by an IO pad for measurement use.

In order to infer the stored data of a pixel (V_{P_0} or V_{P_2}), we need to build the relation between the voltage at the gate (denoted as V_g) and the voltage at the source (denoted as V_s) of the TFT transistor driving the OLED (i.e., M_2 or M_5). For the fabricated typical and proposed designs, the device dimension of both M_2 and M_5 is 40 μm/8 μm. Fig. 26(a) illustrates how we built the relation between V_g and V_s of M_2 (or M_5), where we generate a 1 Hz triangle wave ranging from 0 volt to 10 volt at V_g and then measure the corresponding V_s through an IO pad. The transistor's drain is connected to V_{DD} (10 volt). Fig. 26(b) shows the measured V_s versus V_g. Due to the noise of the measured result, we utilize a monotonically-increasing sixth-order polynomial to fit this curve and use the polynomial to map the measured V_s to V_g. Note that this relation between V_g and V_s is characterized combining the effect of the prober's parasitic

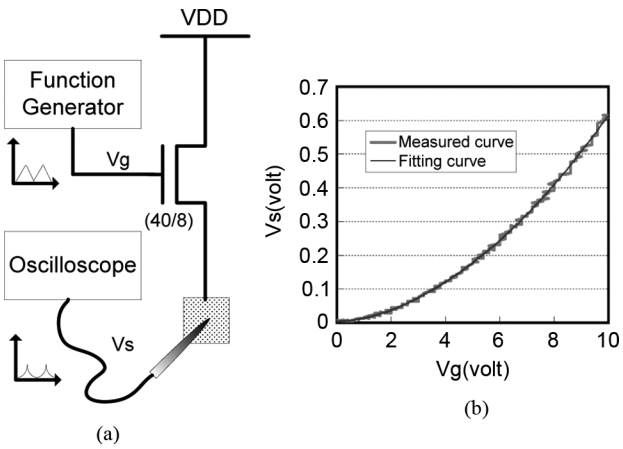

Fig. 26. V_s versus V_g of the TFT driving the OLED.

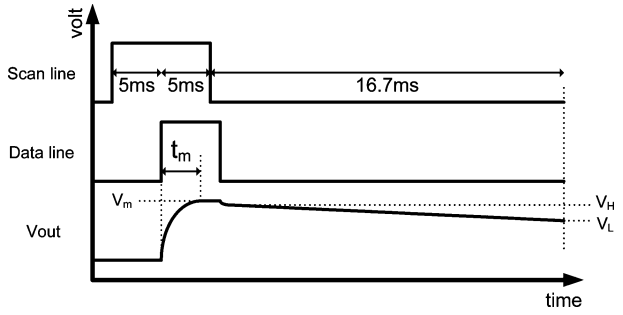

Fig. 27. Signal at $Scan\_line$ and $Data\_line$ and an exemplary measured result.

capacitance and resistance, which is exactly the same condition when measuring the fabricated pixel designs. Thus, no compensation needs to be added into this characterized $V_g - V_s$ relation when it is used to infer the stored data of a pixel design.

Fig. 27 shows the signal at $Scan\_line$ and $Data\_line$ during our measurement as well as an exemplary measured voltage at the output IO pad (denoted as V_{out}). When $Scan\_line$ just turns on, $Data\_line$ keeps on 0 volt for 5 ms to make sure that the stored data is set to 0 volt. Next, $Data\_line$ is set to 10 volt and we start to measure the write time. After another 5 ms, we turns off $Scan\_line$ and start to measure the display-data variation during the next 16.7 ms (the period of the data-retained phase). Note that, due to the coupling effect mentioned previously, the voltage setting of the $Data\_line$ has been slightly adjusted for equal stored data in both the typical and the proposed design.

To obtain the display-data variation, we measure the highest V_{out} (denoted as V_H) and the lowest V_{out} (denoted as V_L) during the 16.7 ms data-retained phase. Then we map V_H and V_L into their corresponding V_{P_2} (or V_{P_0}) using the characterized $V_g - V_s$ relation shown in Fig. 26(b). The difference between the two mapped V_{P_2} is the measured display-data variation.

To obtain the write time, we measure the time from $V_{\text{out}} = 0$ to $V_{\text{out}} = V_m$ (denoted as t_m), where V_m is the maximum voltage when $Scan\_line$ is on. The measured write time is equal to t_m minus the gate-source delay of the transistor. Fig. 28 shows how we obtain the gate-source delay, where a square wave is generated at the gate and measure the time when V_s reach the top. In fact, we only choose to use the time when V_s

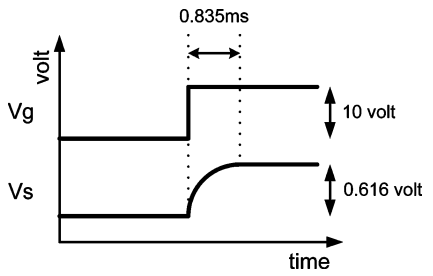

Fig. 28. Measurement of the gate-source delay.

TABLE II
MEASUREMENT RESULTS FOR 3 DIFFERENT CONFIGURATIONS OF THE TYPICAL PIXEL DESIGN

Typical design				
Config.	(W/L) of M_1	C_{st}	data var. ratio	write time ratio
T-1	(8/8)	$200fF$	1	1
T-2	(8/16)		1.22	1.98
T-3	(8/24)		2.38	3.40

reaches the 98% of the top as the gate-source delay since the signal above the 98% vibrates severely and it takes long time to reach the true top of V_s. Similarly, when measuring t_m, we also choose the time when the measured V_{out} reaches the 98% of V_m.

B. Measurement Result

Table II lists the measured display-data variation and write time for three configurations of the fabricated typical pixel designs, denoted as T-1, T-2, and T-3. The difference among the three configurations is the channel length of their M_1 TFT transistor, where the channel length of T-2 and T-3 is double and triple of that of T-1, respectively. The reported display-data variation for a configuration T-x is actually a ratio compared to that of T-1, which is ΔV_{P_0} of T-1 over ΔV_{P_0} of T-x. The reported write time for a configuration T-x is the write time of T-x over that of T-1.

As the result shows, increasing the channel length of M_1 can indeed reduce the display-data variation. However, its write-time overhead is directly proportional to its channel length. If we triple the channel length, its measured write time will increase more than 3 times. Also, its improvement on display-data variation is only 2.38. This result further demonstrates that increasing the channel length of M_1 is not a cost-effective method to reduce the display-data variation.

Table III lists the measured display-data variation and write time for nine configurations of the fabricated proposed pixel designs, denoted as P-1 to P-9. Each configuration utilizes a different capacitance setting with $C_{st} = 200$ fF. The device dimension of both M_3 and M_4 for all nine configuration is 8 μm/8 μm. Similar to Table II, the reported display-data variation and write time is a ratio compared to that of the typical design using T-1 configuration.

As the result shows, the reported display-data variation and write time fit our analysis and simulation results. Basically, a larger C_3/C_{st} can result in a lower display-data variation and a shorter write time before reaching its optimal point ($C_3/C_{st} = 0.86$ in our simulation). Also, a larger $C_2/(C_1+C_2)$ can always

TABLE III
MEASUREMENT RESULTS FOR NINE DIFFERENT CONFIGURATIONS OF THE PROPOSED PIXEL DESIGN

Proposed new design ($C_{st} = 200fF$)					
Config.	(W/L) of $M_{3,4}$	$\frac{C_3}{C_{st}}$	$\frac{C_2}{(C_1+C_2)}$	$\frac{\Delta V_{P_0}}{\Delta V_{P_2}}$	$\frac{WT_{pro}}{WT_{typ}}$
P-1	(8/8)	40%	10%	1.86	1.51
P-2		40%	20%	1.45	1.40
P-3		40%	30%	1.34	1.33
P-4		50%	10%	2.24	1.40
P-5		50%	20%	1.97	1.36
P-6		50%	30%	1.89	1.26
P-7		60%	10%	4.06	1.36
P-8		60%	20%	2.96	1.29
P-9		60%	30%	2.21	1.22

result in a shorter write time. Compared to that of the typical design T-1, the best improvement on display-data variation among the nine fabricated proposed designs is 4.06× with only 1.36× write time. This result again validates the effectiveness of the proposed pixel design based on real fabricated TFT circuits.

IX. CONCLUSION

In this paper, we have introduced a novel pixel design to reduce the data variation caused by the leakage current of nc-Si TFT. We first theoretically analyzed the trend of its worst-case data variation and its worst-case write time. Next, several simulations associated with different capacitance settings were conducted to verify the correctness of our analysis. As the result shows, the proposed pixel design can achieve a 5.55× reduction on its data variation while requiring only 1.15× write time when compared to the typical pixel design. The resulting contrast resolution can also be improved by two bits. In addition, the area overhead of the proposed pixel design can be effectively limited by the layout techniques, and thus the proposed design can still provide an aperture ratio over 40%. We further discussed the proper setting of the turn-off voltage at $Scan\_line$ and the impact of the coupling effect on the proposed pixel design. At last, we reported the measurement results based on the PECVD-based bottom-gate nc-Si-TFT technology developed by ITRI [8].

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