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Electrical properties of SiGe nanowire following fluorine/nitrogen plasma treatment

Kow-Ming Chang [a], Chu-Feng Chen [a,*], Chiung-Hui Lai [b], Po-Shen Kuo [a], Yi-Ming Chen [a], Tai-Yuan Chang [a]

[a] Department of Electronics Engineering, National Chiao Tung University, No. 1001, University Road, Hsinchu 300, Taiwan, ROC
[b] Department of Electronics Engineering, Chung Hua University, Hsinchu 300, Taiwan, ROC

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ABSTRACT

The improvements to electrical properties of SiGe nanowires by surface plasma treatment were investigated. Various durations of pre-oxidation with fluorine; ambients for post-nitridation plasma treatment, and annealing temperature after plasma treatment, 800–950 °C, were applied. Pre-oxidation treatment using fluorine plasma; improved the conductance of SiGe nanowires because the Si–F binding energy created a more stable interface state than bare nanowire on the surface of SiGe. N_2 plasma incorporated more N than does in NH_3 plasma, and NH_3 has the drawback of introducing electron traps, causing Si–H bonds to break in the subsequent annealing process. Since the reparation of surface defects by plasma treatment is valid, the high post-annealing temperature to reduce defect by re-crystallizing can be reduced. Hence, Ge diffusion at low post-annealing temperature did not reduce the high concentration of Ge at the SiGe nanowire surfaces.

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1. Introduction

The modification of the band structure of strain Si metal–oxide–semiconductor filed-effect transistors by in-plane tensile strain is known to improve electron and hole mobilities [1,2]. However, the hole mobility enhancement is only slight, because in $Si_{1-x}Ge_x$ material contains only a small fraction of Ge [3,4].The value of x should be as large as 0.3 to enhance mobility significantly [5]. The Ge condensation process has the benefit of increasing the Ge fraction by oxidation, allowing a much lower Ge fraction to be used in the starting material. A low-Ge fraction is expected to inhibit the formation of dislocations in SiGe, because it associated with a low lattice mismatch between the initial SiGe and SOI layer [6–9]. The free surface of a semiconductor is well known to have a high surface state because it has many dangling bonds. A free Si surface generally has a surface density of approximately 10^{15} cm^{-2} eV^{-1} [10], but the interface density at SiO_2/Si can be made less than10^{11} cm^{-2} eV^{-1}.Thus, surface passivation is very important in suppressing the degradation of carrier mobility in SiGe films. A passivated SiO_2 layer, thermally grown [11] or deposited by PECVD [12], effectively reduces density of surface states when SiGe undergoes oxidation process. Therefore, fluorine and nitrogen have been incorporated into interfacial layers (IL) and dielectric layer for high-κ material has been reported [13–16]. Hence, the main goal of this investigation is to elucidate the effect of fluorine and nitrogen incorporation on the surface of SiGe nanowire by plasma treatment.

2. Experiment

The side-wall spacer method [17] is the cheapest and easiest method for fabricating a nanowire sensor, and it was utilized heein to fabricate the nanowire samples. A p-type (boron doped) Si substrate (1 0 0) with a resistance of 8–10 Ω cm^{-1} was used. Following an initial standard RCA cleaning, the 500 nm-thick oxide was grown on the Si substrate by wet oxidation. Then, the oxide layer was patterned by optical lithography and dry etching. The remaining oxide thickness was approximately 300 nm. This 300 nm-high oxide layer served as the bottom oxide in side-wall spacer etching. A 200 Å-thick amorphous Si (α-Si) layer was deposited by LPCVD at 650 °C and a 2000 Å-thick $Si_{0.86}Ge_{0.14}$ layer was deposited by UHV-CVD at 655 °C after RCA cleaning of the wafer. Self-aligned etching was carried out to form side-wall-spacer nanowires. Fig. 1 schematically depicts three SiGe nanowire samples that had undergone surface treatments. Fig. 1(a) presents a bare SiGe nanowire, without any surface treatment; Fig. 1(b) shows the SiGe nanowire that had been pre-treated with CF_4 plasma. After the formation of the α-Si/SiGe layer and the pre-plasma treatment, the samples were treated in

* Corresponding author. Tel.: +88635731887; fax: +88635731887.
E-mail address: grapechen@gmail.com (C.-F. Chen).

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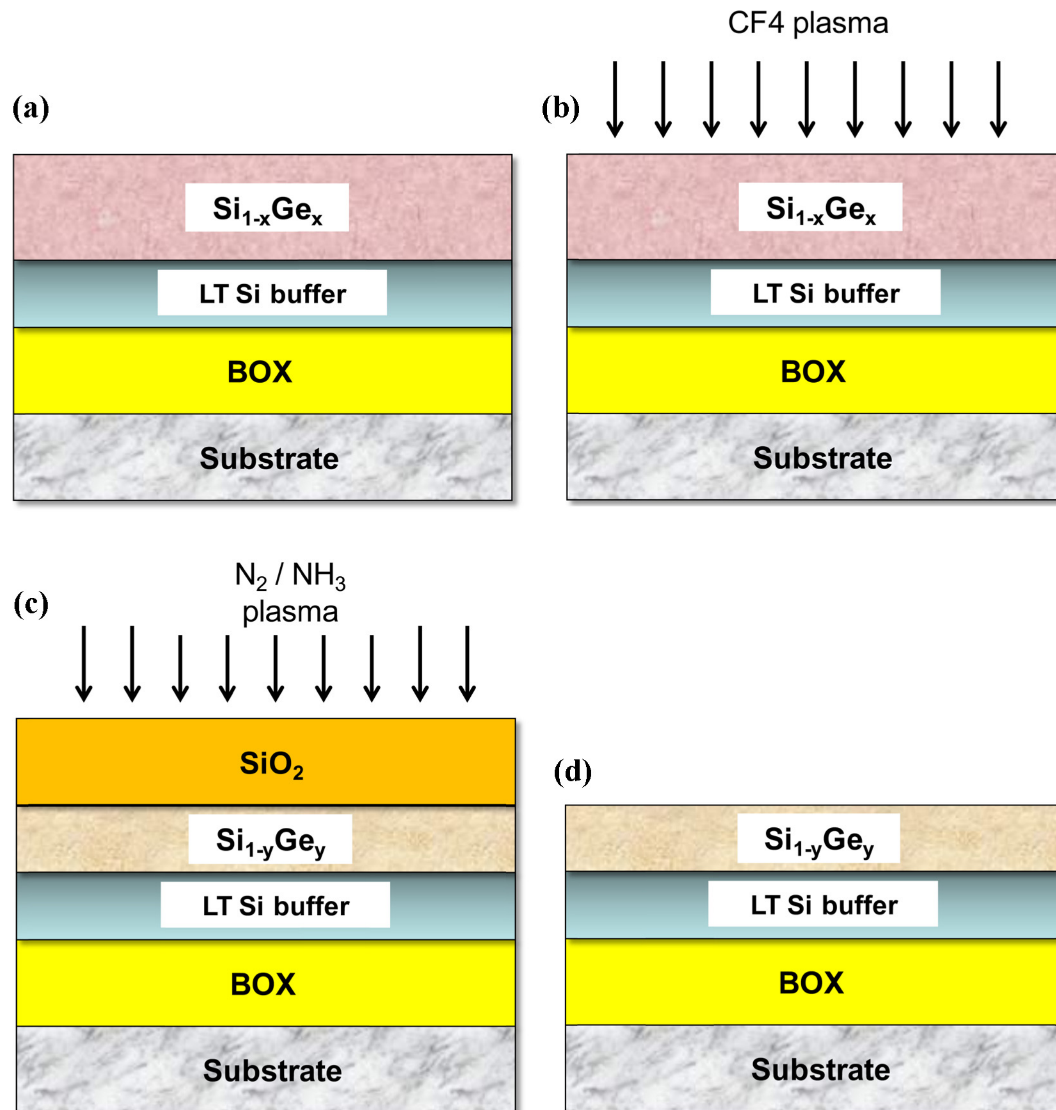
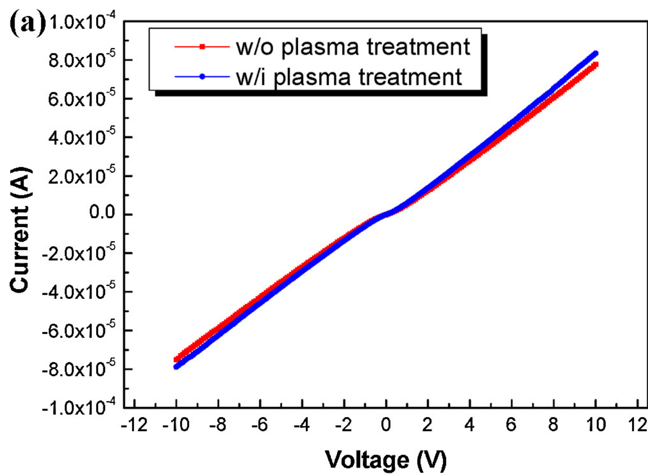


Fig. 1. The schematics of SiGe nanowire surface treatment process (a) the "bare" SiGe nanowire without plasma treatment, (b) the SiGe nanowire with CF4 plasma treatment before Ge condensation by oxidation, (c) the SiGe nanowire with N_2 or NH_3 post-plasma treatment, and (d) the SiGe nanowire was annealed at 800–950 °C and the thermal oxide was removed.

a diluted O_2 gas ambient environment for 3 min. After the Ge condensation by oxidation, the pre-treated SiGe nanowire was treated with N_2 or NH_3 plasma treatment that is displayed in Fig. 1(c). Fig. 1(d) shows a SiGe nanowire that was annealed at 800–950 °C for 180 s in N_2 gas before the thermal oxide was removed. Following Ge condensation and annealing, these nanowires were implanted with 3×10^{15} ions/cm^2 of BF_2 to form p-type nanowires. The final metallization process involved the deposition of a 500 nm-thick layer of aluminum followed by Al sintering at 400 °C. Finally, the electrodes were defined by the mask process. A Hewlett Packard HP 4156A instrument was utilized to measure the electrical characteristics of the nano-wire sensor. The drain voltage (VD) was varied from −10 V to 10 V in steps of 500 mV, and the back gate voltage was fixed at 0 V. The electrical characteristics were measured at each stage of the surface modification, and the mean conductance was then extracted from the ID–VD characteristics with VD = 3–6 V.

3. Results and discussion

Fig. 2(a) plots the *I–V* characteristic of $Si_{0.86}G_{0.14}$ nanowire with/without the plasma treatment. The plasma condition was CF_4/N_2 = 10 s/90 s and the post annealing temperature was 950 °C. The current in plasma-treated sample and the slope of its *I–V* curve of the sample were higher than those of the un-treated nanowire sample. Fig. 2(b) plots the conductance of the SiGe nanowire samples that were shown in Fig. 2(a). The increase in conductance of the plasma-treated sample is caused by the reduction of the density of surface defects by Ge condensation. Hanrath et al. found that [18]; Ge nanowire exhibited p-type behavior; and that Ge tended to accumulate holes at its surface owing to a trapped negative surface charges. Accordingly, the *I–V* curve of the bare SiGe nanowire sample should have had a higher slope than those of the other SiGe nanowire samples. This difference was caused by enhanced surface doping; therefore, the scattering of carriers by ionized impurities and surface scattering are major concerns in relation to conductance variation [11,19]. Fig. 3 plots the effect of post annealing temperature on conductance after plasma treatment. The rate of increase of the conductance with temperature declined with increasing temperature, since the Ge atoms did not diffuse from the SiGe nanowire surface to the LT Si-buffer layer. Ge condensation caused Ge to pile-up at surface of the SiGe nanowire, so the conductance and sensing surface area increased with the Ge fraction.



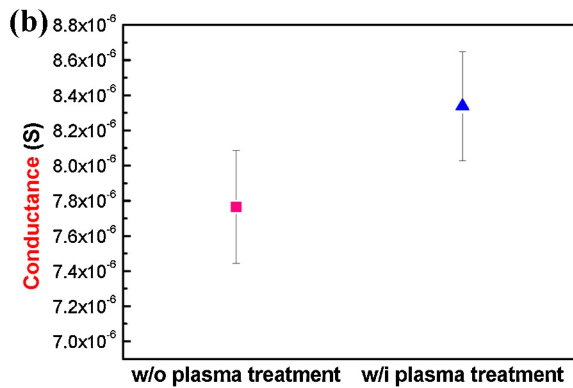


Fig. 2. (a) *I–V* curves of the SiGe nanowires with/without plasma treatment, and (b) the characteristic of conductivity of SiGe nanowires with/without plasma treatment.

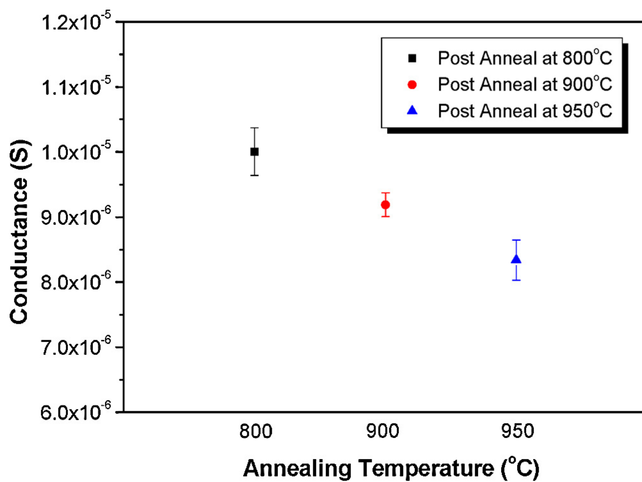


Fig. 3. The characteristic of conductivity of plasma-treated SiGe nanowires are in different post annealing condition.

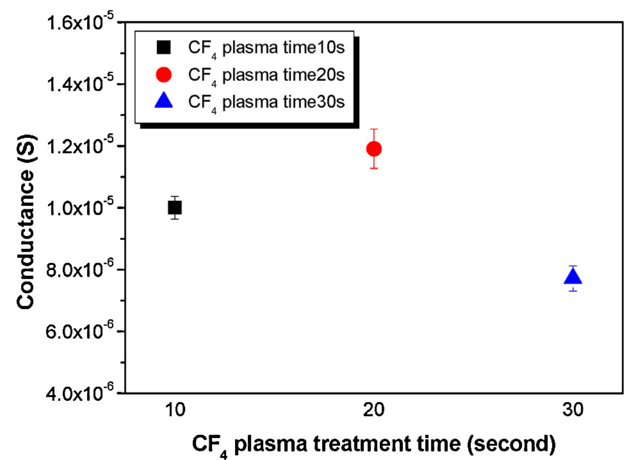
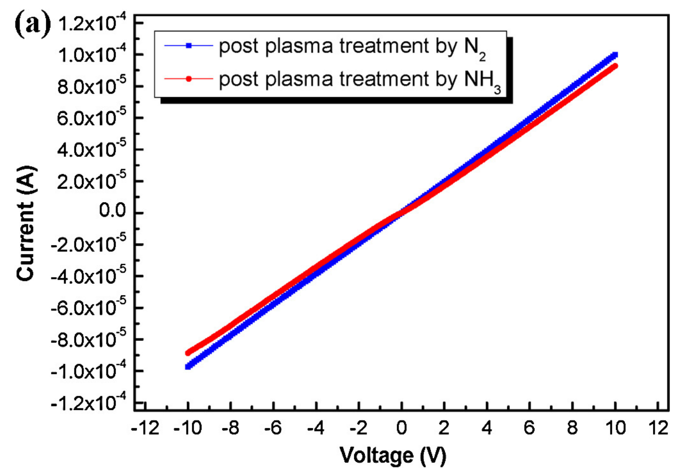


Fig. 4. The characteristic of conductivity of plasma-treated SiGe nanowires are in different CF4 treatment time period.



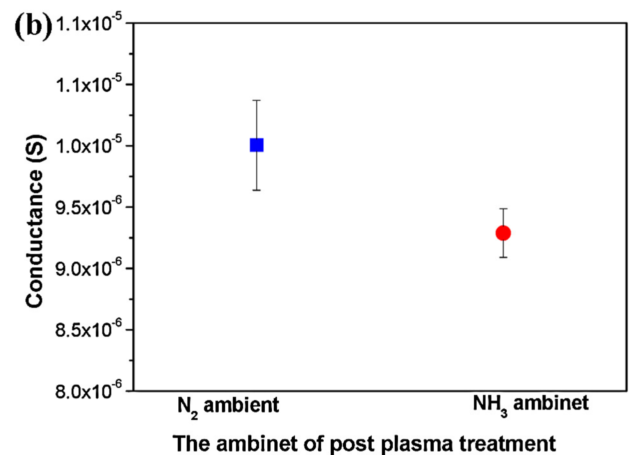


Fig. 5. (a) *I–V* curves of the SiGe nanowires with N_2 or NH_3 plasma post-treatment, and (b) the characteristic of conductivity of SiGe nanowires with N_2 or NH_3 plasma post-treatment.

Therefore, high temperature annealing results in Ge re-distribution and diffusion from the sensing surface. Fig. 4 plots the variation of the conductance of SiGe nanowires with period of treatment by CF_4 plasma at post annealing temperature of 800 °C. A treatment time of 20 s yielded a peak value conductance. When the treatment period was 10 s, it assumed that the F atoms were a few to repair the surface defects on SiGe nanowire; treatment period was 30 s, the conductance was degraded by plasma-induced damage [20,21]. Fig. 5(a) plots the *I–V* characteristics of SiGe nanowire that underwent post-plasma treatment in various ambient. The sample that underwent N_2 plasma treatment had a greater conduction current than sample that was treated with NH_3 plasma. Fig. 5(b) compares the conductance of the nanowires that are described in Fig. 5(a). The N_2-treated sample has the higher conductance because it incorporates more N atoms than the NH_3-treated sample. Weak Si–H bonds are easily broken in the following annealing process at high temperature, casing the dangling bonds to reappear. In the NH_3-treated sample, these dangling bonds trap the conduction carriers

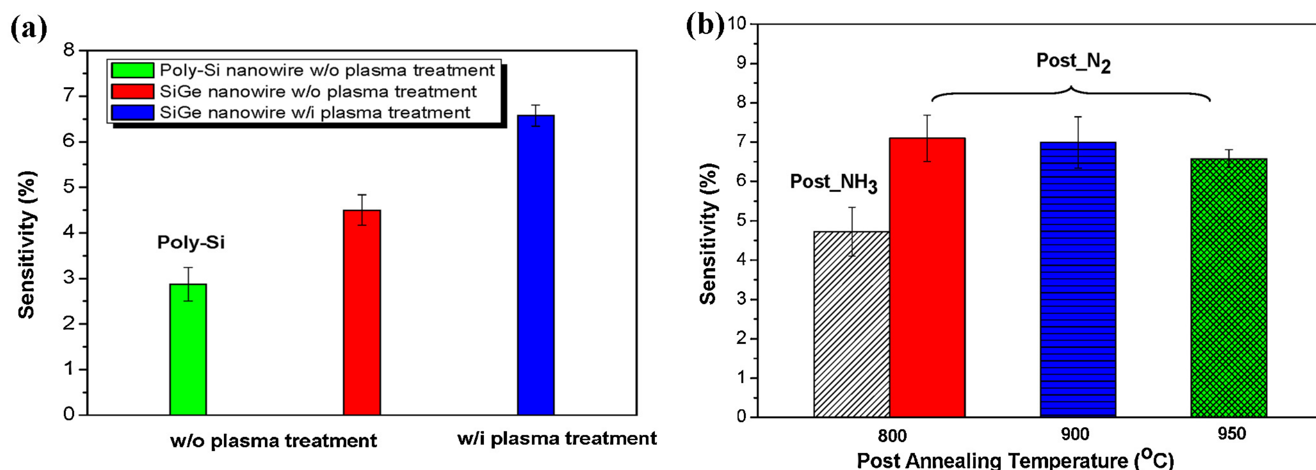


Fig. 6. The characteristic of sensitivity of nanowires when APTMS was dripped onto its surface (a) the comparison of sensitivity is between poly-Si nanowire; unplasma-treated SiGe nanowire are, and plasma-treated SiGe nanowire, (b) the comparison of sensitivity in different pre-plasma and post-plasma treatment condition.

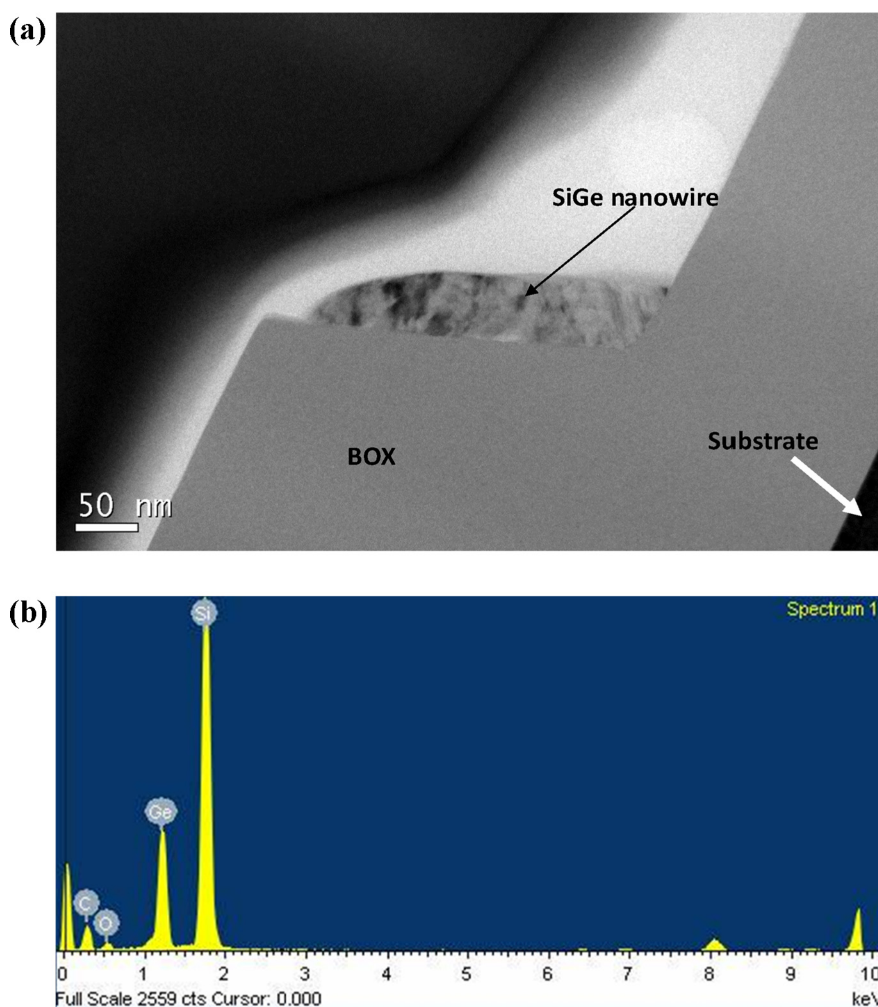


Fig. 7. (a) The TEM image of SiGe nanowires after oxidation which oxide layer on SiGe nanowire was stripped, and (b) the EDAX at surface of SiGe nanowire after oxidation.

are trapped in n-type traps [22–25], reducing its conductance. The conductance varied with the plasma treatment conditions and sensitivity of the SiGe nanowire may also have varied in a manner similar to the conductance. The nanowires samples were functionalized using 3-aminopropyltri-ethoxysilance (APTMS) to modify the silicon oxide surfaces that surrounded the nanowires. Each hydroxyl functional group on the oxide surface was replaced by methoxy groups of APTMS modules, while the nanowire surfaces were simultaneously terminated by amine groups. The conductance of the nanowire decreased when APTMS was dripped onto its surface. APTMS was prone to become positively charged, as reflected by the decrease in conductance when hole carriers were

depleted from the surface of the p-type nanowire [26].The sensitivity (S) of a nanowire-based sensor was defined as the ratio of the magnitude of the change in conductance to the baseline conductance:

$$S = \frac{|G - G_0|}{G_0} = \frac{\Delta G}{G_0}, \quad (1)$$

where G_0 denotes the conductance before capture of a molecule; G is the conductance following capture of a molecule, and ΔG is the difference between G and G_0. Fig. 6(a) displays the sensitivity of the SiGe nanowire with/without plasma treatment when APTMS was dripped onto nanowire's surface and that of the traditional poly-Si nanowire, which was fabricated as a control sample. The SiGe nanowire samples were more sensitive than the poly-Si nanowire because the strained-Si material enhanced the hole mobility [5,26]. The sensitivity exhibits the same trend as in Fig. 2; so the SiGe nanowire with larger conductance has greater sensitivity. Fig. 6(b) plots the variation of sensitivity with both by the post-plasma treatment ambient species and the post-annealing temperature. The sample that underwent N_2 post-plasma treatment and post annealed at 800 °C had greater percentage of sensitivity than the other nanowire samples. This result is consistent with the characteristics plotted from Figs. 3–5. Fig. 7(a) displays the TEM cross-section of SiGe nanowires. The average width of the nanowires after oxidation is 80 nm. Fig. 7(b) presents the EDAX at the surface of a SiGe nanowire following oxidation. The fraction of Ge in the oxidized nanowire is 18.25%, which is approximately 4.73% higher than that 13.52%, in the un-oxidized SiGe nanowire.

4. Conclusions

This study examined various methods for increasing the conductance of SiGe nanowires in the Ge condensation process. Fluorine plasma treatment efficiently improved the conductance and enhanced the sensitivity of SiGe nanowires because the high Si–F binding energy creates a more stable interface state than bare nanowire sample on the surface of SiGe. F atoms can eliminate the dangling bonds in the Ge condensation process and improve the conductance of the nanowires. The period of CF_4 plasma treatment can be controlled to prevent the reappearance of defects by plasma damage and consequent reducing of the conductivity of the SiGe nanowire. Post-plasma treatment in N_2 ambient is better than that in NH_3 because the H atoms are more easily dissolved by the subsequent high temperature annealing. Weak Si–H bonds are easily broken in the following annealing process at high temperature, casing the dangling bonds to reappear. The temperature of post-annealing can also be controlled to improve conductivity and sensitivity. A lower annealing temperature can prevent Ge redistribution. If Ge diffuses away from the surface of a SiGe nanowire where most sensing occurs and diffuses into the amorphous Si/buried oxide interface, then conductivity and sensitivity are reduced.

Acknowledgments

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