Enhancing the Performance of Germanium Channel nMOSFET Using Phosphorus Dopant Segregation

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***Abstract*—In this letter, we present a high performance Ge n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) with a NiGe Schottky junction source/drain fabricated using phosphorus dopant segregation. Phosphorus atoms were implanted into NiGe and then driven toward the NiGe/p-Ge interface to depin the Fermi level and form a Schottky junction. A high effective barrier height (Φ_{Bp}) of 0.57 eV, resulting in a high junction current ratio of >10^4 at the applied voltage $|V_a| = \pm 1$ V. The nMOSFET exhibited a high I_{ON}/I_{OFF} ratio of ~8×10^3 (I_D), ~10^5 (I_S), and a subthreshold swing of 138 mV/decade. The nMOSFET developed in this letter exhibited greater transconductance and a drain leakage current that is more than two orders of magnitude lower compared with nMOSFETs with the conventional n^+/p junction.**

***Index Terms*—Shottky barrier height, dopant segregation, NiGe, nMOSFET.**

I. Introduction

GERMANIUM (Ge) channel devices have been regarded as a replacement for Si channel metal-oxide-semiconductor field-effect transistors (MOSFETs) because Ge has a high carrier mobility [1], [2]. Although the high performance Ge p-channel MOSFETs has been demonstrated [3], [4], fabricating high performance Ge n-channel MOSFETs remains extremely challenging because n-type dopants diffuse rapidly and have relatively low solid solubility [5], [6]. Moreover, n-type dopants, even with a high activation temperature, have been reported to exhibit a poor activation efficiency [7]–[9], making the formation of a S/D with adequately low resistance very difficult. A possible solution is to use a Schottky junction S/D (or metal S/D) to replace the conventional n^+/p junction S/D. By using a phosphorus dopant segregation (DS) technique, the NiGe/p-Ge junction can be changed from an ohmic contact to a Schottky contact. Recently, many elements from group V, including phosphorus, arsenic, and antimony, have been proven to modulate the Schottky barrier height (SBH) of NiGe/Ge [10]–[13] because they segregate at the interface. Li *et al*. successfully fabricated a NiGe/p-Ge Schottky diode with a low electron SBH of 0.1 eV by implanting phosphorus after NiGe formation [12]. Koike *et al*. induced phosphorus atoms in the NiGe/p-Ge to tune the SBH [13]. Even though the underlying mechanism for the modulation of the SBH value has been intensively discussed [10]–[13], the fabrication of high performance nMOSFETs with a Schottky junction S/D by using a DS technique has not yet been demonstrated in the literatures.

In this letter, a high performance Ge nMOSFETs with a NiGe/p-Ge Schottky junction S/D was fabricated using a phosphorus DS technique. The resultant high effective barrier height (Φ_{Bp}) led to a considerably low leakage current in the devices. High I_{ON}/I_{OFF} ratio and good SS were achieved. Therefore, using this approach greatly improved the electrical characteristics of Ge channel nMOSFETs.

II. Device Fabrication

A 400 nm plasma enhanced chemical vapor deposition (PECVD) isolation oxide was deposited on a p-Ge (100) substrate with a resistivity of 0.1-0.6 ohm-cm after cleaning. The S/D pattern was defined by using photolithography, and the subsequent oxide etch was accomplished by using a buffer oxide etchant. Nickel was deposited by sputtering, and a lift-off process was performed; rapid thermal annealing (RTA) at 200 °C for 60 s was used to form the NiGe alloy as the metal S/D of the nMOSFET. The phosphorus dopants (10 keV, 1×10^{15} cm^{-2}) were then implanted in the metal S/D regions. The dopants segregated at the NiGe/p-Ge interface when they were activated using RTA at 500 °C for 60 s. Moreover, an interesting approach often referred to as the snowplow effect, or the pile-up of phosphorus dopants, has been verified by using a secondary ion mass spectrometry (SIMS) depth profile [10]–[12], [14]. A GeO_2 was used as a surface passivation layer using rapid thermal oxidation (RTO) at 520 °C for 30 s and then an Al_2O_3 deposition was performed by atomic layer deposition (ALD) after the active area was defined. Finally, the Al (400 nm) gate and the metallization contact were established by using an evaporator.

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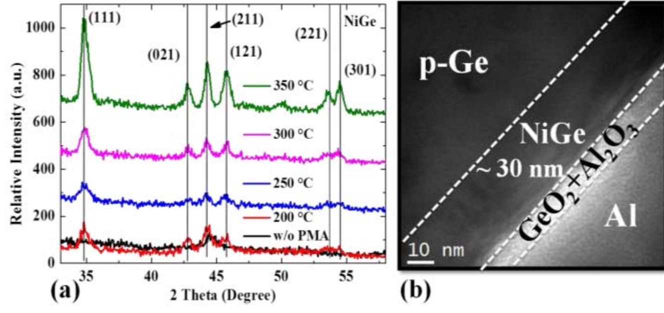

Fig. 1. (a) GIXRD spectra of NiGe films with various annealing temperatures. (b) TEM picture of gate-to-drain overlapping region of nMOSFET device; gate stack and NiGe/p-Ge junction are shown.

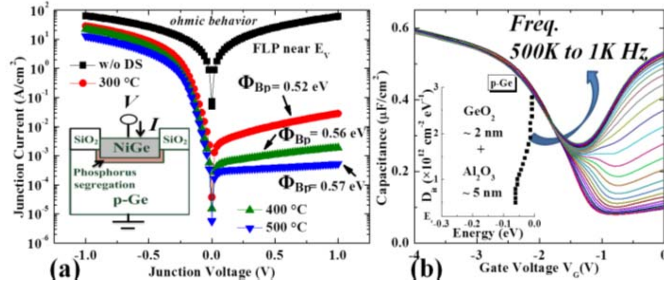

Fig. 2. (a) I–V characteristics of NiGe/p–Ge diodes with/without phosphorus DS with different annealing temperatures. The inset is the schematic illustration of junction cross section. (b) C–V characteristics of Al/Al_2O_3/GeO_2/p-Ge structure and D_{it} distribution near the Ge midgap (inset).

nMOSFETs with the conventional n^+/p junction S/D were also accomplished for comparison.

III. Results and Discussion

Fig. 1(a) shows the grazing incidence X-ray diffraction (GIXRD) spectra recorded at various annealing temperatures used for verifying NiGe formation. The peaks corresponding to (111), (021), (211), (121), (221), and (301) NiGe were clearly identified. Ni/n-Ge test Schottky junctions were also employed to determine the optimal PMA conditions (not shown). Performing RTA at 200 °C for 60 s was sufficient to form the NiGe phase. The transmission electron microscopy (TEM) image of the gate-to-drain overlapping region of the nMOSFET is shown in Fig. 1(b). The thickness of the NiGe film and that of the $GeO_2+Al_2O_3$ were around 30 nm and 7 nm, respectively; the device structure is shown in the inset of Fig. 3(a).

Fig. 2(a) shows the I–V characteristics of the NiGe/p–Ge contacts fabricated using different annealing temperatures (300 °C, 400 °C, and 500 °C) with and without phosphorus DS. It was clear that the control sample without DS exhibited ohmic contact behavior caused by the strong Fermi level pinning (FLP) near the valence band and the resultant low Φ_{Bp}. Rectifying behavior was obtained by implanting phosphorus dopants into NiGe and subsequently conducting RTA. Phosphorus atoms are segregate near the NiGe/p-Ge interface when using RTA. The highest value of the effective Φ_{Bp} extracted from the I–V characteristics [15] was ~0.57 eV, which was

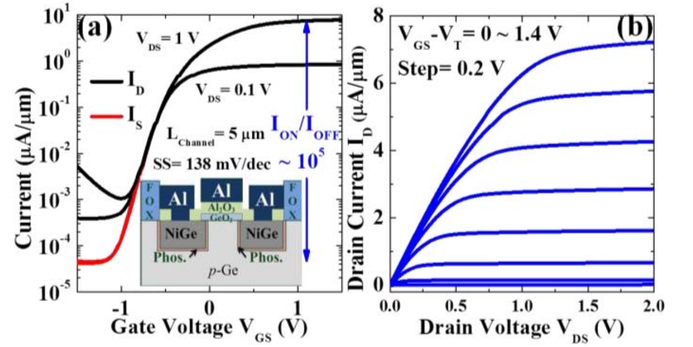

Fig. 3. (a) Transfer characteristics of Ge nMOSFET with a NiGe Schottky junction S/D and the I_{ON}/I_{OFF} ratio is of $\sim 10^5\,(I_S)$. Schematic diagram of device structure (inset). (b) I_D-V_{DS} output characteristic of device and the saturation current is of 4 μA/μm at V_{DS} = 1V and V_{GS}-V_T = 1V.

beneficial in restraining the reverse leakage current of the Schottky junction. Fig. 2(b) shows the C–V characteristics of metal-oxide-semiconductor (MOS) capacitor used to examine the surface interface state density (D_{it}) of the Al_2O_3/GeO_2/p-Ge stack; the inset shows the extracted D_{it} distribution near the Ge midgap obtained using a conductance method at room temperature [15]. Based on analyzing the C–V curves, a small hump was observed in the weak inversion as the measuring frequency decreased. The voltage for the hump corresponded to that at which the peak conductance of the G-V curves (not shown) happens; the peak conductance arose from generation-recombination through D_{it} [16]. The estimated D_{it} value is of $\sim 3 \times 10^{12}$ $cm^{-2}eV^{-1}$ near the Ge mid-gap and the C–V hysteresis width is of around 200 mV.

Fig. 3(a) shows the I_D-V_G transfer characteristics of the Ge nMOSFET with a NiGe Schottky junction S/D in the linear region at V_{DS} = 0.1 V and saturation region at V_{DS} = 1 V. The schematic cross-sectional view of the device with an $L_{Channel}$ of 5 μm is shown in the inset of Fig. 3(a). A high I_{ON}/I_{OFF} ratio of $\sim 10^5\,(I_S)$, $\sim 8 \times 10^3\,(I_D)$ at V_{DS} = 1 V, and a good subthreshold swing of 138 mV/dec are illustrated. A driving current of 7.3 μA/μm at V_{GS}-V_T = 1.3 V and a low drain leakage current of ~1 nA/μm at V_{GS}-V_T = −0.7 V were attributed to the thin tunnel barrier for electrons and a high effective $\Phi_{Bp} \sim 0.57$ eV for holes, respectively. A peak mobility ~440 cm^2/V-s was extracted by split C–V (not shown). Recently, numerous articles focusing on the Ge nMOSFETs with the conventional n^+/p junction S/D have been published. Fu *et al* [17] reported a Ge nMOSFET (S.S. = 150 mV/dec) with a source current I_{ON}/I_{OFF} ratio $\sim 2 \times 10^4$ at V_D = 1 V, in which the I_{ON} was ~3 μA/μm at V_G = 1.5 V. Zhang *et al* [18] reported a Ge nMOSFET on a (100) wafer with a poor drain current I_{ON}/I_{OFF} $\sim 10^2$ at V_D = 1 V and a high drain leakage current of >10 nA/μm at V_G = −1 V. Lee *et al* [19] presented a Ge nMOSFET on a (111) plane with a driving current of ~4 μA/μm at V_G = 1.5 V and V_D = 1 V and a drain current I_{ON}/I_{OFF} ratio of $\sim 2 \times 10^3$ even though the equivalent oxide thickness (EOT) was reported in sub-nanometer. Compared with the former results [17]–[19], the Ge nMOSFET with a NiGe Schottky S/D fabricated in this letter exhibited a

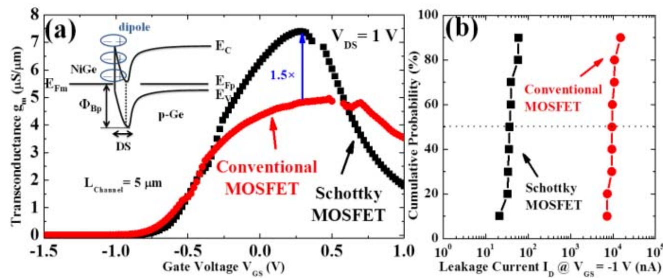

Fig. 4. (a) g_m versus V_{GS} characteristic of nMOSFET with a Schottky S/D and conventional S/D at $V_{DS} = 1$ V and the inset shows the speculative band diagram of NiGe/p-Ge with DS in thermal equilibrium. (b) Cumulative plot versus drain leakage current of nMOSFETs at $V_{GS} = -1$ V.

superior performance regarding the I_{ON}/I_{OFF} ratio, and the SS. Fig. 3(b) shows the I_D-V_{DS} output characteristics of the Ge nMOSFET; the saturation current of the device was 4 μA/μm at V_{DS} and V_{GS}-V_T = 1V. In previous studies [20], [21], numerous methods have been proposed for improving the S/D series resistance of nMOSFETs to enhance the driving current; however, the devices with a Schottky junction S/D shows the highest output current [20], [21]. In addition, a nMOSFET with a conventional n^+/p junction S/D and NiGe contact was fabricated for comparison. The transconductance (g_m) versus gate voltages is shown in Fig. 4(a). The peak g_m value of the Schottky MOSFET was around 1.5 times higher than that of the conventional MOSFET at V_{DS} = 1 V. Because the phosphorus dopants were segregated near the NiGe/p-Ge interface, the combined effects of the surface dipoles and the band bending were determined to modulate the electron tunneling barrier; the speculated band diagram in thermal equilibrium is shown in the inset of Fig. 4(a). On the other hand, the hole effective SBH (∼0.57 eV) can also be modulated by the dopants, which leads to the considerably suppressed hole current (leakage current) in the off state. Fig. 4(b) shows the cumulative plot of the drain leakage current at $V_{GS} = -1$ V; the leakage current of the SBH MOSFET is at least two orders of magnitude lower than that of the conventional MOSFET. The narrow distribution of the low leakage current indicates that the DS process is extremely stable. As a result, a high performance Ge nMOSFET with NiGe S/D was demonstrated; the DS technique was employed to alleviate the FLP effect and an ohmic contact was successfully changed to a Schottky contact, which resulted in a low leakage current.

IV. Conclusion

In conclusion, a high performance Ge nMOSFET with a NiGe Schottky junction S/D was fabricated using the DS technique. The device exhibited a high I_{ON}/I_{OFF} ratio of $\sim 10^5$ (source current), and a SS of 138 mV/dec. The high driving current of 7.3 μA/μm at V_{GS}-V_T = 1.3 V and low drain leakage current of ∼1 nA/μm at V_{GS}-V_T = −0.7 V were attributed to the thin tunnel barrier for electrons and the high effective SBH for holes, respectively. Moreover, the study shows that the performance of the Ge nMOSFET with a NiGe Schottky S/D is superior to that of a conventional device. Finally, the results indicate that this high performance Ge nMOSFET with a NiGe Schottky S/D can be applied in Ge CMOS realization.

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