# Body-Tied Germanium Tri-Gate Junctionless PMOSFET With *In-Situ* Boron Doped Channel

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***Abstract*— In this letter, we demonstrate body-tied Ge tri-gate junctionless (JL) p-channel MOSFETs directly on Si. Our tri-gate JL-PFET exhibits higher current than the conventional inversion-mode transistor through *in-situ* heavily doped technique and trimming down Ge fin width. We show that the JL-PFET with tri-gate structure has excellent $I_{ON}/I_{OFF}$ ratio and good short channel effect control on the channel potential. The current ratio is of $\sim 6 \times 10^3$ ($I_D$) at $V_{DS} = -0.1$ V, $V_{GS} = -3$, and 0 V. The relatively low OFF-current is of 6 nA/ $\mu$m at $V_{DS} = -0.1$ V and $V_{GS} = 0$ V. The subthreshold swing of 203 mV/decade and drain induced barrier lowering of 220 mV/V are reported at $L_G = 120$ nm.**

***Index Terms*— Junctionless, tri-gate, germanium, body-tied, in-situ heavily doped.**

## I. Introduction

GERMANIUM has been reported to be one of the candidates for replacing Si to continuously enhance the circuit performance [1]. A higher permittivity of Ge than that of Si leads to more severe SCE. To meet the pressing requirement of the channel potential control, non-planar structures have been suggested to the fabrication of Ge MOSFETs. Germanium FinFETs have been fabricated successfully on the Si substrate [2]–[3]. However, the degradation in current ratio for the short channel devices was observed. Junctionless device possesses the same doping type of channel and S/D, which is essentially an accumulation-mode device. It is like a resistor and the amount of mobile majority carriers can be modulated by the bias on the gate electrode. The ON state current comes from the majority carrier conduction already existing in the channel; while the OFF state is achieved by depleting the majority carriers through the work function difference between the gate electrode and semiconductor. Recently, the long channel planar Ge junctionless PMOSFET using double-gate structure on GeOI (Germanium on insulator) substrate has been reported [4]–[5]. Obviously, the driving current and subthreshold characteristics of their device were poor and needed to be further improved. In addition, the non-planar Ge junctionless nanowire transistors fabricated on GeOI wafers have been reported [6]–[7]. As known, the non-planar structure is very attractive from the viewpoint of gate control.

In this letter, we fabricate the Ge multi-fin junctionless PMOSFET with tri-gate structure integrated on the bulk Si platform. The device illustrates a low off current ($I_{OFF}$) of 6 $n$A/$\mu$m at $V_{GS} = 0$ V and $V_{DS} = -0.1$ V. Furthermore, an excellent $I_{ON}/I_{OFF}$ drain current ratio of $\sim 6 \times 10^3$ at $V_{DS} = -0.1$ V, $V_{GS} = -3$ and 0 V. The good subthreshold characteristics (S.S. = 203 $m$V/dec, DIBL = 220 $m$V/V) are obtained.

## II. Device Fabrication

An in-situ heavily boron doped Ge film via $B_2H_6$ source was epitaxially grown on the bulk n (2∼7 ohm-cm)-Si(100) substrate using an rapid thermal chemical vapor deposition (RTCVD) system after a standard cleaning. Threading dislocation density was improved by the post Ge deposition annealing of 825 °C for 10 minutes in a high vacuum ambient. The multi-fin structure was formed by using reactive ion etching (RIE) after the pattern was defined by e-beam lithography. We performed a wet trimming process with a chemical solution of $H_2O_2$: $H_2O$ = 1 : 10 at room temperature for 45 s to eliminate thin amorphized Ge residual layer without causing additional plasma damage and shrink down fin width to be 15∼20 nm. This is a key process for scaling down of device dimension. Spin on glass (SOG) as the device isolation was coated and etched back by the dilute buffered oxide etch (BOE). A $GeO_2$ (at 520°C for 30s) surface passivation using rapid thermal oxidation (RTO) and then a 5 nm ALD $Al_2O_3$ dielectric deposition were carried out. A metal gate Ti (5 nm)/Pt (100 nm) was deposited by sputtering. NiGe contacts were accomplished by post metal annealing (PMA) at 200 °C for 1 min. Finally, forming gas annealing (FGA) at 300 °C 30 min was performed. In this way, the simple and Si process compatible body-tied Ge tri-gate JL MOSFET devices were fabricated.

## III. Results and Discussion

Fig. 1(a) shows the schematic diagram of the structure of tri-gate Ge JL-PFET with ISHD channel. Majority carriers (holes) can be effectively depleted by the voltage on the multiple gates

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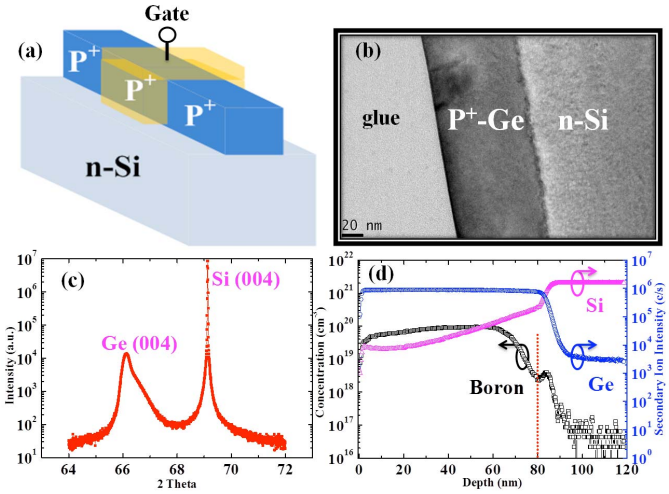


Fig. 1. (a) Schematic diagram of tri-gate Ge junctionless p-channel MOSFET device on bulk Si. (b) Cross-sectional TEM image of $p^+$-Ge film on n-Si using in-situ heavily doped epitaxy. The dislocation density is quite low. (c) XRD pattern of $p^+$-Ge film on n-Si. (d) SIMS depth profile of boron dopant and the red line indicates the thickness of epi-Ge layer.

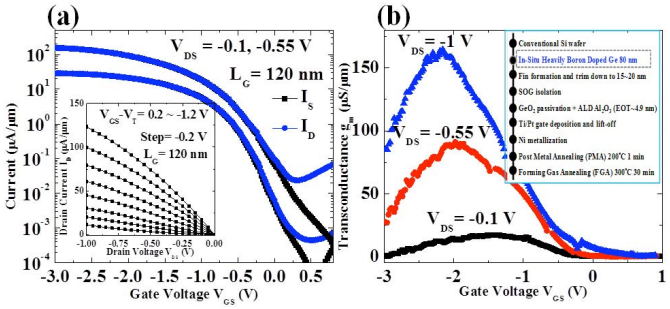


Fig. 2. (a) Transfer characteristic of Ge JL-PFET with a $L_G$ of 120 nm and the $I_{ON}/I_{OFF}$ ratio is $\sim 6\times10^3$ ($I_D$) at $V_{DS} = -0.1$ V,$V_{GS} = -3$ and 0 V. $I_D$-$V_{DS}$ output characteristic (inset). (b) $g_m$ versus $V_{GS}$ characteristics at $V_{DS} = -0.1$ V, $V_{DS} = -0.55$ V, and $V_{DS} = -1$ V. Fabrication process flow of Ge JL-PFET (inset).

for achieving the off-state. Fig. 1(b) shows the cross-sectional TEM image of uniformly epitaxial $p^+$-Ge (~80 nm) film on the n-Si substrate. The dislocation density is estimated to be $5\times\ 10^6\sim10^7$ $cm^{-2}$ as measured on the thicker Ge sample. The single crystalline $p^+$-Ge thin film was confirmed through XRD pattern (or rocking curve), as shown in Fig. 1(c). Moreover, the ISHD technique can reduce the thermal budget and result in shallower dopant distribution as compared with the implantation process. Fig. 1(d) shows the secondary ion mass spectrometry (SIMS) profile of $p^+$-Ge on n-Si using ISHD and boron concentration is observed to be $\sim1\times\ 10^{20}\,cm^{-3}$. More importantly, the significant suppression of boron doping tail and the resultant deep dopant distribution, observed in the conventional implantation scheme [8], is demonstrated. In other words, the ISHD prevails in the formation of shallow junction.

Fig. 2(a) shows the transfer characteristic of Ge multi-fin JL device with $L_G$ of 120 nm and the inset is the output characteristic. The device shows a high $I_{ON}/I_{OFF}$ ratio of $\sim6\times10^3$ ($I_D$) at $V_{DS} = -0.1$ V,$V_{GS} = -3$ and 0 V. The S.S. is of 203 $m$V/dec and the DIBL of 220 $m$V/V. The total effective channel width $W_{Eff} = 5\ \times(2\times\ H_{Fin}+ W_{Fin})$ of multi-fin device is equal to ~900 nm. Drain current ($I_{DS}$) and transconductance ($g_m$) are normalized by the effective total channel width. Recently, the reported current ratio was only a little bit more than $10^4$ at $V_{DS} = -50$ mV ($L_G = 230$ nm) in a study of IM-PFET using the Ω-gate structure with NiGe metal source/drain on the GOI substrate [9]. The minimum off-state leakage current was $\sim1nA/\mu m$ at $V_G = 1$ V, which is obviously worse than ours (~450 $pA/\mu m$ at $V_G = 0.5$ V). A Ge IM p-channel FinFET using aspect-ratio-trap scheme has been published last year [10], showing a ratio of $\sim 10^4$ at $V_{DS} = -50$ mV ($L_G = 110$ nm). Another IM device with strained Ge nanowire and metal S/D structure has been published last year [11], exhibiting a ratio of $<10^3$ ($L_G = 65$ nm) and a parasitic resistance of $\sim1.3$ k$\Omega\times\mu$m at $V_{DS} = -50$ mV. Moreover, for our Ge multi-fin IM-PFET on the Si substrate, a poor current ratio of $\sim\ 2\times10^3$ has been reported based on the standard gate-last process [3]. The value of threshold voltage $V_T$ >0 needed to be adjusted for the CMOS inverter application. Clearly, the present JL device depicts much higher current ratio and more appropriate $V_T$ value (-0.6 V) than our former IM device [3]. The relatively low off-state leakage current is attributed to the effectively depleted channel because the fins in the structure are sufficiently narrow. For the planar JL device [4]–[5], the stringent requirement of ultra thin channel brings out the difficulty of process control as well as the surface roughness issue. Theoretically [12], the fin width ($W_{Fin}$) should be smaller than twice the depletion width ($W_{dep}$), that is $W_{Fin} <2W_{dep}$, to effectively turn off the current at off-state in a tri-gate structure. In other words, the non-planar JL device with multiple gates is more suitable than the planar JL device; the resultant driving current of the non-planar JL device is supposed to be larger due to the larger effective channel width at the current level. The output characteristic exhibits a relatively high saturation current of 100 $\mu A/\mu m$ at $V_{GS}$-$V_T = -1$ V and $V_{DS} = -1$ V. Our JL device shows much higher saturation current than IM device [3]. The transconductance ($g_m$) characteristics are shown in Fig. 2(b) and process flow (inset); the peak value of $g_m$ at $V_{DS} = -1$ V is much larger than that of the IM device at $V_{DS} = -0.95$ V in the early report [13] using in-situ doped raised S/D technique on GOI substrate. We can see that the $g_m$ value increases significantly as the high drain voltage increases, indicating a relatively low S/D resistance in our device. Fig. 3(a) shows the output characteristics of JL and IM devices with longer channel length ($L_G = 1\ \mu m$) in order to compare the channel resistance between two devices, especially in the linear region. The cross-sectional TEM image of Ge tri-gate PMOSFET device is shown in the inset of Fig. 3(a). It is clear that there is around two times in output current of JL device at $V_{DS} = -1$ V and overdrive voltage equal to $-1$ V. Total resistances $R_{Total}$ of JL and IM device as a function of gate voltage at $V_{DS} = -0.1$ V are shown in Fig. 3(b). The width of Ge single fin is around 18.4 nm, as shown in the inset of Fig. 3(b). The relationship between

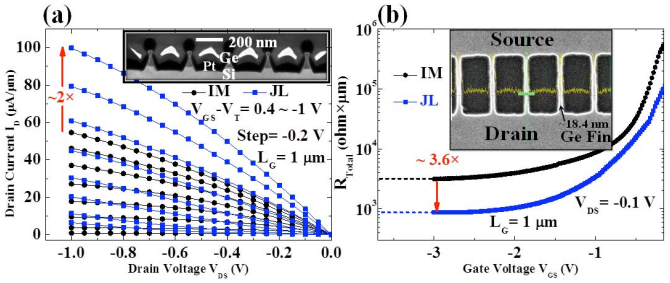


Fig. 3. (a) $I_D$-$V_{DS}$ output characteristics of JL and IM devices with $L_G$ = 1 $\mu$m and cross-sectional TEM of Ge tri-gate PMOSFET (inset). JL shows better output current is around two times higher than that IM. (b) Total resistance of JL and IM devices as a function of gate voltage, showing around 3.6 times reduction than IM. Inset is top-view SEM picture after wet trimming process (Ge fin width ~18.4 nm).

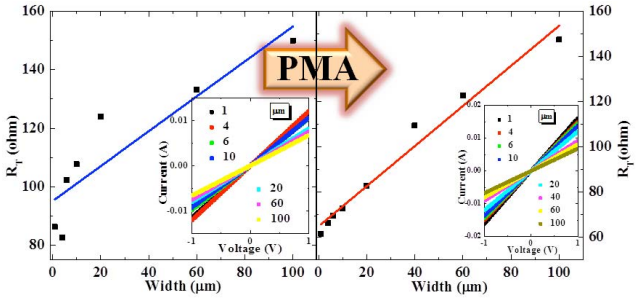


Fig. 4. Total resistance versus width before (left) and after (right) PMA for JL-PFET. Inset is $I-V$ plot.

the S/D series resistance ($R_{SD}$) and the $R_{Total}$ is described by [14]

$$R_{Total} = R_{ch} + R_{SD} = \frac{L_G}{W_{eff}\mu_{eff}C_{OX}(V_{GS}-V_T)} + R_{SD} \quad (1)$$

where $R_{ch}$ is the channel resistance, $W_{eff}$ is the effective channel width, $\mu_{eff}$ is the effective mobility, and $C_{OX}$ is the oxide capacitance. The $R_{SD}$ of JL device is around 870 $\Omega\times\mu$m using ISHD technique, which is around 3.6 times reduction as compared to that of the IM device at $V_{GS} = -3$ V. Moreover, the $R_{SD}$ value of our JL device is around 2.8 times lower than IM device in the work with in-situ boron doped S/D [13]. The transfer length method (TLM) was applied to extract the values of contact resistance ($R_C$) and sheet resistance ($R_{sh}$). The total resistances of Ni/$p^+$-Ge are plotted versus contact width before PMA (left) and after PMA (right); the $I$-$V$ curves are shown in the inset of Fig. 4. The contact resistance is of 33 $\Omega$ with 30 % reduction and the sheet resistance is of 27 $\Omega$ after PMA treatment. We think this reduction arises from the formation of NiGe. According to our experimental results, we suggest that the Ge non-planar JL-PFETs directly on the bulk Si is very attractive from the viewpoint of process complexity and low cost for the future high performance circuits.

## IV. Conclusion

Body-tied Ge multi-fin tri-gate JL-PFETs of $L_G$ down to 120 nm directly on the bulk Si substrate have been demonstrated. Trimming down the fin width to 15~20 nm is sufficient to turn off the JL device which possesses excellent current ratio and good subthreshold characteristics. Our JL-PFETs show higher driving current than the IM-PFETs and depicts much better performance than the planar JL-PFET [4]. We think our work demonstrates the potential of easily fabricated non-planar Ge JL MOSFET on the Si substrate for the future high performance low power logic applications.

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