Low-Leakage-Current DRAM-Like Memory Using a One-Transistor Ferroelectric MOSFET With a Hf-Based Gate Dielectric

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***Abstract*— The power consumption of capacitor leakage current, increase of the capacitor aspect ratio, and lack of higher dielectric constant (κ) material are the difficult challenges to downscaling dynamic random access memory (DRAM). This letter reports a new one-transistor ferroelectric-MOSFET (1T FeMOS) device that displays DRAM functions of a 5 ns switching time, 10^{12} on/off endurance cycles, and 30 times on/off retention windows at 5 s and 85 °C. A simple 1T process and a considerably low OFF-state leakage of 3 × 10^{-12} A/μm were achieved. This novel device was achieved by applying ferroelectric ZrHfO gate dielectric to a p-MOSFET, which is fully compatible with existing high-κ CMOS processing.**

***Index Terms*— Ferroelectric, ZrHfO, 1T, DRAM, FeMOS, MOSFET, memory.**

I. Introduction

THE search for higher dielectric constant (κ) material is the difficult challenge for dynamic random access memory (DRAM) [1]–[5]. Although $SrTiO_3$ is promising because it contains a $\kappa > 100$, the dielectric thickness of the low metal/insulator barrier height (φ_b) must be increased to lower the leakage current [2]. This is the fundamental material-related problem of high-κ dielectric materials, of which the φ_b decreases as the κ value increases. Nevertheless, the relatively large thickness is difficult to fill into the smaller footprint of the DRAM capacitor. Therefore, increasing the capacitor height is one solution to continuous downscaling of the planar size of DRAM cell, but the increased aspect ratio increases the difficulty of fabricating the DRAM capacitor. Furthermore, the power consumption from the capacitor's leakage current is a crucial concern of multi-Gb DRAM, which account for a substantial amount of the total power consumption of a system [6]. Therefore, a novel DRAM-like device with a low leakage current and improved power consumption must be invented.

However, this new memory device must satisfy the benchmarks of a sufficiently large memory window, high endurance, a long data retention time with an improved refresh cycle, a fast switching speed, and a simple, inexpensive process for both commodity and embedded applications, to compete with existing DRAM.

In this letter, we present a DRAM-like one-transistor ferroelectric MOSFET (1T FeMOS) device with superior DRAM functions using a simpler capacitor-less 1T structure and a very lower off-current (3 × 10^{-12} A/μm) than those of existing DRAM devices, in addition to a 5 ns switching time and 10^{12} on/off endurance cycles. This low-power green device with DRAM functions was achieved using a p-MOSFET by applying a ferroelectric effect [7]–[10] to a thin high-κ ZrHfO gate dielectric. This Hf-based ferroelectric FeMOS has the extra merit of full process compatibility with a sub-32nm high-κ CMOS [11]–[14], which is distinct from conventional non-Hf-based ferroelectric gate dielectric MOSFETs using $Pb(Zr,Ti)O_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT), and $Bi_{3.75}La_{0.25}Ti_3O_{12}$ (BLT) [7]–[9]. The process compatibility using Hf-based ferroelectric dielectric is the enabling technology to realize the 1T FeMOS proposed as early as 1999 [15].

II. Experiments

The self-aligned, gate-first TaN/ZrHfO/SiO_2 p−MOSFETs were fabricated on standard n-type Si substrates. A thin 3-nm SiO_2 was grown on n-type Si substrate. Then ∼30-nm high-κ ZrHfO was deposited by physical vapor deposition (PVD), and followed by 400 °C post-deposition annealing. A Zr/Hf ratio of ∼1 was used to reach the largest polarization and hysteresis [10]. The TaN metal-gate was then deposited by PVD and patterned. The self-aligned B^+ ions were then implanted and activated by rapid thermal annealing (RTA) at 950 °C. After opening the contact window at source-drain region, the contact was formed by Al metal deposition, patterning, and annealing at 350 °C. The fabricated p-MOSFETs have a gate length and width of 10-μm and 100-μm, respectively. Therefore, this p-MOSFET has full process compatibility with Hf-based high-κ CMOS. The material properties of high-κ ZrHfO gate dielectric were examined by grazing incidence x-ray diffraction diffractogram (GI-XRD). The fabricated devices were characterized by capacitance-voltage (C-V), current-voltage (I-V), and pulsed switching endurance measurements.

III. Results and Discussion

Fig. 1(a) shows the measured C-V characteristics of the high-κ ZrHfO p-MOSFET, in which the schematic 1T FeMOS was inserted. Similar to conventional 1T1C DRAM, the word

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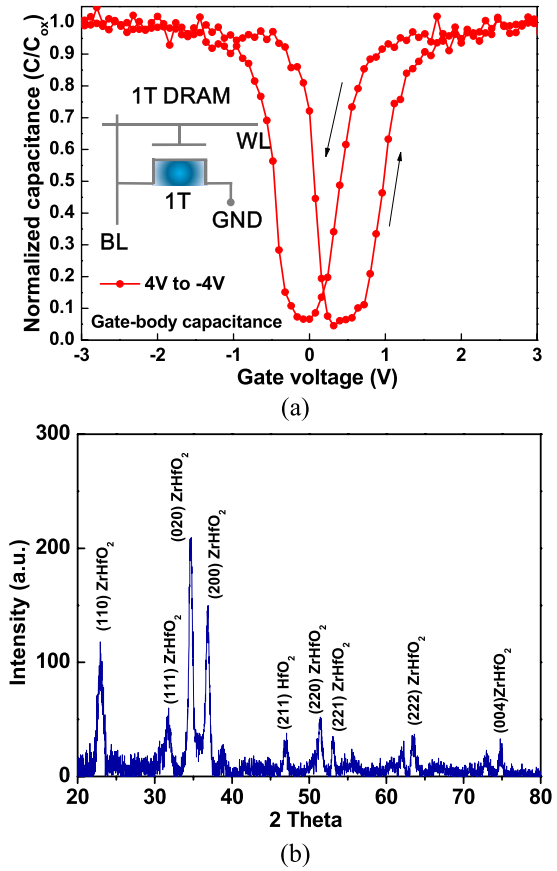

Fig. 1. (a) Measured C-V characteristics and (b) GI-XRD diffractograms of high-κ ZrHfO p-MOSFET. The inserted figure in Fig. 1(a) is the schematic plot of 1T FeMOS.

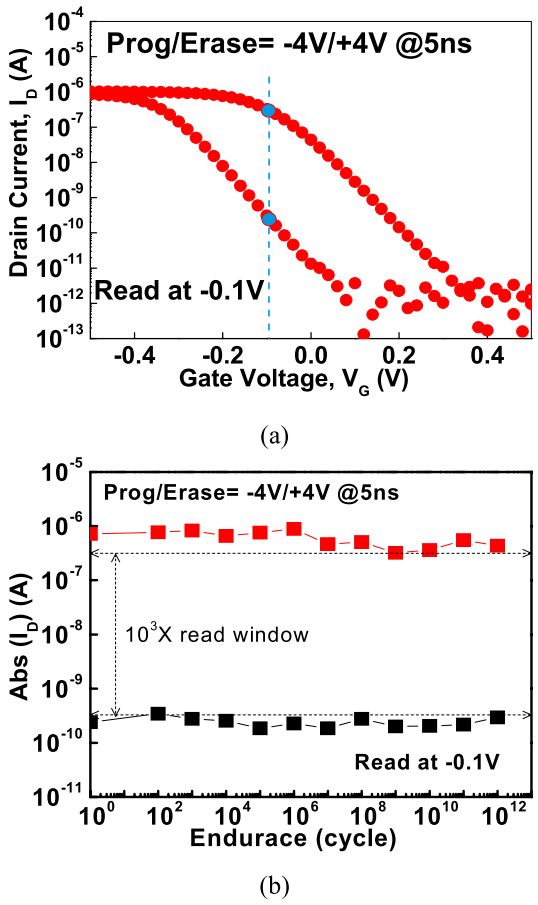

Fig. 2. (a) I_D-V_G after write at −4V/+4V 5 ns P/E pulses and (b) endurance characteristics of ferroelectric ZrHfO p-MOSFET.

and bit lines are connected to respective gate and drain to write/read the stored data. The ferroelectric hysteresis loop and flat band voltage shift were discovered at a 4 V to −4 V sweep. The ferroelectricity is related to the crystalline structure of the ZrHfO gate dielectric observed using GI-XRD diffractograms, as shown in Fig. 1(b), in which various crystalline phases were shown. It is crucial to notice that the ferroelectric gate dielectric thickness in 1T FeMOS was thinner for ZrHfO than for PZT, SBT and BLT [8]. Such a thin thickness is necessary to integrate ferroelectric gate dielectric into a highly scaled deep 1× nm MOSFET, in addition to the Hf-based dielectric compatibility with high-κ CMOS [11]–[14].

The FeMOS [7]–[8], in which the ferroelectric material was incorporated into the gate dielectric of the MOSFET, was previously used to perform nonvolatile memory functions. However, the FeMOS was subjected to read disturbance and degraded data retention caused by the depolarization effect [16]. To address the read disturbance problem, a novel read scheme was used here to measure the current at a small $V_G = -0.1$ V, which is different from measuring the V_T changes by using conventional methods at a high voltage. Such a low voltage reading has been used in resistive RAM (RRAM) [17]–[19] that can lower the read disturbance effectively in this FeMOS. Fig. 2(a) shows the measured I_D-V_G characteristics of the ferroelectric ZrHfO p−MOSFETs, after being written at 5 ns −4 V/+4 V program/erase (P/E) and read at a low $V_G = -0.1$ V.

The endurance characteristics are plotted in Fig. 2(b). Stable on-state current (I_{on}) and off-state current (I_{off}) were maintained for up to 10^{12} P/E cycles, and 5 ns P/E was the fastest pulse time in our system. A considerably large I_{on}/I_{off} read window of 1000 times and a considerably low DC off-state leakage current of 3×10^{-12} A/μm were measured, which are critical for energy saving. Although this device has substantially improved DC leakage power, the AC switching power ($CV^2f/2$) [20] was 1.1 times higher than that of the 32-nm 1T1C DRAM listed in the *ITRS* [1], assuming that was operated at the same frequency (f). Here C is the gate capacitor and/or MIM capacitor; V is the drain voltage and/or MIM capacitor voltage. Further reducing the device voltage is necessary for reducing the AC power. Considerably longer endurance is expected at a faster P/E speed with less stress to gate dielectric, because a sub-100 ps polarization switching time was reported in a ferroelectric capacitor.

The retention characteristics of I_{on} and I_{off} are shown in Fig. 3. Although the I_{on} and I_{off} degraded over time because of the depolarization effect, three orders of magnitude I_{on}/I_{off} read windows were still achieved after 10 s of retention at 25 °C. It is important to notice that the endurance and retention performances of this 1T FeMOS are already comparable with or superior to another type of 1T DRAM [21]. Further endurance to 10^{16} cycles using faster pulse generator equipment is necessary to explore the full potential for 1T1C DRAM

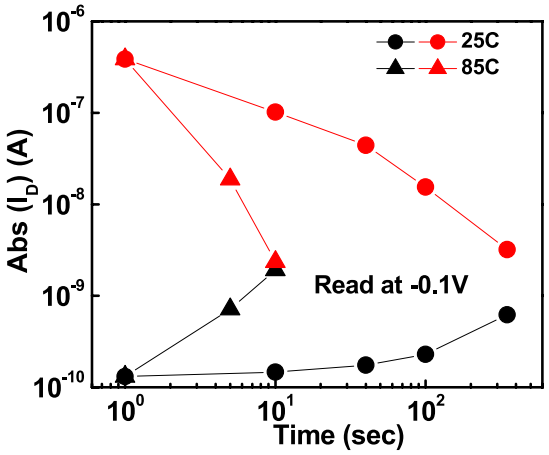

Fig. 3. Retention characteristics of the ferroelectric high-κ ZrHfO p-MOSFET.

replacement. Further retention improvement may be expected using a thinner SiO_2 [22] or high-κ interfacial layer [8], for which more than ten years retention was reported [22]. This new DRAM offers a considerably low DC off-state leakage of 3×10^{-12} A/μm, a simple capacitor-less 1T process, and a potentially sub-ns switching speed, all of which are impossible for existing 1T1C DRAM devices.

IV. Conclusion

This device offers superior DRAM functions with considerably low DC off-state leakage, a much simpler capacitor-less 1T structure, and a potentially faster speed, all of which far exceed those of existing DRAM devices. These excellent device characteristics were achieved using a ferroelectric high-κ ZrHfO gate dielectric in a p-MOSFET that is fully compatible with the existing high-κ MOSFET process used in current ICs.

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