A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic CMOS SoC for Real-Time Epileptic Seizure Control

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***Abstract*—An 8-channel closed-loop neural-prosthetic SoC is presented for real-time intracranial EEG (iEEG) acquisition, seizure detection, and electrical stimulation in order to suppress epileptic seizures. The SoC is composed of eight energy-efficient analog front-end amplifiers (AFEAs), a 10-b delta-modulated SAR ADC (DMSAR ADC), a configurable bio-signal processor (BSP), and an adaptive high-voltage-tolerant stimulator. A wireless power-and-data transmission system is also embedded. By leveraging T-connected pseudo-resistors, the high-pass (low-pass) cutoff frequency of the AFEAs can be adjusted from 0.1 to 10 Hz (0.8 to 7 kHz). The noise-efficiency factor (NEF) of the AFEA is 1.77, and the DMSAR ADC achieves an ENOB of 9.57 bits. The BSP extracts the epileptic features from time-domain entropy and frequency spectrum for seizure detection. A constant 30-μA stimulus current is delivered by closed-loop control. The acquired signals are transmitted with on-off keying (OOK) modulation at 4 Mbps over the MedRadio band for monitoring. A multi-LDO topology is adopted to mitigate the interferences across different power domains. The proposed SoC is fabricated in 0.18-μm CMOS and occupies 13.47 mm^2. Verified on Long Evans rats, the proposed SoC dissipates 2.8 mW and achieves high detection accuracy ($> 92\%$) within 0.8 s.**

***Index Terms*—Closed-loop control, epilepsy, neuron modulation, neural prosthesis, system-on-Chip (SoC), wireless power transmission.**

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I. Introduction

EPILEPSY is a one of the common neurological disorders. Around 1% of the world population is affected. Epileptic seizures are caused by sudden excessive electrical discharges in a group of cortical neurons. It is characterized by recurrent seizures, which may vary from a brief lapse of attention and unnatural posturing to severe and prolonged convulsions. The unexpected seizures impact the quality of life for patients and their families.

Currently, numerous anti-epileptic drugs are available for seizure control, but approximately 30% of epileptic patients remain either drug-resistant or develop limiting adverse effects [1]. Conventional resection surgery might be beneficial to patients who respond poorly to medical treatment. However, only some patients are suitable for resection surgery. The possibility of obtaining undesired neurologic deficits is always a concern. Electrical neuromodulation to control drug-resistant epilepsy has been attempted due to several potential advantages over conventional surgery, such as its reversible characteristic [2], [3].

In addition to peripheral vagus nerve stimulation, preliminary results show that electrical stimulation on the central nervous system is a promising solution, which is still under development. It delivers electrical impulses to a selected brain region in response to detected epileptic or pre-epileptic activities [4]. Preferably, a neural-prosthetic device realizing a recip-

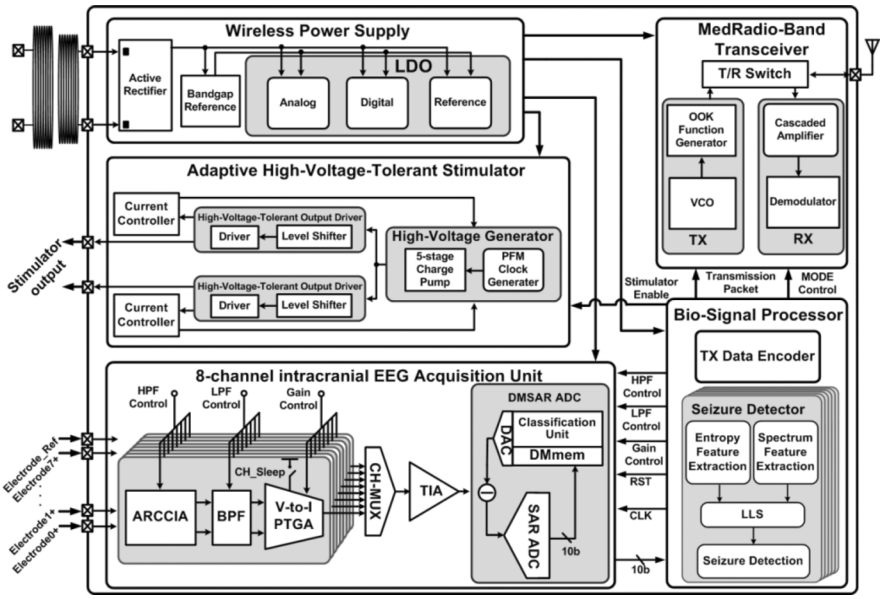

Fig. 1. System architecture of the proposed SoC.

rocal function is used to intersect the nervous system and to reset brain dynamics from a pathological to a physiological state. For epilepsy therapy, a responsive neural stimulation system should immediately and accurately detect epileptic activities to achieve higher treatment efficacy. Power consumption is another design consideration for such an implantable system. To prevent the tissue from damage by the heat from the system, the power consumption of the system should be lower than 35 mW [5], [6].

Several works have been developed for neural signal acquisition and seizure detection [7], [8]. An EEG acquisition SoC with seizure classification achieves 84.4% detection accuracy within 2 s [7]. A seizure onset detector with 100% accuracy has been presented in [8], but the detection latency is 13.5 s. In [9], a recording front-end with a spike-triggered stimulator has been presented, but the detection algorithm for specific seizure detection was not reported. In prior works, either detection accuracy is moderate or the detection latency is too long. Moreover, the responsive neural stimulation function has not been included.

To address these issues, we develop a fully integrated SoC composed of analog front-end amplifiers, an ADC, a bio-signal processor, and an electrical stimulator for closed-loop epileptic seizure control [10]. High detection accuracy ($> 92\%$) within 0.8 s has been achieved for real-time neuromodulation on animal experiment of Long Evans rats. With the inclusion of wireless power and data transmission, the proposed SoC is a promising solution for implantable devices of epilepsy treatment.

This paper is organized as follows. Section II describes the system architecture of the proposed SoC. In Section III, the design concepts and implementation details of each subsystem are presented. System verification and animal experiment results are given in Section IV. Finally, Section V concludes the paper.

II. System Architecture

The proposed 8-channel closed-loop neural-prosthetic SoC is shown in Fig. 1. The SoC is composed of two major parts: 1) a closed-loop signal-processing path including an 8-channel iEEG acquisition unit consisting of an 8-channel AFEA and a 10-b DMSAR ADC, a BSP, and an adaptive high-voltage-tolerant stimulator and 2) a wireless transmission link including a MedRadio-band transceiver and a wireless power supply system.

The operation of the signal processing path is described as follows. The iEEG signals are sensed by the electrodes and acquired by the AFEA. The AFEA provides three-step gains to amplify the iEEG signals, and the amplified signals are then sent to the DMSAR ADC. The DMSAR ADC samples the difference between the present signal and previous signal stored in a memory array at 62.5 kSamples/s/channel, which translates to 500 kSamples/s when eight channels are utilized. By employing the fine and coarse conversion operations, the signals are resolved to obtain 10-bit digital codes.

The digitized 10-bit iEEG signals are further fed to the BSP to extract the epileptic features in time-domain entropy and frequency spectrum. Once a seizure has been detected, the BSP sends a command to activate the adaptive stimulator in order to deliver current to suppress the aberrant brain activities. To adapt to a wide range of load impedances of the electrode–tissue interface, a high-voltage generator with five-stage charge pump and a pulse-frequency modulator (PFM) has been designed to supply a variety of voltages (up to 10 V) for the output drivers. A current controller detects the output current and sends a feedback signal to control the PFM. The charge pump circuit modulated by the clock generator pumps the supply voltage to an adequate level to deliver a constant 30-μA stimulation current. Thus, the closed-loop seizure control is carried out by a sequence of operations from signal acquisition, seizure detection, to electrical stimulation.

The recorded iEEG signals are transmitted at a data rate of up to 4 MHz over the MedRadio band (401 to 406 MHz) for signal monitoring. The transmitted signals are encoded with reliable cyclic redundancy check (CRC) for error checking. The

encoded data are then sent to an OOK modulator. At the receiver, cascaded gain stages and a four-input current-mode envelope detector are used to recover the signals.

For an implanted system supported by a battery, the voltage of the battery decrease as time passes after implantation, and thus the signal quality and system performance of the implanted system are degraded. Moreover, frequent surgery for battery replacement increases the risk for the patients. Therefore, a wireless power supply system has been designed to supply a steady power to the implanted device and hence maintain signal quality and system performance. A rechargeable battery can also be implanted to be a backup power source for the implanted system. The required power of the SoC is transmitted through inductive coils. The wireless power supply system includes a pair of coils with a resonance frequency of 13.56 MHz, an active rectifier, and three low-dropout regulators (LDOs). In the active rectifier, two delay comparators are used to compensate both gate turn-on and turn-off delay times of the power MOS devices to achieve a conversion efficiency of 84.8%. A multi-LDO topology is adopted to mitigate interferences across different power domains.

III. Circuit Design

Here, the 8-channel aquisition unit, the bio-signal processor, and the adaptive high-voltage-tolerant stimulator are described first. The other two additional subsections describe the supporting units: the MedRadio-band transceiver and the inductive link power supply system.

A. 8-Channel Acquisition Unit

The architecture of the 8-channel acquisition unit is described in Fig. 1. It consists of an 8-channel AFEA and a DMSAR ADC. The 8-channel AFEA consist of eight auto-reset capacitive-coupled instrumentation amplifiers (ARCCIAs), configurable bandpass filters (BPFs), power-gating programmable transconductance gain amplifiers (PTGA), a multiplexer, and a shared transimpedance amplifier (TIA). Each AFEA channel is implemented by using two cascaded stages. The first stage is the ARCCIA with a low-noise amplifier and an auto-reset unit (ARU) followed by a BPF to provide a 40-dB gain. The ARU detects the range of the output of the ARCCIA and provides an additional path to prevent saturation of the AFEA by electrical stimulation or other extra injection charges. Hence, periodic reset or auto-zeroing, which degrades the high-pass frequency, can be avoided. With the use of the proposed T-connected pseudo-resistor (TPR), a low high-pass cutoff frequency can be realized with lower impedance to ensure the stability of the AFEA. The second stage includes the PTGA and TIA, which provide additional gains for proper voltage-level adjustment. All passive components and bias circuits are designed on chip to avoid off-chip components and to achieve better matching characteristics.

1) Analog Front-End Amplifier: In the neural-prosthesis SoC for implantable devices, the acquired iEEG signals have the characteristics of small amplitude (0.05–1 mV), low frequency (0–200 Hz), and low signal-to-noise ratio [11], [12]. Thus, the AFEA must meet the following design requirements.

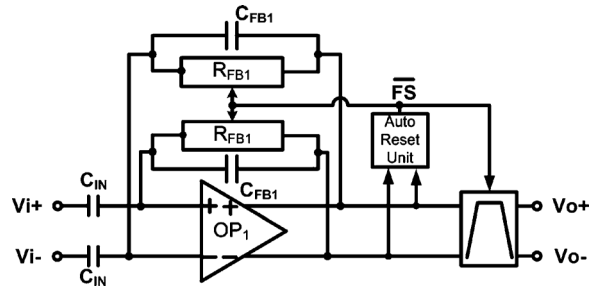

Fig. 2. Structure of the ARCCIA.

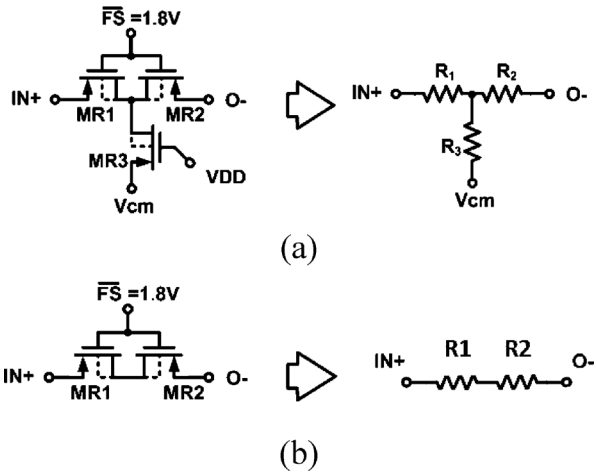

Fig. 3. (a) Schematic of $\mathrm{RFB_1}$ implemented with TPR and the equivalent model. (b) Schematic of the conventional pseudo-resistor and the equivalent model.

1) The power consumption should be minimized to extend the system lifetime and to reduce the heat to prevent damaging the surrounding tissues by heating.
2) The noise rejection ability should be high to reduce output noise from sources including power-line interference and electrically or magnetically induced interference.
3) The electrode dc offset (EDO) should be eliminated to prevent saturation of the succeeding amplifier. An ultra-low high-pass cutoff frequency must be realized to filter out the EDO and prevent in-band signal degradation.

The first stage of the AFEA is an ARCCIA combined with a BPF. As shown in Fig. 2, capacitors $\mathrm{C_{in}}$ at the input node block out any EDO from the electrode–tissue interface. The ac-coupled signal is further amplified by a succeeding low-noise amplifier. The low-noise amplifier has a fully differential operation amplifier (OP) which includes a capacitor and a resistor in parallel as a feedback circuit. The-fully differential OP amplifier $\mathrm{OP_1}$ is employed to improve both common-mode rejection ratio (CMRR) and linearity. The differential input and output swings of $\mathrm{OP_1}$ are designed as 10 mVp-p and 1 Vp-p, respectively, for neural signal recording. The bias voltages in $\mathrm{OP_1}$ are generated by an on-chip biasing circuit.

Fig. 3(a) shows the feedback resistor $(\mathrm{R_{FB1}})$ implemented with the proposed TPR and its equivalent circuit. The equivalent resistance of the TPR is $R_1 + R_2 + R_1 \cdot R_2/R_3$, which is larger than the resistance $R_1 + R_2$ of the conventional architecture shown in Fig. 3(b) [13]. The resistance (around $1\mathrm{T}\Omega$) of each

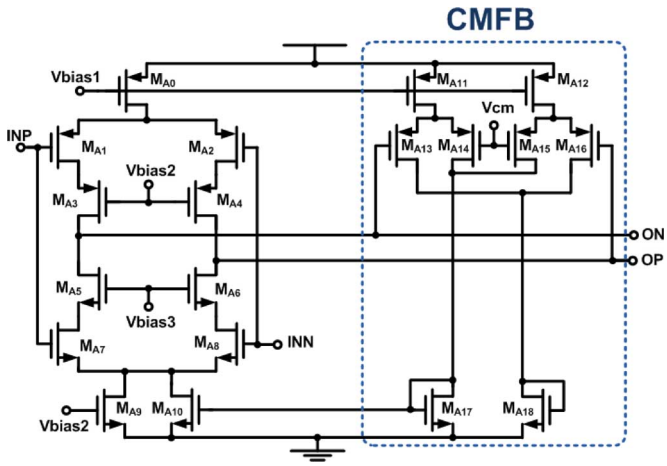

Fig. 4. Schematic of OP_1.

pseudo-resistor in the TPR is designed to be smaller than that in [7] to avoid the nonlinearity caused by the ultra-high resistance.

The OP_1 has both PMOS and NMOS transistors as input pairs to achieve a better noise-to-power tradeoff [14], as shown in Fig. 4. Transistors $\mathrm{M_{A3}}$–$\mathrm{M_{A6}}$ are used to improve the gain of OP_1 without extra supply current and to retain stability. The input-referred noise density of OP_1 can be expressed as

$$\frac{\overline{Vn_{OP1}^2}}{\Delta f} = \frac{1}{(g_{mN}+g_{mP})^2} \times \left[\frac{8}{3}kT(g_{mN}+g_{mP}) + 2\cdot\left(\frac{K_N\cdot g_{mN}^2}{C_{oxN}\cdot f\cdot W_N\cdot L_N}+\frac{K_P\cdot g_{mP}^2}{C_{oxP}\cdot f\cdot W_P\cdot L_P}\right)\right] \quad (1)$$

where g_{mN} and g_{mP} are the transconductances of input NMOS ($\mathrm{M_{A7}}$, $\mathrm{M_{A8}}$) and PMOS ($\mathrm{M_{A1}}$, $\mathrm{M_{A2}}$), respectively, f is the signal frequency, k is the Boltzmann constant, T is the absolute temperature, Δf is the bandwidth of amplifier, and $C_{\mathrm{oxN}}/C_{\mathrm{oxP}}$ is the gate-oxide capacitance per unit area of NMOS/PMOS. All input transistors are designed to operate in the subthreshold region to achieve a high transconductance efficiency. The input-referred noise of the ARCCIA with respect to that of OP_1 is represented by

$$\overline{Vn_{\mathrm{ARCCIA}}{}^2} = \left(\frac{C_{\mathrm{IN}}+C_{\mathrm{FB1}}+C_{P1}}{C_{\mathrm{IN}}}\right)^2 \cdot \overline{Vn_{OP_1}{}^2} \quad (2)$$

where C_{P1} is the parasitic input capacitance of OP_1. Increasing the gate area of the input transistors suppresses the flicker noise of OP_1, but increases the weight of $\overline{Vn_{OP1}{}^2}$ in (2). Thus, the gate areas of the input devices are sized to minimize $\overline{Vn_{\mathrm{ARCCIA}}{}^2}$.

The transfer function of the ARCCIA can be expressed approximately as

$$T(s) = \frac{C_{\mathrm{IN}}}{C_{FB1}}\cdot\frac{j\omega R_{FB1}C_{FB}}{(1+j\omega R_{FB1}C_{FB})\cdot\left(1+j\omega\frac{C_{\mathrm{IN}}C_{LP}}{C_{FB1}g_m}\right)}. \quad (3)$$

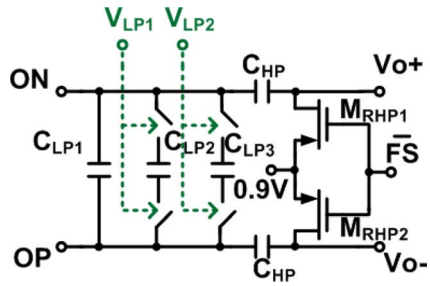

Fig. 5. Schematic of a bandpass filter.

From (3), the high-pass and low-pass cutoff frequencies are $1/(2\pi\cdot R_{FB1}\cdot C_{FB1})$ and $(g_m\cdot C_{FB1})/(2\pi\cdot C_{IN}\cdot C_{LP})$, respectively where g_m is g_{mN} plus g_{mP}. The mid-band gain is C_{IN}/C_{FB1}, which is designed for 40-dB amplification.

The BPF has been implemented with PMOS pseudo-resistors and parallel-connection capacitors as shown in Fig. 5. A high-pass function has been designed to further eliminate the output offset (+2.5 to −2.75 mV) of the ARCCIA, that is amplified from the input offset voltage $\mathrm{V_{os}}$ of OP_1 by the TPR factor of $(R_2+R_3)/(R_2)(=6)$ as may be seen from Figs. 2 and 3(a). After the BPF and PTGA, the output offset voltage is around 19 mV and the equivalent input referred offset voltage is 0.19 mV. The low-pass function is controlled by the digital signals $\mathrm{V_{LP}}$ ($\mathrm{V_{LP1}}$, $\mathrm{V_{LP2}}$). With different values of $\mathrm{V_{LP}}$, the number of parallel-connected capacitors is selected to adjust the low-pass cutoff frequency. The sizes of $\mathrm{C_{LP1}}$, $\mathrm{C_{LP2}}$, and $\mathrm{C_{LP3}}$ are 0.45, 0.75, and 2.78 pF, respectively. The voltage of 0.9 V in Fig. 5 supplies the common-mode voltage for Vo+ and Vo− which are the input signals of the following stage (PTGA).

An ARU is used in the ARCCIA for fast start-up and recovery from channel saturation. The ARU is implemented with four dynamic voltage comparators and reset control logic. The differential output voltages of OP_1 are compared with the given high and low threshold voltages. Once the differential output voltages of OP_1 exceed the thresholds, the gates of transistors in TPR and the pseudo-resistor in BPF are connected to ground ($\overline{FS}=$ 0 V) to reduce the recovery time, specified by $\mathrm{R_{FB1}}$ and $\mathrm{C_{FB1}}$ [15].

The second stage of the AFEA is a programmable-gain stage composed of a PTGA and a TIA as shown is Fig. 6. The PTGA transfers a voltage signal to a current signal. The current signal is further transfer to an output voltage signal by the TIA. A power-gating function is embedded to switch between active mode and standby mode by controlling CLK_Sleep which reduces the power dissipation by 40%. The parallel-connected resistors ($\mathrm{R_{G0}}$, $\mathrm{R_{G1}}$, $\mathrm{R_{G3}}$) are selected to adjust the transconductance of the PTGA with digital control signals ($\mathrm{V_{G1}}$, $\mathrm{V_{G2}}$) so that three gain steps (1 ×, 3 ×, 10 ×) can be provided for adaptive signal scaling. The low input impedance of the TIA stage, consisting of $\mathrm{C_{FB2}}$, $\mathrm{R_{FB2}}$, and OP_2, improves the slew rate and linearity of the PTGA.

2) Delta-Modulated SAR ADC: In DMSAR ADC, only the voltage difference between two successive samples needs to be resolved to reduce the conversion steps and decrease the power consumption [16]. The proposed DMSAR ADC includes

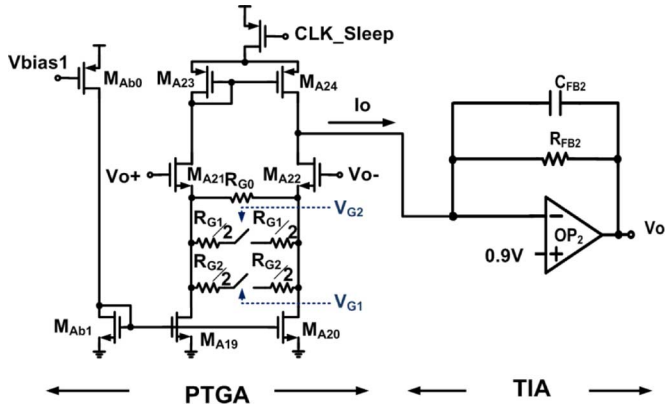

Fig. 6. Schematic of PTGA and TIA.

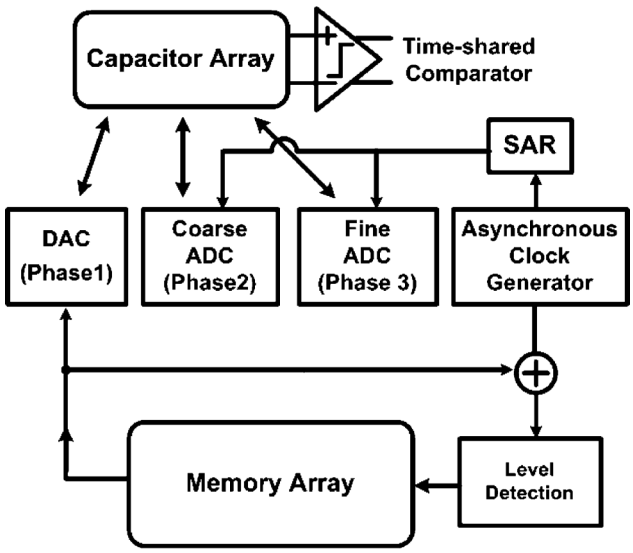

Fig. 7. Architecture of the DMSAR ADC.

a switched-capacitor array, a time-shared comparator, a memory array, registers, an adder, and an asynchronous clock generator as shown in Fig. 7. It is operated in three phases. First, a binary-weighted DAC samples the value stored in the memory array for channel i and output of AFEA$_i$ to obtain the voltage difference. Second, the coarse ADC determines the range of the sampled voltage difference. Finally, the fine ADC resolves the voltage difference for LSBs. The comparator is shared in the coarse and fine conversion phases. The 10-bit memory for each channel is required to store previously quantized data which are sent back to the DAC to obtain the signal difference for conversion from the same channel. Delta modulation is embedded in the conversion process.

In the proposed acquisition unit, one DMSAR ADC is shared by eight AFEAs. The sampling rate is set to 62.5 kHz per channel, which is sufficient for neural signal sampling. For iEEG with 200-Hz bandwidth, 312 points are sampled within one period for real-time observation. Since the signal difference between two consecutive samples is relatively smaller than the peak signal swing, the delta modulation is adopted. As a result, the number of conversion steps can be further reduced, saving power consumption by up to 66%.

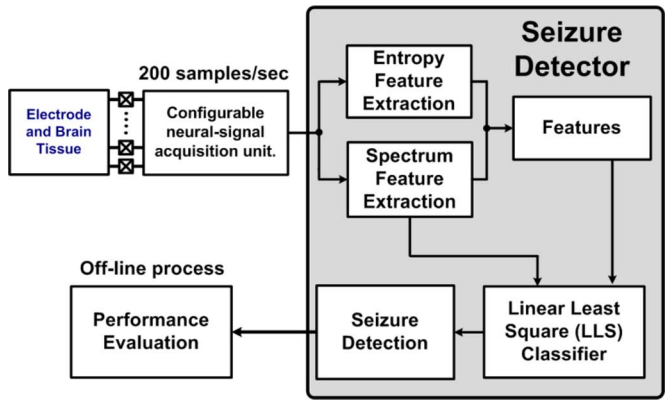

Fig. 8. Architecture of a single-channel detector.

B. Bio-Signal Processor

The proposed BSP contains seizure detectors and one TX data encoder for cyclic redundancy check (CRC). A power-efficient fast Fourier transform (FFT) core, an approximated entropy (ApEn) encoder, and a linear least square (LLS) classifier are integrated as single seizure detector. The digitized iEEG signals from the DMSAR ADC are sent to the BSP to extract the features of the entropy and the spectrum. Fig. 8 shows the seizure detection algorithm and the signal processing flow. Both signal entropy and frequency spectrum are extracted as epileptic features to enhance the seizure detection performance [17]. In our previous studies [18]–[21], it was observed that ApEn with multiband EEG power spectra can be used to effectively classify seizure and nonseizure EEG signals.

ApEn is a measure that evaluates the randomness or the regularity of a time sequence [22]. An experiment showed that the ApEn index yielded a dominant factor (when compared with spectra analysis) in the trained LLS model for absence seizure detection in [19]. In our LLS model, the weighting factors of ApEn and two power spectrum bands are 51.6%, 32%, and 16.4%, respectively. Multiband iEEG power spectra are therefore utilized as the complementary features of ApEn to reduce the false alarm rate and enhance the detection accuracy. Apart from the accuracy of the utilized algorithm on epileptic seizure, low computational cost, and short detection delay also provides low power consumption and real-time ability for various implementations.

Based on the algorithm presented in [19], a prototype with enhanced 8051 microcontroller [21] is demonstrated to achieve 117.66 mW/channel for the absence animal model. An improvement in power consumption of over $10\times$ is reported (7.21 mW/channel) on the implementation of high-performance reduced instruction set computing (RISC) processor [17] with code optimization. To further improve energy efficiency, the first hardware-based prototype is presented in [20], which provides two-channel processing capability and is verified on field-programmable gate array (FPGA). Through approximation of numbers and pipeline execution, the detection accuracy and delay of hardware prototype still fail to meet specifications (accuracy $>$ 90% and delay $<$1.0 second.) In this work, the SoC integrates more channels of detectors [20] and achieves power consumption of 162.31 μW/channel (77.91 μJ/detection.) The

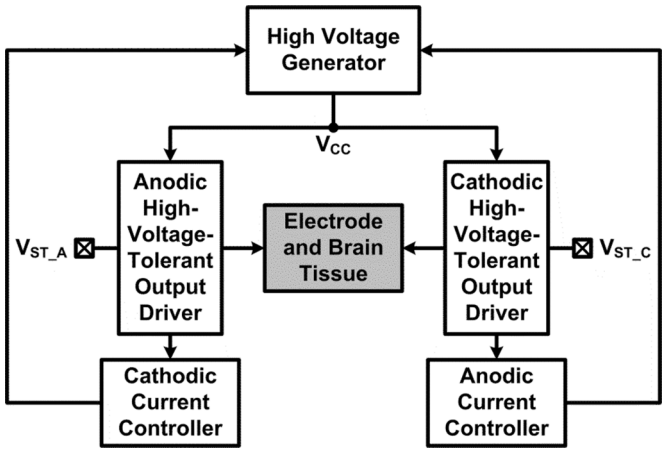

Fig. 9. Architecture of adaptive high-voltage-tolerant stimulator.

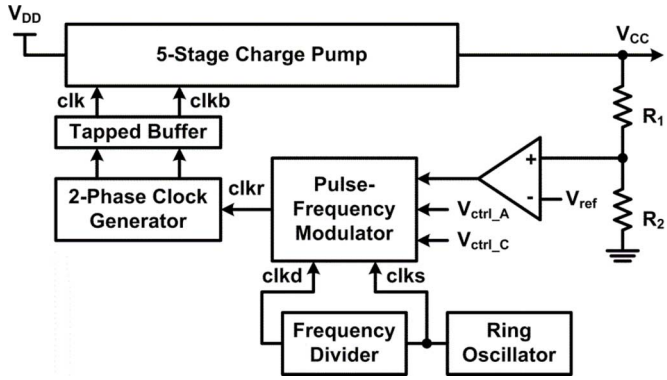

Fig. 10. Architecture of high-voltage generator.

proposed BSP detects more than 92% of seizures within 0.8 s. It outperforms the support vector machine (SVD)-based EEG acquisition processor in [7], which achieves 84.4% detection accuracy within 2 s. It also provides the faster response than prior works [23], [24].

A two-phase seizure detection [18], [25], consisting of patient-specific training and online detection, is performed. The utilized linear least-square model finds a best fitting curve to minimize mean-square errors between detection results (circuit) and desired output (determined by neurologist). In the off-line training stage, continuous neural signals of seizures (SWD) and non-seizures (WK, SWS, and artifact) are recorded for feature extraction. iEEG data corresponding to various behavioral states are utilized for training a classifier. The time-domain and frequency-domain characteristics of iEEG signals, with respect to various physiological states, are integrated as seizure detection features. These spontaneous events are used to train the seizure classifier program off-line. The training procedure is performed until the accuracy is over 90% and detection delay is shorter than 1.0 s.

A short-range radio-frequency (RF) transmitter is integrated into the SoC to provide real-time waveform observation. Before wireless transmission, iEEG data packet is down-sampled by a factor of 4 to save data bandwidth. Next, the CRC encoder with CRC-7 polynomials is utilized against data corruption. A universal asynchronous receiver/transmitter (UART)-like protocol is adopted to encapsulate iEEG data and CRC codes. CRC computation and wireless transmission are operated under 8 × sampling clock. Incorporated with 8 × sampling clock and down-sampling scheme, the iEEG data can be transmitted continuously for real-time monitoring.

C. Adaptive High-Voltage-Tolerant Stimulator

For system integration, a high-voltage-tolerant stimulator with adaptive loading in a standard process is proposed in order to avoid the use of high-voltage transistors. The proposed stimulator consists of a high-voltage generator, a pair of high-voltage-tolerant output drivers, and a pair of current controllers, as shown in Fig. 9. The stimulator has been designed to deliver biphasic stimulus currents with H-bridge topology [26]. The biphasic stimulus pattern a constant $\pm 30\ \mu$A current. With a supply voltage $\mathrm{V_{DD}} = 1.8$ V, the biphasic stimulus currents are modulated by a pair of enable signals ($\mathrm{V_{ST\_A}}$ and $\mathrm{V_{ST\_C}}$) generated from the BSP. To adapt to a wide range of loading impedances between the electrode and the brain tissue, the high-voltage generator is designed to supply a variable voltage ($\mathrm{V_{CC}}$, up to 10 V) for the output drivers.

When the stimulator is activated, the enable signal $\mathrm{V_{ST\_A}}$ ($\mathrm{V_{ST\_C}}$) controls an anodic (cathodic) high-voltage-tolerant output driver to deliver anodic (cathodic) stimulus currents to the electrode and brain tissue. The anodic (cathodic) current controller detects the anodic (cathodic) stimulus current, and sends a control signal back to the high-voltage generator. The high-voltage generator then delivers $\mathrm{V_{CC}}$ to the output drivers. The detailed circuits of each block for the loading impedance of 10–250 kΩ will be discussed in the following.

High-Voltage Generator: As shown in Fig. 10, the high-voltage generator consists of a five-stage charge pump, a voltage divider ($\mathrm{R_1}$ and $\mathrm{R_2}$), a comparator, a PFM, a ring oscillator, a frequency divider, a two-phase clock generator, and tapped buffer. Because of the wide voltage range of $\mathrm{V_{CC}}$, the high-voltage generator must be carefully designed. The charge pump circuit is adopted without sacrificing the gate–oxide reliability [27]. The output voltage of the five-stage charge pump circuit with 1.8 V $\mathrm{V_{DD}}$ supply can be pumped up to around 10 V. To support such a wide range of voltages, the pumping frequency of the charge pump is adjustable. The PFM is proposed to choose and modulate the clock frequency. In this work, if $\mathrm{V_{CC}}$ is lower than 5 V, the PFM chooses a low-frequency *clkd* (3.125 MHz) as the central frequency. Otherwise, a high-frequency *clks* (31.25 MHz) is chosen. Using the lower clock frequency helps to reduce the glitch current with the lower $\mathrm{V_{CC}}$. If a higher or lower $\mathrm{V_{CC}}$ is required, the PFM also modulates the clock frequency to be higher or lower.

The power efficiency of the charge pump is defined as

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{CC}} \cdot I_{\mathrm{load}}}{V_{\mathrm{DD}} \cdot I_{\mathrm{total}}} \tag{4}$$

where I_{load} and I_{total} denote the loading current and the total current consumption in the charge pump [28]. Considering the five-stage charge pump, the output voltage is

$$V_{\mathrm{CC}} = 6 \cdot V_{\mathrm{DD}} - \frac{5 \cdot I_{\mathrm{load}}}{f \cdot C} \tag{5}$$

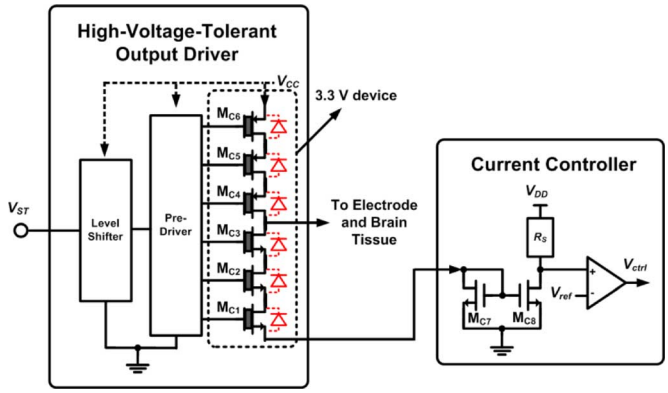

Fig. 11. Architecture of high-voltage-tolerant output driver and current controller with the parasitic diodes string in the output series transistors.

and the total current consumption is

$$I_{\text{total}} = 6 \cdot I_{\text{load}} + 5 \cdot C_p \cdot f \cdot V_{\text{DD}} \tag{6}$$

where f, C, and C_{p} denote the clock frequency, stage capacitance, and parasitic capacitance, respectively. Since this charge pump is designed to output a wide range of V_{CC} voltages, the clock frequency, total current, and power efficiency of the charge pump vary with the output voltage. The simulated power efficiency of the charge pump lies between 43% and 72%.

High-Voltage-Tolerant Output Driver: Fig. 11 shows the anodic and cathodic high-voltage-tolerant output drivers. It includes associated parasitic-diode string in the output series transistors, which consist of a level shifter, a pre-driver, and stacked 3.3-V MOS transistors. The stacked MOS structure along with 3.3-V transistors placed between V_{CC} and ground can sustain up to 10 V without electrical overstress issues [29].

The level shifter is designed to convert the low (0 V/1.8 V) enable signals to a high-voltage level. The pre-driver receives the high-voltage signal and then controls the output stage of stacked transistors. The pre-driver outputs are varied according to the loading impedance. The PMOS and NMOS transistors in output stage are well controlled to decide whether the stimulation is on. For example, if the loading impedance leads the stimulus voltage to 4.3 V/9.2 V, the pre-driver outputs for M_{C1}–M_{C6} are 0 V/0 V, 1.4 V/3.3 V, 2.9 V/6.3 V, 2.9 V/6.3 V, 2.9 V/6.3 V, and 2.9 V/6.5 V, respectively. All voltage differences across the stacked MOS transistors are smaller than 3.3 V to sustain reliability.

Current Controller: The current controller consists of a current mirror, a trimmable resistor (R_{S}), and a comparator. When the stimulator is turned on, the stimulus current flows through both stacked transistors and current mirror to induce a proportional current $(\text{I}_{\text{mirror}})$. The current controller utilizes the I_{mirror} flowing through R_{S} to generate a voltage signal $(\text{V}_{\text{DD}} - \text{I}_{\text{mirror}} \times \text{R}_{\text{S}})$ to compare with a reference voltage (V_{ref}). Our previous studies have demonstrated an intra-incertal current stimulation of $\sim$30 μA to successfully stop seizures [19], [21], [30]. The comparator compares these two voltages and determines if the stimulus current is under or below 30 μA. The adjustable supply voltage (V_{CC}) for the output driver is controlled by the output signal of the current controller. If the anodic stimulus current is lower than 30 μA, the output signal of the current controller goes high $(\text{V}_{\text{ctrl\_A}} = 1.8\ \text{V})$. The high-voltage generator keeps pumping to provide a higher voltage until the anodic stimulus current reaches 30 μA. Once the anodic stimulus current is higher than 30 μA, the output of the current controller goes low $(V_{\text{ctrl\_A}} = 0\ \text{V})$. The high-voltage generator will stop pumping until the anodic stimulus current returns to 30 μA. Since the stimulus current is 30 μA per channel, the power consumption of the current mirror in the current controller is about 10 μW. The latency from the input to the output of the current controller is around 25 ns. The feedback control loop causes the anodic stimulus current to keep around 30 μA during anodic stimulation. Similarly, the cathodic stimulus current is kept at -30 μA during cathodic stimulation.

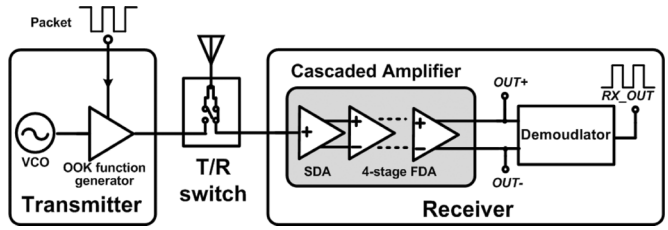

Fig. 12. Architecture of the OOK MedRadio-band transceiver.

D. MedRadio-Band Transceiver

To reduce power dissipation and to minimize chip area for implantable devices, OOK modulation has been adopted for data transmission. The proposed OOK transceiver is designed for the FCC MedRadio Service band (401–406 MHz). It includes a transmitter (TX), a T/R switch, and a receiver, as shown in Fig. 12. The transmitter (TX) is composed of a ring-oscillator VCO with an OOK function generator [31]. The receiver (RX) has a single-ended-to-differential amplifier (SDA), four cascaded fully differential amplifiers (FDAs), and a full-wave current-mode envelope detector (demodulator) [32] The proposed detector rectifies the input signal with appropriate gain to eliminate extra baseband amplifier. Local oscillator and down-conversion mixer are not included to reduce power consumption and chip area. The demodulator is designed to recover the amplified signals from the gain stages with a bandwidth of up to 4 MHz. A T/R switch is designed to increase the isolation and switch between TX and RX ports. The output power of the transmitter is -17 dBm, which is lower than the specified limitation of -16 dBm. At the receiver, the sensitivity is -53 dBm at a distance of 10 cm.

E. Inductive Link Power Supply System

In order to eliminate the use of a battery to avoid frequent surgery for battery replacement, an inductive link power transmission system is proposed to supply the power for the SoC. The architecture of the proposed inductive link power supply system consists of a pair of near-field coils, an active rectifier, and three local LDOs, as shown in Fig. 13. The primary coil transmits the power through a magnetic inductive link at a carrier frequency of 13.56 MHz in the Industrial, Scientific and

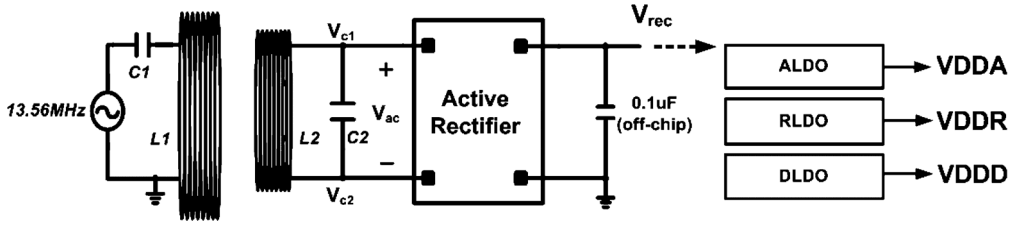

Fig. 13. Architecture of the inductive link power supply system.

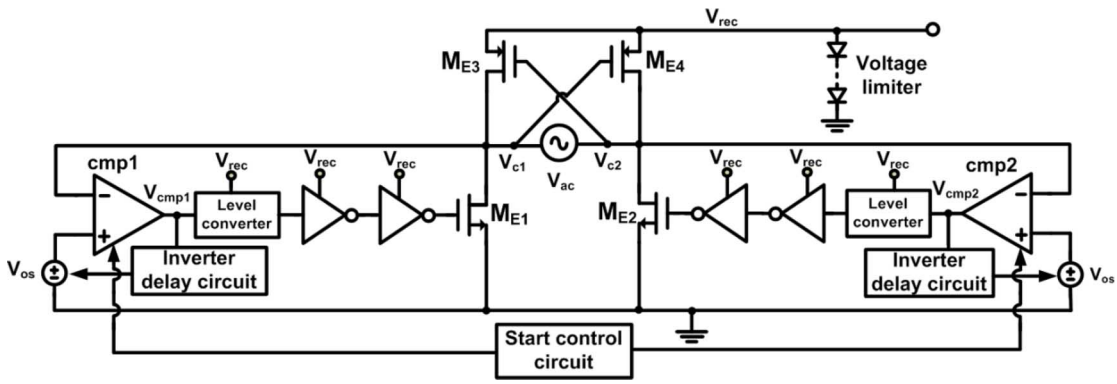

Fig. 14. Schematic of the active rectifier.

Medical (ISM) band to the secondary coil. The rectifier converts the received ac power to a dc signal ($\mathrm{V_{rec}}$). The LDOs regulate $\mathrm{V_{rec}}$ to support stable power sources for different circuit requirements. In the proposed rectifier, a fully on-chip dynamic compensated topology is employed to enhance the power efficiency. The multi-LDO topology is adopted to optimize the LDO performance and isolate the disturbances from digital circuit domain.

Active Rectifier: The schematic of the active rectifier is shown in Fig. 14 The power PMOSs ($\mathrm{M_{E3}}$, $\mathrm{M_{E4}}$) form a cross-coupled pair and function as switches [33], which are turned on by $\mathrm{V_{ac}}$. Two two-terminal comparators cmp1 and cmp2 are used to control the gate voltages of the power NMOSs ($\mathrm{M_{E1}}$, $\mathrm{M_{E2}}$) by comparing the input node voltages (V_{c1} and V_{c2}) with ground voltage respectively. A start-up circuit controls the comparator output voltage when $\mathrm{V_{rec}}$ starts from zero. The voltage limiter limits $\mathrm{V_{rec}}$ to a maximum value of 2.5 V (normally at 2 V) when the input power of the active rectifier is too large. The output voltages $\mathrm{V_{cmp1}}$ and $\mathrm{V_{cmp2}}$ from the comparators of cmp1 and cmp2, respectively, are used to dynamically adjust the current sources of the differential input pairs. With different bias currents, different input offset (V_{os}) voltages are created to compensate both turn-on and turn-off gate delay times of the power MOS devices to achieve an efficiency of 84.8%, with 20-mA output current and 327.5-mV dropout voltage.

Low-Dropout Regulator: A topology of multiple local capacitor-free LDOs with a replica-biased loop is proposed to isolate the interference between power domains and satisfy different circuit requirements, as shown in Fig. 15. The output stage of each LDO is the same but with different compensation techniques according to the requirements in driving capabilities. Each regulation loop is designed for each power domain and it drives the designated circuit individually.

ALDO, RLDO, and DLDO are designed for analog circuits, reference voltages, and BSP with stimulator circuits, respectively. The replica-biased loop is used to generate a stable bias voltage VSET for load regulation whereas the fast voltage regulation is achieved by the local regulation loops. VO, VDDA, VDDR, VDDD are the output voltages of replica-biased loop, ALDO, RLDO, and DLDO, respectively. Flipped voltage follower (FVF) [34] cells are used as the output stages for the LDOs. The adaptive-biased voltage-controlled current source (ABVCCS) and voltage control current source (VCCS) are designed to enhance the stability under a variety of load conditions for ALDO and RLDO. A slew-rate enhancement (SRE) circuit is used to achieve fast transient response in the absence of a large external capacitor for DLDO.

IV. Experimental Results

Fig. 16 shows the chip photograph. The proposed SoC was fabricated in an 0.18-μm CMOS process and the total chip area is 13.47 mm^2 including the ESD pads. Each subsystem was tested separately and the function of the whole system was verified in an animal experiment.

A. System Verification

Fig. 17 shows the measured frequency response of the AFEA where both the high-pass and low-pass cut-off frequencies are tunable. The high-pass cut-off frequency of the AFEA is measured by adjusting the gate voltage ($\overline{FS}$) of the pseudo-resistor ($\mathrm{M_{RHP1}}$, $\mathrm{M_{RHP2}}$) in Fig. 5 to eliminate the EDO while maintain the signal amplitude of the low-frequency signal. The high-pass (low-pass) cut-off frequency is adjusted from 0.1 to 10 Hz (0.8

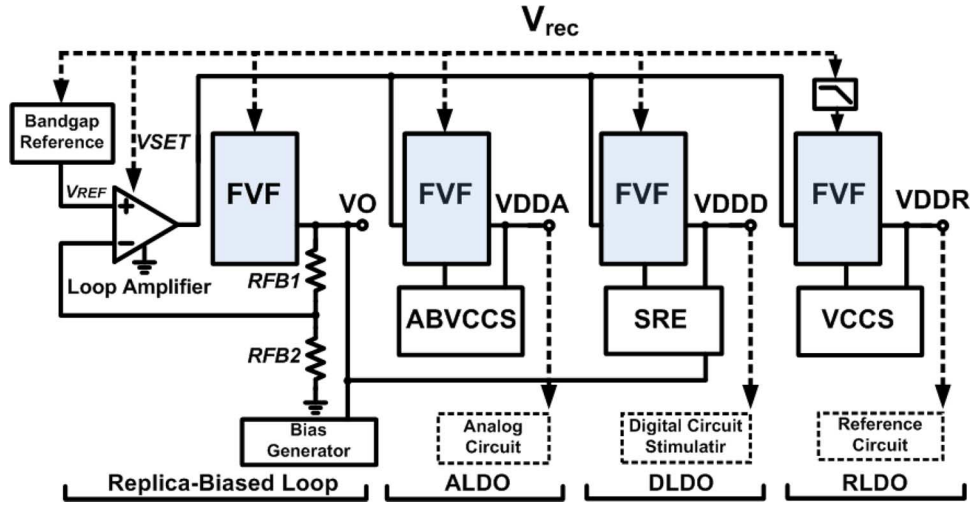

Fig. 15. Architecture of the multiple LDOs.

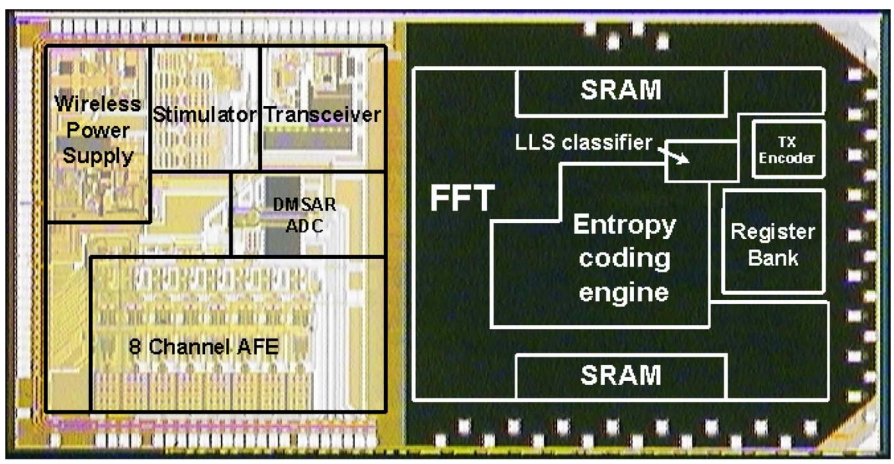

Fig. 16. Chip photograph of the SoC.

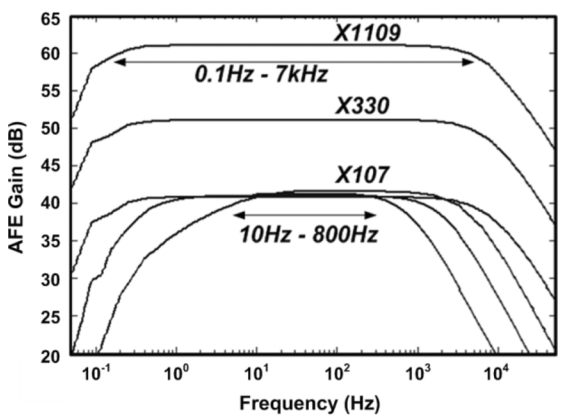

Fig. 17. Measured frequency response of the AFEA.

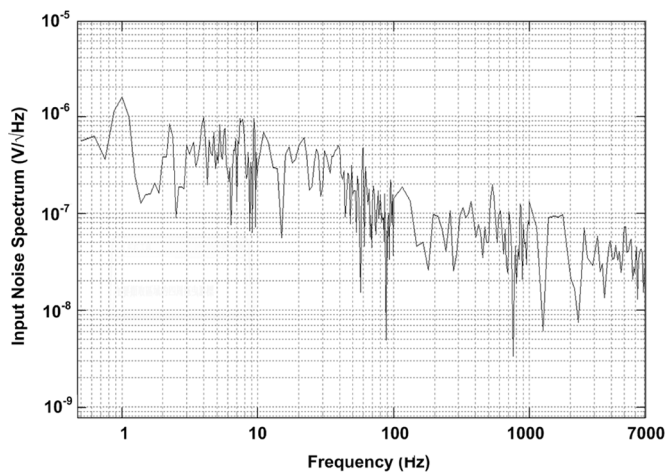

Fig. 18. Measured input-referred noise of the ARCCIA.

to 7 kHz). The AFEA provides three-step gains (41, 50, and 61 dB). The power spectrum of the measured input-referred noise for 0.5 Hz–7 kHz is measured with external power supply and the HPF, LPF, and gain are set to 1 Hz, 7 kHz, and 40 dB, respectively, as shown in Fig. 18. The power consumption of the ARCCIA and the AFEA is 0.97 and 53.7 μW, respectively. The measured input-referred noise is 5.23 $\mu V_{\rm rms}$ and the NEF with a 7-kHz bandwidth for the ARCCIA stage is 1.77. The DMSAR ADC operates at 500 kSample/s and the measured

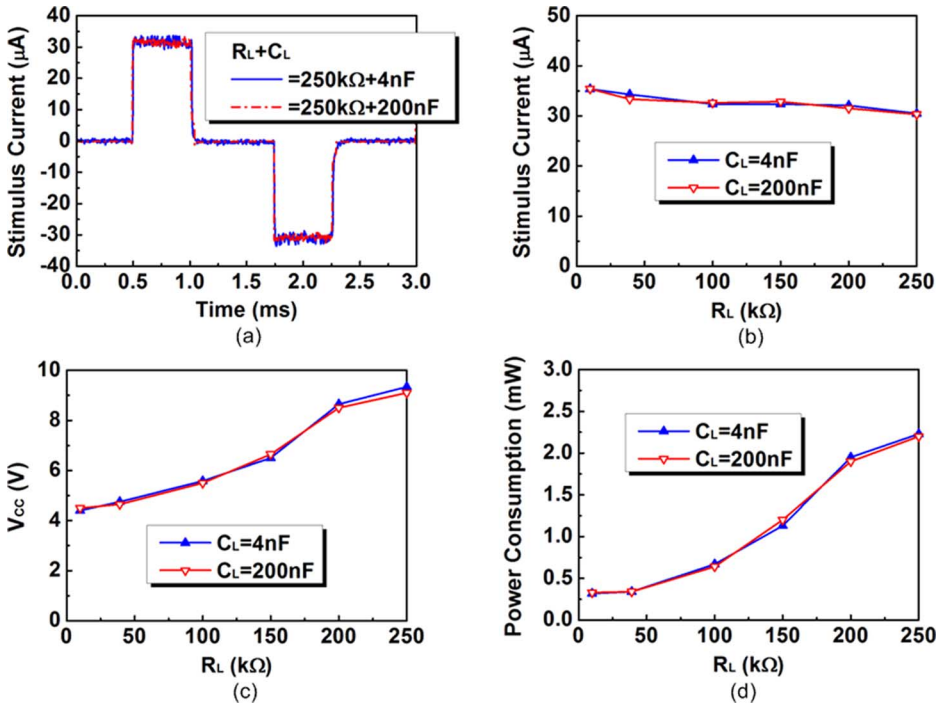

Fig. 19. (a) Measured stimulus currents with different loading impedances. (b) Measured stimulus currents under different loading impedance. (c) Measured $V_{\rm CC}$ under different loading impedance. (d) Measured power consumption under different loading impedance.

ENOB is 9.57 b with power of 3.0 μW per channel. The measured INL/DNL of the DMSAR ADC is 0.32/0.08 LSB.

Fig. 19(a) shows the measured stimulus currents passing through the loading impedance. A 250 kΩ resistor and a 4 nF/200 nF capacitor are used to represent the electrode and brain tissue. The measured stimulus current, $V_{\rm CC}$, and total power for various loading impedances are shown in Fig. 19(b)-(d). As can be seen from Fig. 19, the stimulus current is limited within 30–35 μA. The proposed stimulator can be operated at a lower operating voltage and consumes less power for lower loading impedances.

The MedRadio-band transceiver was tested at a data rate of 4 Mbps through the 401–406-MHz band. Fig. 20 shows the transmitted packet to the TX port, the modulated OOK signal received at the RX port, and the recovered signal from the RX. From Fig. 20, the encoded OOK signal is transmitted and recovered to the original signal at RX. The output power of the TX is −17.2 dBm and the sensitivity is −45.7 dBm. With a data rate of 4 Mbps, the energy-per-bit of the TX and RX is 0.16 and 0.07 nJ/b, respectively.

Fig. 21 shows the received waveform of the secondary coil, comparator output in the active rectifier, and the output of the active rectifier in the inductive link power supply system. The amplitude of the signal received by the receiver coil is 2.45 V. After being rectified, the output DC voltage becomes 2 V with 10.2 mV ripples. The LDOs regulate the noisy voltage to sustain a steady voltage of 1.8 V with 5.9/72.4/1.4 $\rm mV_{p-p}$ in ALDO/DLDO/RLDO regions.

The power consumption of the proposed SoC is 2.8 mW, and the system-level power breakdown is shown as Fig. 22. The chip performance is summarized in Table I.

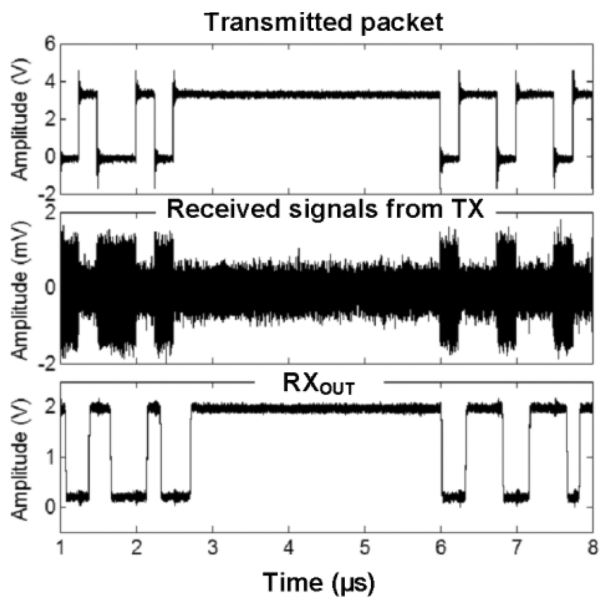

Fig. 20. Measured waveforms of the transmitted packet signal to the TX, the received signal at RX, and the recovered signal.

B. Animal Experiment

Four adult Long-Evans rats were tested in this study. All surgical and experimental procedures were reviewed and approved by the Institutional Animal Care and Use Committee of National Cheng Kung University, and all experiments comply with NIH (USA) recommended guidelines on the ethical use of animals. Based on the system verification results, the SoC is used in a microsystem setup and applied to the animal experiment.

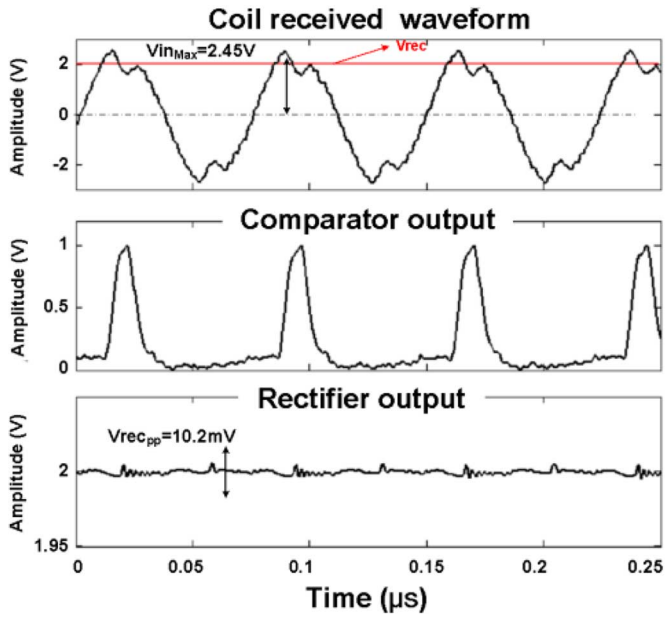

Fig. 21. Measured waveforms of the received signal of the secondary coil, comparator output in the active rectifier, and the output of the active rectifier in the inductive link power supply system.

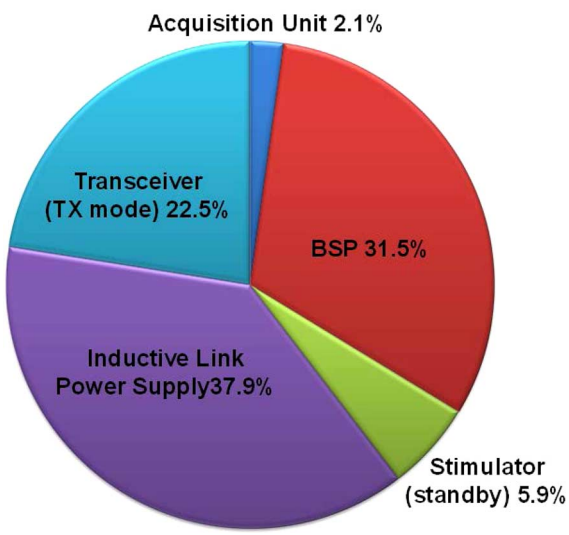

Fig. 22. System-level power distribution pie-chart.

TABLE I
PERFORMANCE SUMMARY

Process	TSMC 0.18μm 1P6M CMOS	
Area	2.76mm x 4.88mm	
AFE	Gain	41-61dB
	High-pass f_{3dB}	0.1-10Hz
	Low-pass f_{3dB}	0.8k-7kHz
	NEF	1.77 (ARCCIA)
DMSAR ADC	ENOB	9.57b @ 500kS/s
	INL/DNL	0.32/0.08 LSB
BSP	Accuracy	92%
	Latency	0.8s
	Energy per detection	77.91μJ
Stimulator	Stimulation mode	Biphasic
	Stimulation Current	30μA
Transceiver	Energy-per-bit	0.16nJ/bit (TX)
		0.07nJ/bit (RX)
Rectifier	Power efficiency	84.82%
ALDO	Current efficiency	95.93%
	Load Regulation	0.21V/A

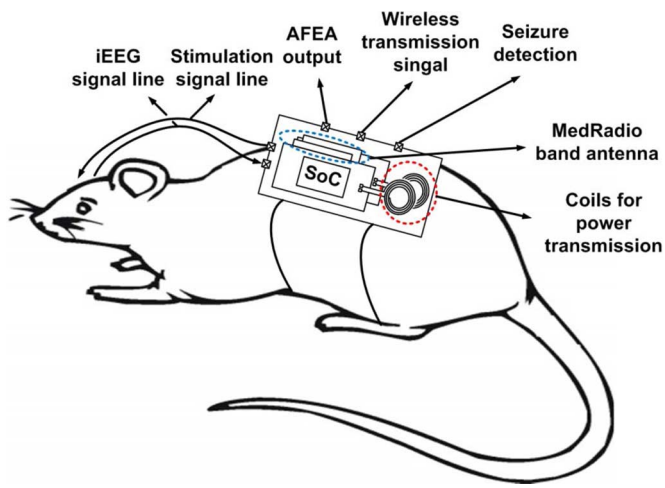

Fig. 23. Measurement setup of the microsystem with SoC on a freely moving Long-Evans rat.

The system was tested in Long-Evans rats with spontaneous spike-wave discharges (SWDs) [35], [36].

Numerous aspects of face validity on spontaneous SWDs in Long-Evans rats have indicated their association with absence seizures of humans, including bilateral synchronous SWDs coincident with minor whisker twitching during sudden immobility [36], [37], SWDs frequently occurring at transients between vigilance states [36], unresponsiveness to mild stimuli during SWDs [36], [38], and comorbidity with anxiety and depression [39], [40]. Moreover, predictive validity, including reducing SWD occurrence frequency by ethosuximide, valproic acid, diazepam, and lamotrigine, increased SWD occurrence frequency by carbamazepine with a dose-related manner, is found in SWDs of Long-Evans rats [35], [39]–[41]. Additional construct validity exists on pathological deficit in the thalamocortical neurons of Long-Evans rats [42].

Bilateral iEEG electrodes were implanted inside Long-Evans rats under pentobarbital anesthesia to record frontal cortical activities. Teflon-insulated stainless steel microwires (#7079, A-M Systems) were inserted into the zona incerta (ZI) of Long-Evans rats. The ZI has been demonstrated in actively modulating spontaneous SWDs [30]. Dental cement was applied to fasten the connection socket to the surface of the skull. Following suturing to complete the surgery, animals were given antibiotics (chlortetracycline) and housed individually in cages for recovery. In particular, a high-frequency (800 Hz)

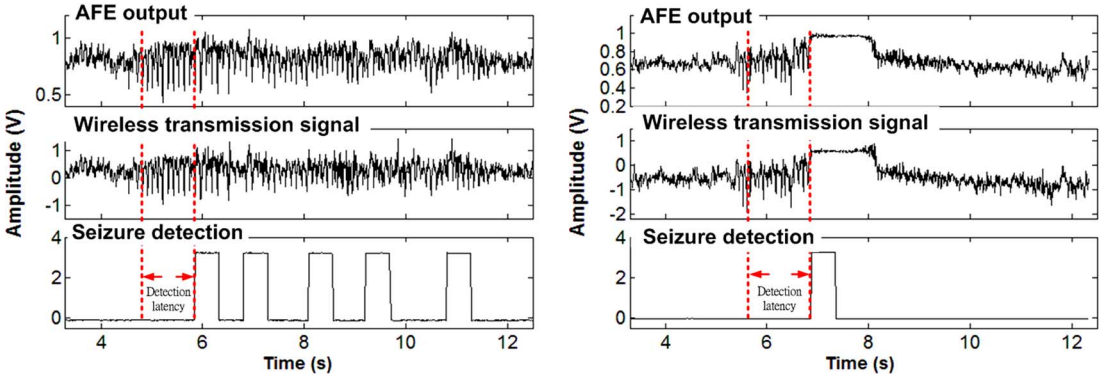

Fig. 24. Spontaneous spike-wave discharges at the output of the analog front-end amplifier (AFEA), digitized wireless transmission signal with the (a) absence and (b) activation of ZI stimulation.

TABLE II
COMPARISON WITH PUBLISHED WORKS

	This Work	[7]	[8]	[9]
NEF	1.77	5.1	n.a	2.68
ENOB	9.57	n.a	×	9.2
Accuracy	92%	84.4%	100.0%	n.a
Latency	0.8s	< 2s	13.5s	n.a
Efficiency	77.91μJ/ (feature ext. + classification)	2.03μJ/ classification	×	n.a
Stimulation	biphasic (constant 30μA)	×	×	Monophasic/Biphasic (0-94.5μA/6b)
Wireless data transmission	OOK modulation (401-406 MHz)	×	×	FSK modulation (433MHz)
Wireless power link	ISM band power transmission	×	×	×

stimulation of the ZI has been demonstrated to stop SWDs successfully [19], [21].

Fig. 23 shows the measurement setup of the microsystem with SoC on a freely-moving Long-Evans rat. For the animal experiment, the antenna for the MedRadio-band transceiver is of planar type with a size of 1.3 cm × 2.7 cm. The secondary coil for the inductive link power supply has a diameter of 2.7 cm. The microsystem with SoC was tested 72 h and powered wirelessly. It connects to the implanted electrodes in the brain for signal acquisition and for electrical stimulation. Fig. 24 shows the received and digitized iEEG waveforms of the spontaneous SWDs. Fig. 24(a) shows the case when the stimulator is turned off. As can be seen the epileptic seizures are detected successfully during a SWD period. When the stimulator is turned on, the seizures are suppressed through the closed-loop control, as shown in Fig. 24(b). From Fig. 24(a), the detection latency is around 1s. In a long-term animal experiment, the latency can be decreased to 0.8 s. Note that once the seizure is detected by the circuit, the signal of detection which is also used as the stimulation activation signal, is designed to be activated for 0.48 s and then cleared to low to start a new detection/stimulation cycle to avoid excessive stimulation. The performance comparison of the proposed SoC with recent works [7]–[9] is given in Table II.

V. CONCLUSION

An 8-channel closed-loop neural-prosthetic SoC has been implemented to perform real-time seizure-triggered neuromodulation. Entropy-and-spectrum-aided seizure detection and adaptive neural stimulation have been also presented. The SoC integrates eight AFEAs, a DMSAR ADC, a bio-signal processor, and an electrical stimulator. The AFEA features with configurable gain and bandwidth. The DMSAR ADC operates at 500 kSamples/s with an ENOB of 9.57 b. The BSP implements an efficient seizure detection algorithm and achieves more than 92% detection accuracy in 0.8 s. The stimulator delivers a constant 30-μA stimulation current. In addition, a wireless power-and-data transmission system including a MedRadio-band transceiver and an inductive link power supply system, has been embedded for signal monitoring and wireless power transmission. It has been demonstrated that the proposed SoC is able to successfully suppress epileptic seizures of Long-Evans rats. Based on the preliminary results,

the developed closed-loop seizure control SoC is a promising solution for treating epilepsy. For future applications on human implants, the chip package, antenna, and coils will be carefully designed to meet all of the system performance and regulatory requirements.

ACKNOWLEDGMENT

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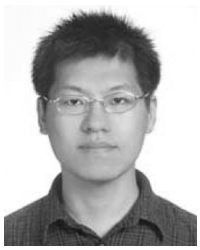

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