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Investigation of p-type junction-less independent double-gate poly-Si nano-strip transistors

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Abstract

In this study, novel independent double-gate (IDG) junction-less (J-less) polycrystalline silicon (poly-Si) nano-strip transistors have been fabricated and investigated. Inversion-mode (IM) IDG poly-Si nano-strip transistors with the undoped channel have also been fabricated for comparison. The experimental data show the superior on-state current of J-less transistors over that of IM transistors mainly due to the reduction of the channel resistance (R_{ch}). However, the drain-induced barrier lowering of the J-less transistors is larger than that of IM transistors but the double-gate (DG) configuration can mitigate this problem to some extent. Besides, the subthreshold swing and its fluctuation of the J-less transistors are worse than those of IM transistors under the single-gate operation. Fortunately, this issue can be significantly improved by the aid of DG configuration according to our experimental results. We also demonstrate the possibility of changing the threshold voltage (V_{th}) under IDG operation for the J-less IDG nano-strip transistors.

Keywords: independent double-gate, junction-less transistor, poly-Si, nanowire, p-type, output characteristics, subthreshold characteristics

(Some figures may appear in colour only in the online journal)

1. Introduction

One of the most difficult challenges of the scaling of conventional inversion-mode (IM) metal-oxide-semiconductor field-effect transistors (MOSFETs) is the seriously deteriorated short channel effects (SCEs) [1]. In order to overcome such issues, the ultra-sharp and ultra-shallow source/drain (S/D) junctions are essential. However, this solution poses the rigid constraints regarding the doping techniques and the thermal budgets [2, 3]. As a result, the junction-less (J-less) transistor has been proposed as the alternative candidate which adopts the ultra-thin and heavily doped channel with the same doping type as the S/D regions [4–7]. Because of the absence of the S/D junctions, the J-less transistors are free from the sophisticated process to form the ultra-sharp and ultra-shallow S/D p–n junctions. Thus, an easier fabricating process with lower thermal budget and lower output resistance are expected [8]. Such advantages make the J-less transistors particularly suitable to be applied in future 3D multiple stacked integration circuits compared to the conventional IM transistors. For example, for flash memory with 3D architecture [9, 10], the degradation of the current flowing through a string of NAND flash memory due to the high series resistance using the conventional IM transistors can be mitigated by using J-less transistors. On the other hand, in order to effectively turn off the heavily doped channel of the J-less transistors, multiple-gate (MG) configuration is proposed to effectively control the electrostatic potential within the ultra-thin channel. Most of the previous studies put emphasis on devices with gate-tied MG structures including the tri-gate [4–7] and the gate-all-around configurations [8, 11]. But the independent double-gate (IDG) structure

has also started to draw a lot of attention owing to the more flexible operations which can be applied in the basic logic circuits [12, 13] or the cells of the string of NAND flash memory to improve the read-disturbed problem [14, 15] by the back-gate bias effect. In this work, we have demonstrated a novel p-type polycrystalline silicon (poly-Si) nano-strip J-less transistor with the IDG configuration. Meanwhile, the p-type IM IDG poly-Si nano-strip transistors with the undoped channel have also been fabricated as the control group. This paper is organized as follows. In section 2, we introduce the fabricating process of the IDG p-type J-less poly-Si nano-strip transistors. In section 3, the transfer characteristics of the J-less transistors will be presented and discussed. In section 4, the output characteristics of the J-less transistors will be investigated. In section 5, the subthreshold characteristics of the J-less transistors will be examined. The conclusions will be drawn in the final section.

2. Device fabrication

Figure 1 shows the schematic process flow of the proposed p-type J-less IDG poly-Si nano-strip transistor, which basically follows the process of the previously published n-type IDG poly-Si nano-strip transistor [16]. First, a 60-nm-thick SiN layer was deposited on 100-nm-thick thermal oxide which grew on the silicon wafer. Because of the p-type channel doping, the J-less transistors require the gate material with a low work function such as n^+ poly-Si in order to achieve a suitable threshold voltage (V_{th}) which is not too positive for p-type transistors. The V_{th} in this work is defined as the gate voltage when the drain current is 10 nA. Thus, 100-nm-thick *in situ* doped n^+ poly-Si and 50-nm-thick SiN were deposited sequentially to serve as the first gate stack. After the first gate stack patterning (step (i)), highly selective plasma etching between poly-Si and SiN was used for the lateral etching of the first poly-Si gate (step (ii)). Then 10-nm-thick TEOS oxide and 100-nm-thick amorphous Si were deposited and subsequently underwent 600 °C annealing in N_2 ambience for 24 h which transformed the amorphous Si into poly-Si (step (iii)). After the BF_2^+ implant with a dose of 5×10^{14} cm^{-2} (step (iv)), the samples were annealed in N_2 ambience at 900 °C for 30 min to drive the dopants into the nano-strip channels (step (v)). Since the poly-Si film is 100-nm-thick, the nominal nano-strip doping concentration is expected to be 5×10^{19} cm^{-3}. However, due to the light mass of boron atoms, a notable portion of doped boron atoms would not remain in the poly-Si film after the annealing. Based on our process experience and TCAD simulation, we estimate that the actual nano-strip doping concentration is around 5×10^{18} cm^{-3} which is approximately one tenth of the nominal value. To further reduce the S/D resistance, an additional S/D doping was performed by implanting BF_2^+ at a dose of 5×10^{15} cm^{-2} (step (vi)). To avoid the possible boron diffusion into the nanostrips, the dopant activation was done by the thermal budget of the following processes. The boron diffusion from the S/D regions into the nanostrips should be insignificant since the highest temperature of the subsequent thermal budget is merely 700 °C in the TEOS

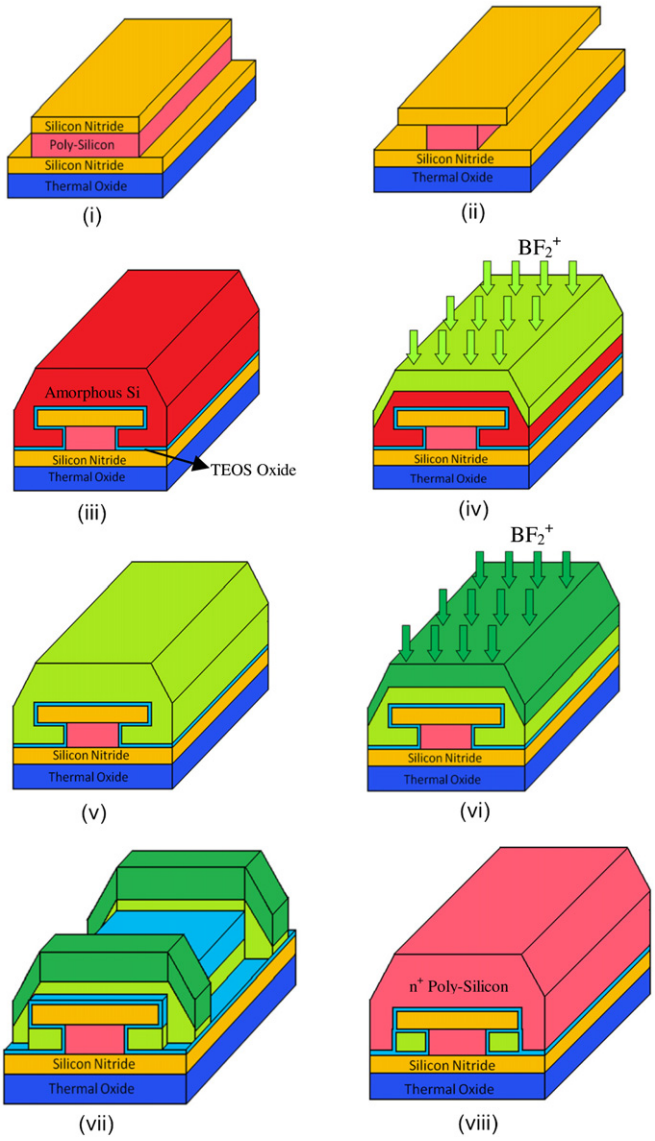
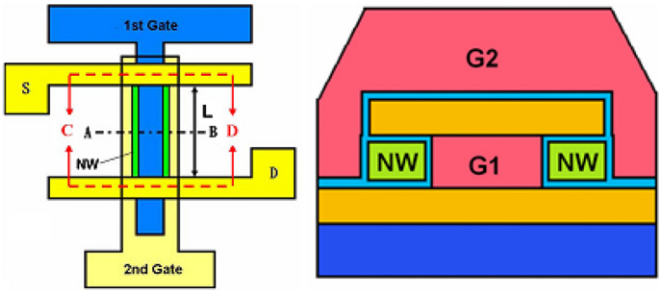


Figure 1. Schematic process flow of the p-type IDG J-less poly-Si nano-strip transistor.

oxide deposition step and its time is about 1 h. We defined the channel and S/D regions by reactive ion etching (step (vii)). The second gate stack consisting of 10-nm-thick TEOS oxide and the subsequent 100-nm-thick *in situ* doped n^+ poly-Si was deposited and followed by patterning (step (viii)). A 200-nm-thick oxide layer was deposited as the passivation layer. After digging the contact holes, the J-less transistors were completed after the metallization process. For the IM transistors which have the undoped channel in this work, the fabrication flow is similar to that of the J-less transistors except that steps (iv) and (v) are omitted. The layout of the p-type IDG J-less poly-Si nano-strip transistor is shown in figure 2(*a*). Figure 2(*b*) is the cross-section view of the device along the dot-dashed line A–B in figure 2(*a*). Two poly-Si nanostrips are surrounded by 10 nm gate oxide and embedded in the ultra-thin cavities underneath the nitride hard mask as shown in figure 2(*b*). Note that the first gate (G1) is the n^+ poly-Si gate between the two nanostrips and the second gate (G2) is the n^+ poly-Si gate outside the two nanostrips. The transmission electron microscopic (TEM)



(*a*) (*b*)

Figure 2. (*a*) Top and (*b*) cross-section views of the p-type IDG J-less poly-Si nano-strip transistor.

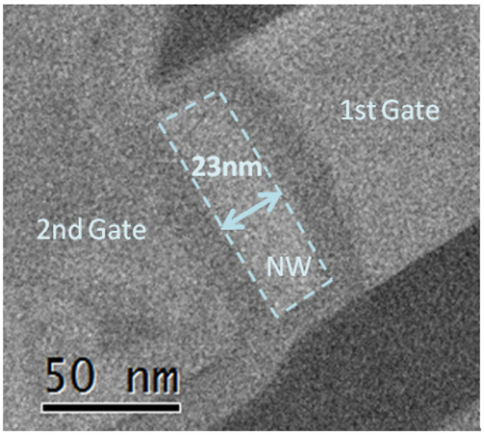


Figure 3. The cross-section TEM image of one of the p-type IDG J-less poly-Si nano-strip transistors.

image of the cross-section view of one of the fabricated J-less transistors are given in figure 3. The lateral channel thickness (T_{si}) of the rectangular poly-Si nanostrip was observed to be 23 nm for this J-less transistor.

3. Transfer characteristics

Due to the unique feature associated with two independent gates in the proposed structure, the device operations of J-less and IM transistors can be categorized into SG-1, SG-2, and DG modes defined as the following. The SG-1 or SG-2 mode denotes, respectively, the scheme when the first or second gate serves as the driving gate while the other gate electrode is the control gate which is grounded by default. In the DG mode, both gates are connected together as the driving gate. The I_D–V_G curves at $V_D = -0.5$ V under the three operation modes of one of the fabricated J-less transistors with the channel length (L_G) of 2 μm is shown in figure 4. Due to the ultra-thin thickness (about 20 nm) of the poly-Si nanostrip, as shown in figure 3, the J-less transistor can be effectively turned off. Good switch ability with the subthreshold swing (SS) of 176 mV dec^{-1} under the DG mode can be achieved for the J-less transistor. The worse SS observed in the J-less transistor operating in the SG-1 mode can be attributed to the ungated region between S/D and the conducting channel as discussed in [16]. There are notable gate-induced drain leakage currents for the J-less transistor since the band-to-band tunnelling current is not only contributed by the gate

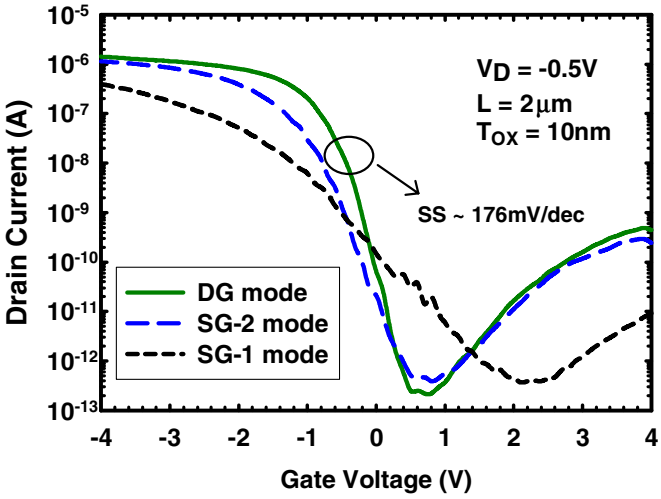


Figure 4. The I_D–V_G characteristics under $V_D = -0.5$ V of one of the J-less transistors with $L_G = 2$ μm.

oxide/drain overlapped interface (2D problem) [17] but also the whole gated nano-strip drain region (3D problem) [18]. Figures 5(*a*)–(*c*) show the I_D–V_G curves at $V_D = -0.5$ and -2 V of one of the J-less transistors with $L_G = 2$ μm under the SG-1, SG-2, and DG mode, respectively. Similar to the traditional IM transistors, we can define the drain-induced barrier lowering (DIBL) as the V_{th} difference between $V_D = -0.5$ and -2 V. Comparing with the IM nano-strip transistors [16], the DIBL of the J-less transistors is large even for the long channel devices ($L_G = 2$ μm) since there is inherently no barrier between source and drain for the J-less transistors and any variation on the drain bias will directly influence the drain current. Nevertheless, the DG mode has lower DIBL than the SG modes, which indicates that, to a certain extent, the MG configuration can alleviate the DIBL problem of the J-less transistors.

4. Output characteristics

One major advantage of the J-less transistors is the remarkable improvement in the on-state current comparing with the IM transistors and this will be verified experimentally in this work. The superior output characteristics of the typical J-less transistors with the long ($L_G = 2$ μm) and short ($L_G = 0.7$ μm) channel are demonstrated in figures 6(*a*) and (*b*), respectively. Note that, to take care of the device variations, here we showed the output characteristics of the sample whose saturation current is the median of the distribution for each kind of devices. Comparing with the control devices (IM transistors), the enhancements of the on-state current of the J-less transistors with $L_G = 2$ μm and $L_G = 0.7$ μm are up to 328% and 198%, respectively, at the gate overdrive of 4 V. The superior output characteristics result in the lower total output resistance (R_{tot}) which can be divided into two parts: the S/D series resistance ($R_{S/D}$) and the channel resistance (R_{ch}). The $R_{S/D}$ and R_{ch} can be experimentally extracted by varying the channel length. The total resistance as a function of the channel length of the J-less and IM transistors are shown in figures 7(*a*) and (*b*), respectively. Again, to take care of the device variations, the total resistance is extracted

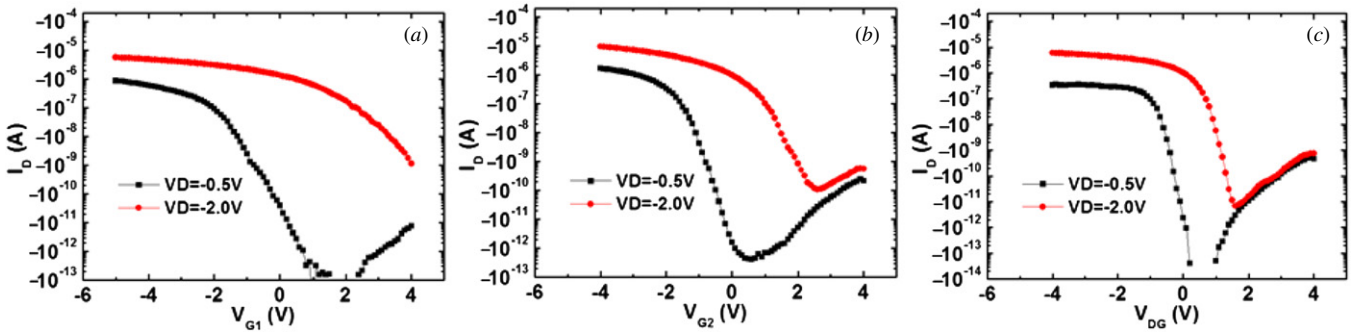


Figure 5. The I_D–V_G curves at $V_D = -0.5$ V and -2 V of one of the J-less transistors with $L_G = 2$ μm under the (*a*) SG-1, (*b*) SG-2, and (*c*) DG mode.

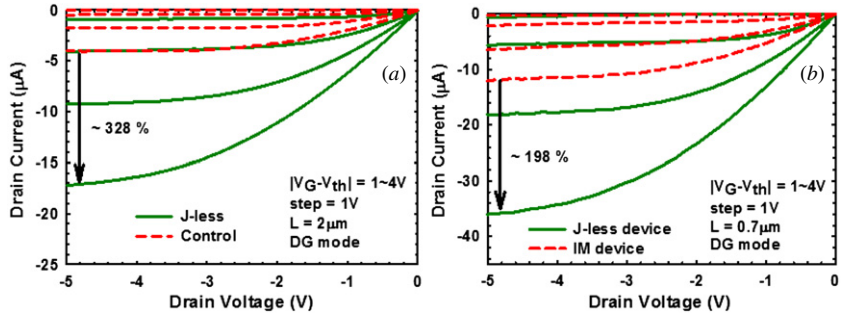


Figure 6. Comparison of the output characteristics between the typical J-less and IM transistors with the channel length of (*a*) 2 μm and (*b*) 0.7 μm.

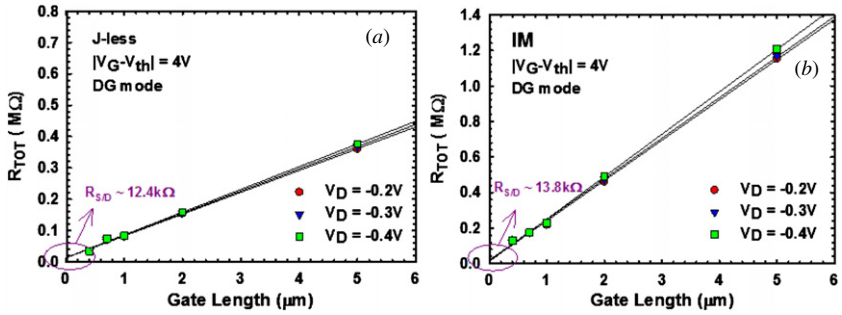


Figure 7. The extracted total resistance versus the gate length for (*a*) J-less and (*b*) IM transistors with the gate overdrive of 4 V under the DG mode.

from the sample whose saturation current is the median of the distribution for each kind of devices. The total resistance is almost independent of the applied drain bias ($V_D = -0.2$, -0.3, and -0.4 V), which implies, within this V_D range, the I_D–V_D relationship is linear (this can also be verified by figure 6). Therefore, we directly extracted the $R_{S/D}$ by extrapolating the curves to $L_G = 0$ μm (R_{ch} approaches zero) without consulting multiple gate overdrives which should give almost the same $R_{S/D}$. The values of $R_{S/D}$ are 12.4 and 13.8 kΩ for the J-less and IM transistors, respectively. About 10% reduction of $R_{S/D}$ for the J-less devices is speculated owing to the lower spreading resistance resulting from the elimination of S/D junctions. The significant reduction of R_{tot} is mainly contributed by the improvement of R_{ch} as shown in figure 8. The R_{ch} of the J-less transistors are about one third of those of the IM transistors. When the devices are turned on, the conduction current density across the nano-strip cross section of the J-less transistor is more uniform than that of the IM transistor whose conduction relies on the inversion layer. Hence, the surface roughness scattering and the transverse electric field in the J-less transistors can be greatly reduced and consequently lower R_{ch} can be obtained. As the L_G is scaled down, the absolute reduction value of R_{ch} decreases. This is why the enhancement of the on-state current of the J-less transistor decreases from 328% to 198% as the L_G is reduced from 2 μm to 0.7 μm.

5. Subthreshold characteristics

Since the subthreshold characteristics have been considered to be the weaknesses of the J-less transistors, here we will examine the subthreshold characteristics of the J-less transistors under the DG and SG operation modes. The SS statistics of the J-less and IM transistors, extracted from ten samples with $L_G = 1$ μm under the SG-2 and DG operation modes, are shown in figures 9(*a*) and (*b*), respectively. Note

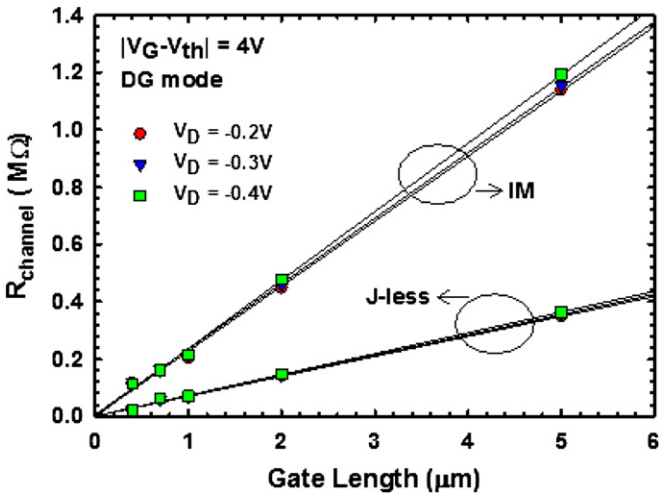


Figure 8. Comparison of the channel resistance versus the gate length between the J-less and IM transistors with the gate overdrive of 4 V under the DG mode.

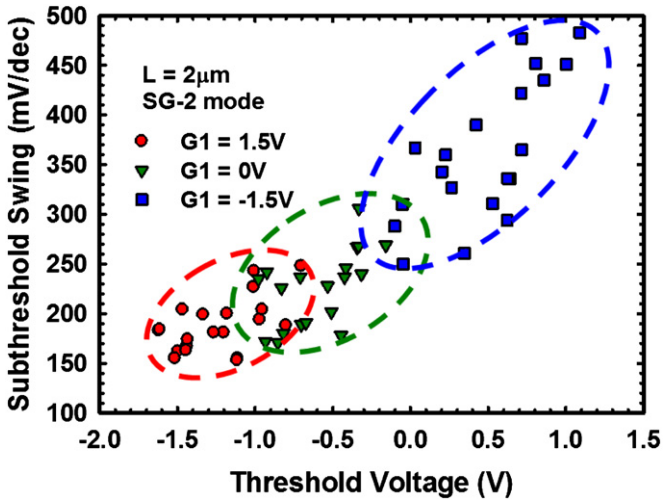


Figure 10. The SS versus V_{th} plot measured from the same 20 samples under the SG-2 mode with $V_{G1} = 1.5, 0, -1.5$ V. The drain bias is -0.5 V.

that since the SG-1 operation mode has the worst performance, here we only present the data of the SG-2 and DG operation modes. Under the SG-2 mode, mainly due to the process variation on the channel doping concentration of the J-less transistors (about 5×10^{18} cm^{-3} in this work), the fluctuation of the SS of the J-less transistors is larger than that of the IM transistors with the intrinsic channel [19]. In contrast to the IM transistors which are turned off by diminishing the inversion layer underneath the interface of the gate oxide and the silicon channel, the J-less transistors are turned off by gradually depleting the heavily-doped channel. Thus, the leakage current in the J-less transistors can flow through the deeper part of the silicon channel and thus degrades the SS. Fortunately, this drawback could be significantly improved by the aid of the DG configuration, as shown in figure 9(*b*). The reduction of the SS and its fluctuation for the J-less transistors is because that the channel is depleted by both gates and thus the leakage current is greatly reduced. Figure 9(*b*) also suggests that the bias of the control gate (i.e. the gate opposite to the driving gate) will play an important role in reducing the SS and its fluctuation for the J-less transistors. The impact of the control gate voltage of the J-less transistors on the SS and its fluctuation was experimentally examined. Figure 10 shows the SS versus V_{th} plot of the J-less transistors measured from 20 samples with $L_G = 2$ μm under the SG-2 mode with the G1 biases of 1.5, 0, and -1.5 V. The V_{th} and SS fluctuations are mainly caused by the process variations, especially the variations on the channel doping and the nano-strip thickness as indicated in [19]. Furthermore, both V_{th} and SS as well as their fluctuations are decreased as the control gate voltage of G1 increases. This trend can be explained by the 3D TCAD simulation results [20]. Figures 11(*a*)–(*c*) show the hole distributions across the nano-strip cross section at the middle channel for the J-less transistor operating at the SG-2 mode with the G2 bias equal to the V_{th} under $V_{G1} = 1.5, 0, -1.5$ V, respectively. In the TCAD simulation, the drift-diffusion (D-D) model serves as the transport model with the quantum correction made by density gradient model [20]. Note that the conducting carriers move away from G2 as V_{G1} decreases from 1.5 V to -1.5 V. This phenomenon can be regarded as the increment of the effective oxide thickness as the control-gate bias V_{G1} decreases. As a result, for the device operating in the SG-2 mode, V_{th} and SS as well as their fluctuations increase as V_{G1} decreases from 1.5 V to -1.5 V. In other words, a positive control-gate bias can decrease the V_{th} and SS as well as their fluctuations; however, a negative control-gate bias will increase them. Since the V_{th} of the SG-2 mode becomes more negative as the control gate bias V_{G1} becomes more positive, figure 10 also demonstrates the possibility of changing V_{th} by

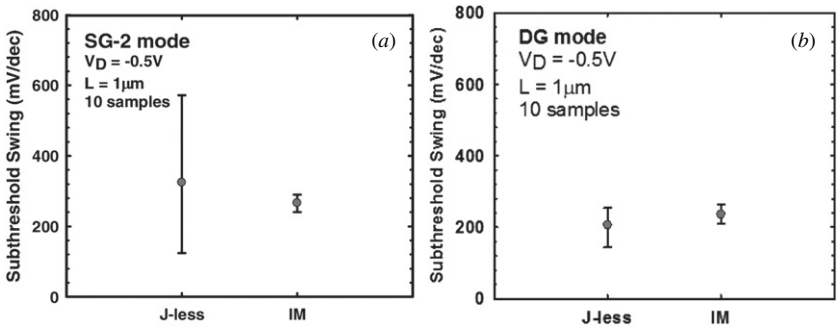
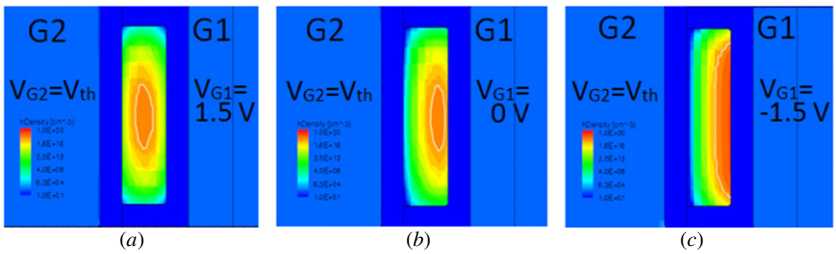


Figure 9. The SS statistics of the J-less and IM transistors operating in (*a*) SG-2 and (*b*) DG modes.



(*a*) (*b*) (*c*)

Figure 11. The hole distributions across the nano-strip cross section at the middle channel for the J-less transistor operating at the SG-2 mode with $V_{G2} = V_{th}$ under (*a*) $V_{G1} = 1.5$ V, (*b*) $V_{G1} = 0$ V, and (*c*) $V_{G1} = -1.5$ V. The drain bias is -0.5 V.

applying different control gate bias for the J-less IDG nano-strip transistors operating in single-gate mode.

6. Conclusion

A novel p-type poly-Si nano-strip IDG J-less transistor featuring rectangular-shaped and heavily doped nano-strip channel and two independently controllable gates is proposed and characterized. Such a device takes the advantage of common CMOS compatible process without resorting to the advanced and costly lithography tools. In addition, its stacking ability can potentially be applied to the 3D integrated circuits. In the work, we demonstrated its superior output characteristics comparing with the IM transistor. Such features make it especially suitable to be applied in the 3D NAND flash memory to mitigate the current degradation problem. Although the DIBL of the J-less transistors is larger than that of the IM transistors, this problem can be alleviated to a certain extent by using the DG configuration. Our experimental and simulation results also showed that the subthreshold characteristics and their fluctuation of the J-less transistors are worse than those of the IM transistors under the SG mode. Fortunately, such an issue can also be greatly improved by adopting the DG configuration. We also demonstrated the possibility of changing V_{th} under independent double-gate operation for the J-less IDG nano-strip transistors.

Acknowledgments

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