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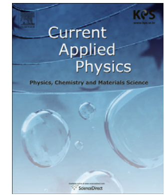

Low power resistive random access memory using interface-engineered dielectric stack of SiO_x/a-Si/TiO_y with 1D1R-like structure

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ABSTRACT

In this study, we report a resistive random access memory (RRAM) using trilayer SiO_x/a-Si/TiO_y film structure. The low switching energy of <10 pJ, highly uniform current distribution (<13% variation), fast 50-ns speed and stable cycling endurance for 10^6 cycles are simultaneously achieved in this RRAM device. Such good performance can be ascribed to the use of interface-engineered dielectric stack with 1D1R-like structure. The SiO_x tunnel barrier in contact with top Ni electrode to form diode-like rectifying element not only lowers self-compliance switching currents, but also improves cycling endurance, which is favorable for the application of high-density 3D memory.

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1. Introduction

With continued scaling down into sub-20 nm of non volatile memory (NVM), the flash NVM faces a physical limitation on charge storage in the scaled cell size [1,2]. Recently, resistive random access memories (RRAMs) [3–14] with simple metal–insulator–metal (MIM) structure and embedded function are the promising candidates for next-generation NVM. However, the large switching power and poor switching distributions are the major challenges for production. To address these issues, we have proposed low power RRAMs [11–14] based on hopping conduction mechanism [15]. Unfortunately, the current distribution related to carrier transport at the electrode/dielectric interface still cannot be well-controlled. To further improve the uniformity, 1D1R (one-diode–one-resistor) [16,17] structure is an alternative approach due to the crosstalk suppression, especially for the crossbar arrays. In this work, we adopt a novel 1D1R-like RRAM structure with good rectifying behavior to improve the switching characteristics. This RRAM device using trilayer SiO_x/a-Si/TiO_y films can achieve a low switching power of 85 μW, stable HRS/LRS ratio after repeated cycling, tight current distribution (coefficient of variation <13%) and robust pulse cycling endurance (10^6 cycles at 50 ns). The excellent switching characteristics are ascribed to the use of bilayer SiO_x/a-Si capping layer that forms a diode-like rectifying behavior (Ni/SiO_x/a-Si) to modify resistive switching characteristics of TiO_y resistor. Compared to the previous RRAM device [18] using covalent-bond oxide for uniformity improvement, the proposed low-power RRAM with 1D1R structure achieves good rectifying property to suppress the sneak current for crossbar array application. The present results show that such low-power RRAM with 1D1R-like structure design has the potential for the application of next-generation memory device.

2. Experimental procedure

First, a 200-nm-thick SiO_2 was formed on the Si substrate as a buffer layer. Then, a 100-nm-thick TaN was deposited by dc sputtering as the bottom electrodes. Next, the stacked layers of 2-nm-thick SiO_x, 6-nm-thick amorphous Si (a-Si) and 15-nm-thick TiO_y (SiO_x/a-Si/TiO_y = 2/6/15) were deposited as resistive switching layers. To investigate the switching function of each layer, we also deposit different thickness ratios of SiO_x/a-Si/TiO_y (3/6/15, 2/8/15 and 2/6/18) on bottom TaN for performance comparison. Because the thickness increase on SiO_x and a-Si layers would generate strong serial resistance effect and apparently affect the resistive switching (fast resistance window shrinking), we only select optimized thickness ratios for a fair comparison to investigate the switching mechanism and current distribution characteristics here.

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Finally, a 50-nm-thick Ni was deposited and patterned to form the top electrode by a metal mask. The schematics of fabrication process are shown in Fig. 1. All electrical characteristics of the fabricated devices were measured by an Agilent 4156 semiconductor parameter analyzer.

3. Results and discussion

For typical RRAM devices, the resistance changes from high-resistance state (HRS) to low-resistance state (LRS) during set process and returns to HRS during reset process. To study the switching characteristics of the Ni/TiO_y/TaN RRAM device, Fig. 2(a) shows the current–voltage (I–V) curve. The forming-free and self-compliance characteristics for set and reset processes are measured. The asymmetric I–V curves is originated from the different work functions of the bottom TaN (4.6 eV) and top Ni (5.1 eV) electrodes. The TiO_y RRAM device is biased at 2.5 V for set with a LRS current of 0.9 mA. For the reset process, the LRS is recovered to HRS using a bias of −2 V (36 μA). The large set current of 0.9 mA induces high power consumption and also leads to an unstable resistance switching during cycling, which is unsuitable for the requirement of low power operation. Fig. 2(b) shows the repeated cycling result after 50 cycles. During set process, the defective TiO_y with narrow bandgap generates a low barrier potential at the TiO_y/TaN interface, which induces easy formation of leakage paths and thus increases HRS current. The fast degradation of HRS current under stress leads to poor endurance. The increased HRS current with pulse cycles would result in a fast window shrinking that is not permitted for RRAM device.

To improve the performances of TiO_y RRAM, we adopted a film stack of SiO_x/a-Si on TiO_y to form a 1D1R-like memory structure. The Ni/SiO_x/a-Si acts as a doide-like rectifying element where the ultra-thin SiO_x layer is used as tunneling barrier. As shown in Fig. 3(a), the Ni/SiO_x/a-Si/TiO_y/TaN RRAM can be set and reset by different bias conditions. Although the HRS/LRS ratio read at −0.5 V becomes larger with increasing set and reset voltages from 2 V to 3 V, the tradeoff between HRS/LRS ratio and switching power needs to be considered for practical application. Moreover, the rectification behavior is clearly observed in LRS. Compared to single TiO_y RRAM, this RRAM using SiO_x/a-Si film stack with diode-like function largely lower set power from 2.3 mW to 84 μW and reset power from 72 μW to 1 μW. The improvement on switching power is due to the rectifying effect of SiO_x tunnel barrier. The rectifying 1D1R-like structure is also favorable for the fabrication of high-density crossbar array. Fig. 3(b) shows the continued cycling result after 100 cycles in Ni/SiO_x/a-Si/TiO_y/TaN RRAM. Apparently, the switching stability of HRS and LRS is much improved through the incorporation of diode-like Ni/SiO_x/a-Si structure.

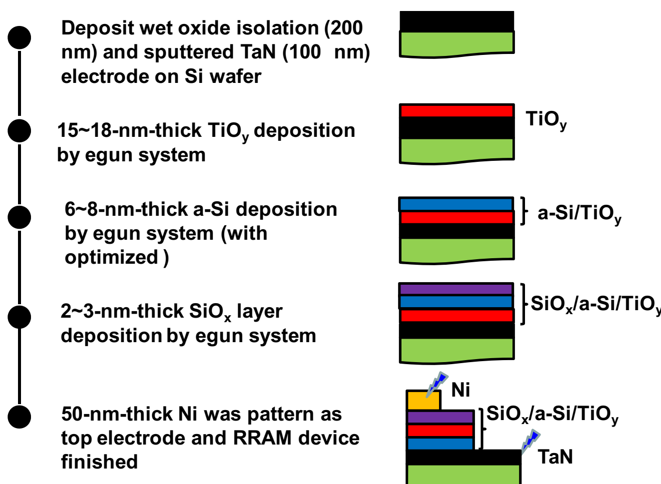


Fig. 1. Schematics of fabrication process of Ni/SiO_x/a-Si/TiO_y/TaN RRAM.

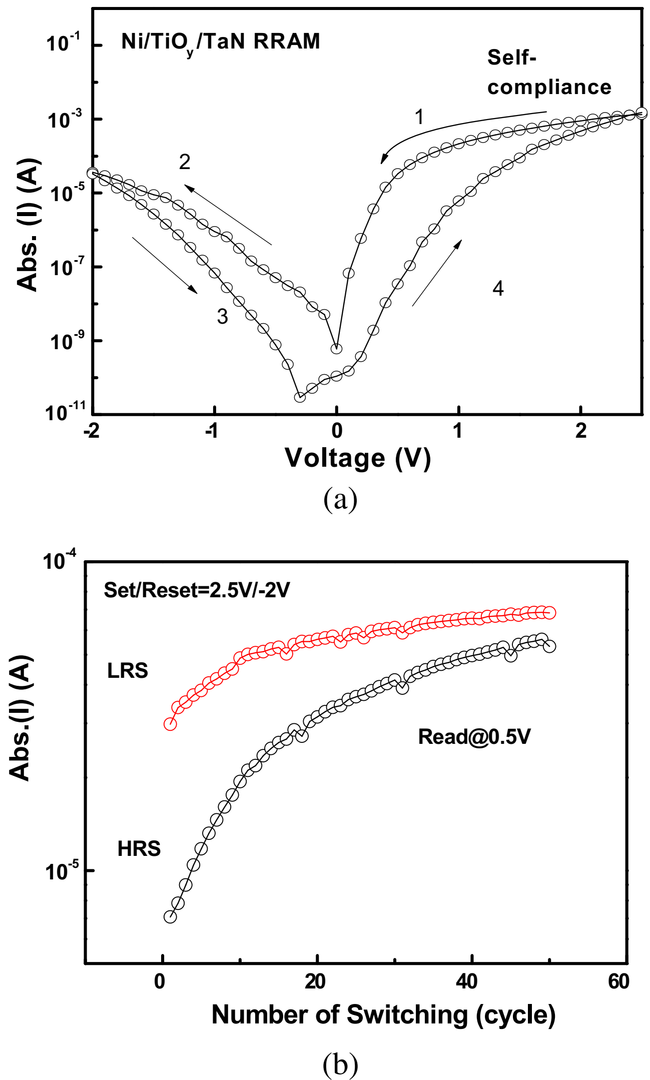
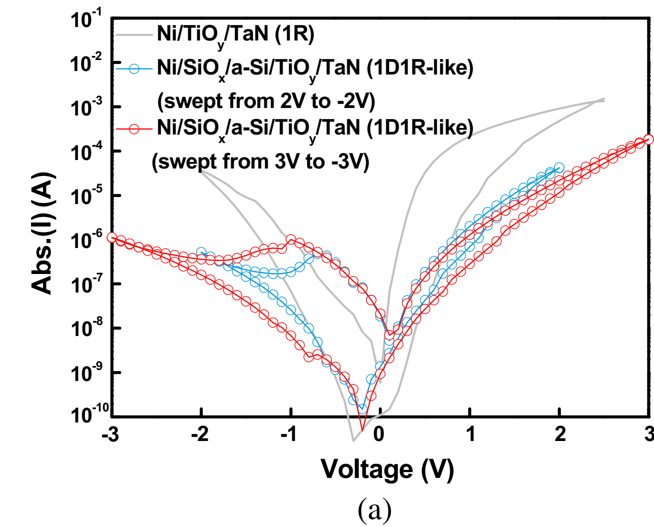


Fig. 2. (a) Swept I–V and (b) repeated cycling characteristics of Ni/TiO_y/TaN RRAM devices.

To further study the conduction mechanism, we plotted the schematic band diagrams under set and reset conditions in Fig. 4. During the set process with a positive voltage, the charged oxygen vacancies are formed via injected electrons from the bottom TaN electrode. The bottom injection of electron carriers from TaN electrode can pass through SiO_x tunnel barrier to form a LRS current. Here, the metal/tunnel barrier (Ni/SiO_x) contact plays a key role to provide the self-compliance function for set process. According to our previous research results, the low self-compliance LRS current not only lowers set power, but also improves the switching uniformity [18]. Under a negative reset bias, the SiO_x tunnel barrier with high conduction band offset forms a large potential barrier (in contact with top Ni) to break conductive paths in LRS and fast recover to HRS at a low driving power of micro-Watt. Thus, the combined effect of electrode work function tuning and interface-engineered dielectric stacks is important to reduce switching power.



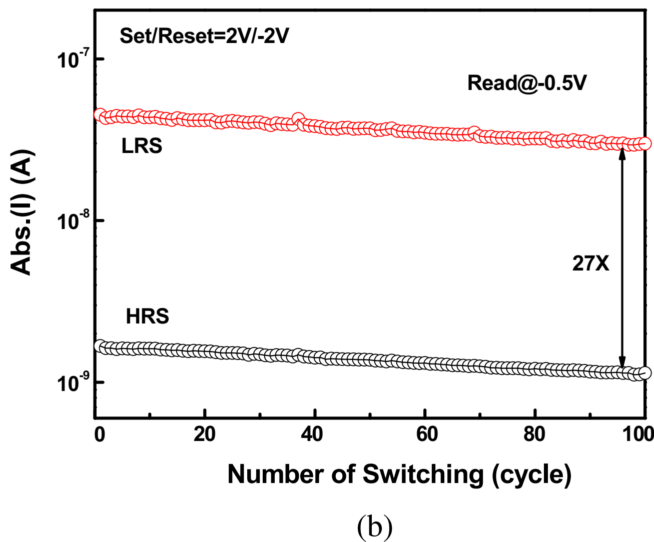


Fig. 3. (a) Swept I–V and (b) repeated cycling characteristics of Ni/SiO_x/a-Si/TiO_y/TaN RRAM devices.

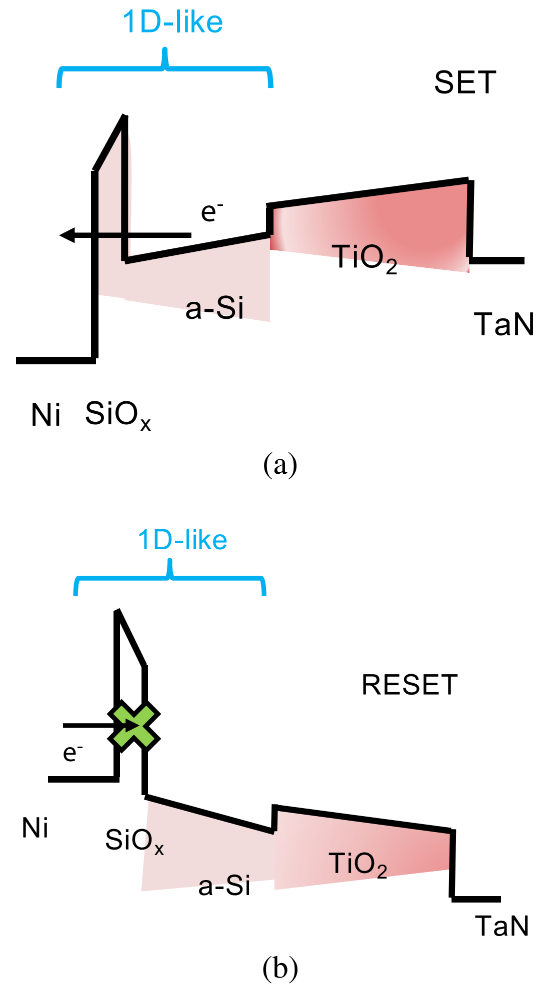
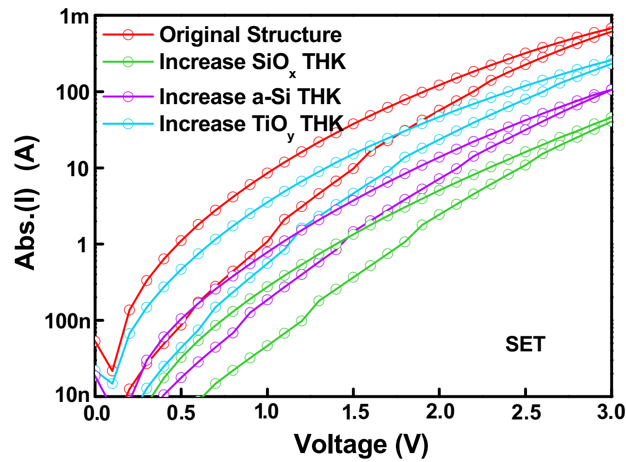


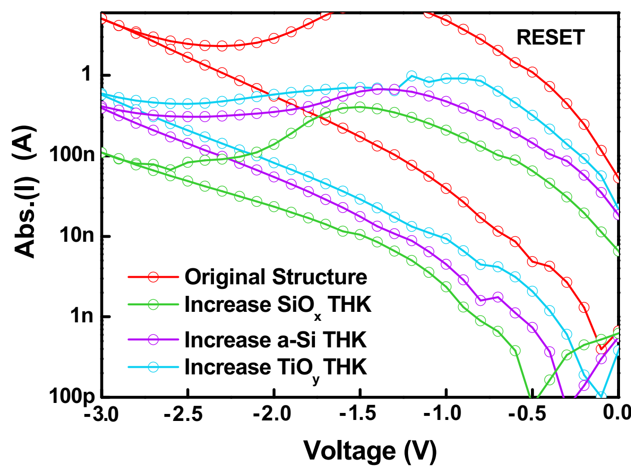
Fig. 4. Schematic energy band diagrams under set and reset conditions.

To further study the switching function of each layer, the RRAM devices with different thickness (THK) for SiO_x, a-Si and TiO_y are also fabricated. The thickness ratios of trilayer SiO_x/a-Si/TiO_y are 3/6/15 (increment of SiO_x THK), 2/8/15 (increment of a-Si THK) and 2/6/18 (increment of TiO_y THK), respectively. Fig. 5(a) and (b) shows the swept I–V curves of RRAM devices with different THK conditions. In comparison with original structure, the set current decreases with THK increment of each layer, especially for large bandgap SiO_x. This result proves that the SiO_x tunnel barrier dominates the self-compliance set current, even only a slight THK increment (~1 nm). Correspondingly, the lowest reset current of 100 nA is also measured for the case of increased SiO_x THK in opposite bias direction, but accompanies with severe interface trapping that is clearly observed near zero bias. The interface trapping phenomena near SiO_x tunnel barrier may lead to a decreased LRS current due to electron pile-up during cycling and finally shrink memory window. Fig. 5(c) summarizes the forward–reverse ratios of different thickness conditions. From the rectifying characteristics, the 404× of increased TiO_y THK case is better than 368× of increased SiO_x one, indicating that the thickness tuning of TiO_y with very high dielectric constant (>40) [19] to modify interface electric field is an appropriate approach to achieve both good rectifying property and low switching power.

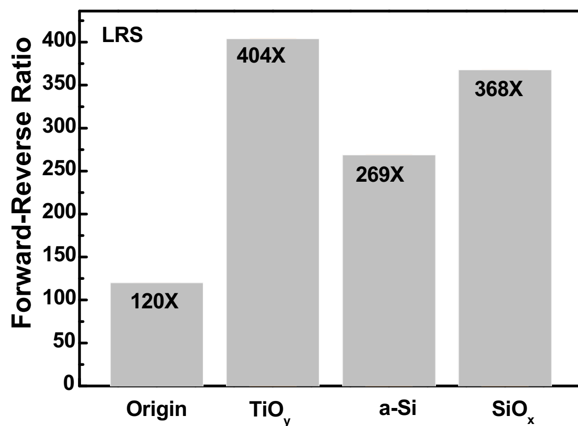
The switching uniformity is important for RRAM to replace commercial flash memory. Fig. 6(a) shows repeated cycling characteristics (100 cycles) under different THK conditions. The case of increased SiO_x THK exhibits poor endurance with a small memory window of 5 × after 100 cycles, which can be attributed to the interface trapping effect as discussed above (Fig. 5(b)). In contrast, the original structure maintains a consistent memory window of 27 × after 100 repeated cycles. The cycle-to-cycle current distributions are shown in Fig. 6(b) and (c). The coefficient of variation (CV) is defined as the ratio of standard deviation (σ) to mean value (μ), according to the equation of CV = σ/μ * 100%. We can observe a very uniform switching for LRS (12.7%) and HRS (11.7%) in original structure, but it cannot be reached in other control samples. Moreover, it is worth to note that the case of increased TiO_y THK with larger memory window of 33× presents the poor CV values for both LRS (18.9%) and HRS (16.3%), suggesting that is related to the increase of oxygen vacancy and interstitial Ti atom in thicker TiO_y case, which induces randomly distributed filaments and leads to poor distributions. Therefore, it is clear that the current distribution of this trilayer RRAM is much better than those of our previously reported 1R memories (GeO_x/SrTiO [11] and GeO_x/HfON [12] RRAMs) with lower switching powers due to the use of rectifying 1D1R-like structure, as shown in Fig. 7(a).



(a)

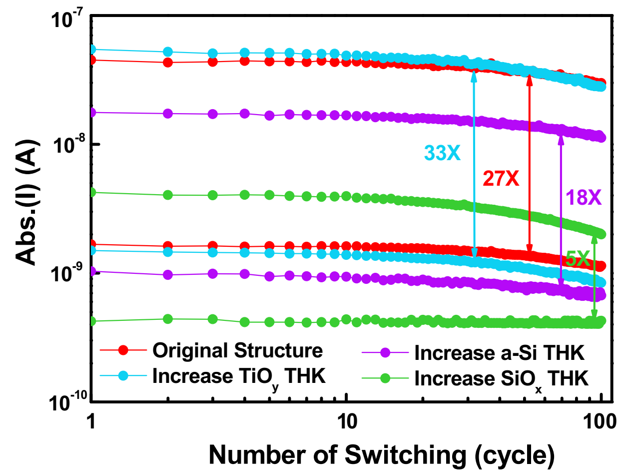


(b)

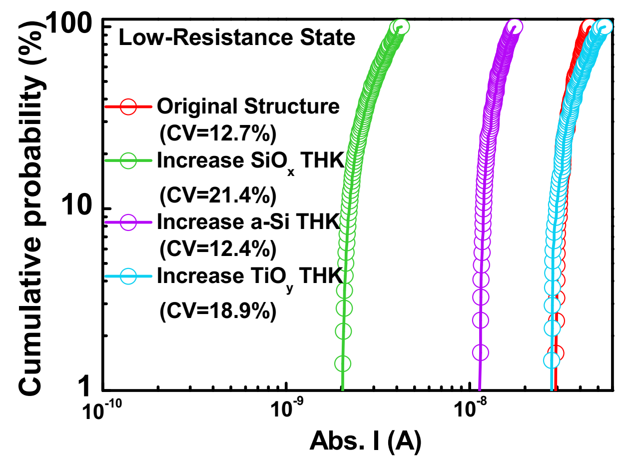


(c)

Fig. 5. Swept I–V curves of Ni/SiO_x/a-Si/TiO_y/TaN RRAM with different THK conditions for (a) set and (b) reset processes. (c) Repeated cycling characteristics of Ni/SiO_x/a-Si/TiO_y/TaN RRAM with different THK conditions.



(a)



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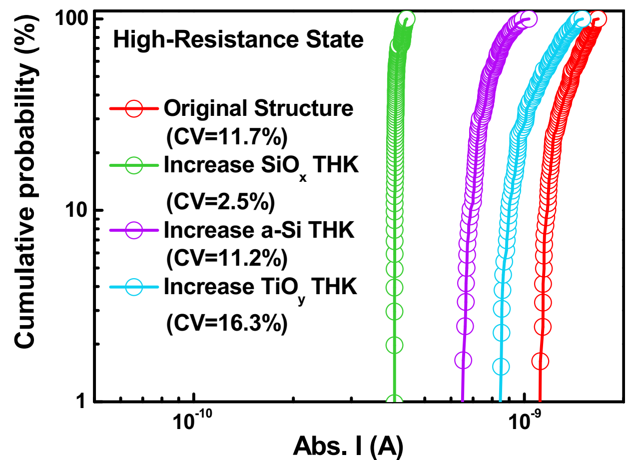
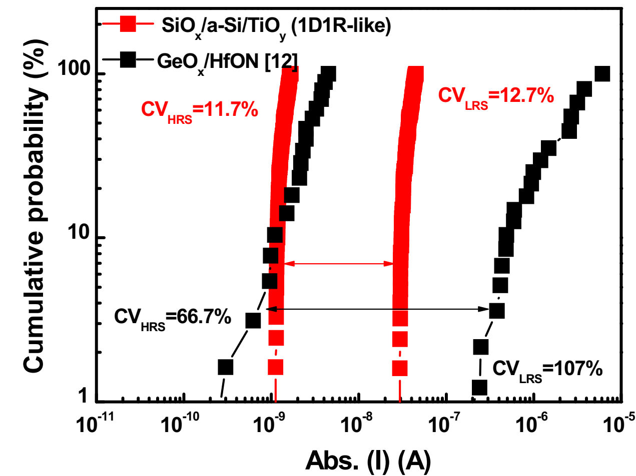


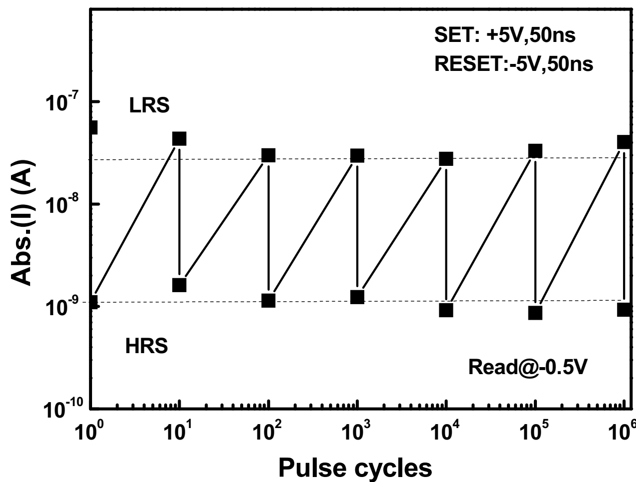
(c)

Fig. 6. (a) 50-ns-pulse cycling characteristics, (b) LRS and (c) HRS current distributions (cycle-to-cycle) of Ni/SiO_x/a-Si/TiO_y/TaN RRAM with different THK conditions.

Good endurance characteristics with uniform switching and fast speed are necessary for RRAM. As shown in Fig. 7(b), a $>20\times$ resistance window and a small LRS/HRS decay are measured for 10^6 cycles under 5 V set/−5 V reset voltages with 50 ns pulse. The fast switching speed is due to electron hopping conduction in LRS that has been demonstrated in our previous works [11–14]. Thus, the good endurance performance can be ascribed to a self-compliance switching current, pronounced LRS rectifying effect



(a)



(b)

Fig. 7. (a) Current distributions of Ni/SiO_x/a-Si/TiO_y/TaN RRAM and previous Ni/GeO_x/HfON/TaN RRAM devices and (b) endurance characteristic of Ni/SiO_x/a-Si/TiO_y/TaN RRAM device.

and very low switching energy of <10 pJ to stabilize electric filed stress across over dielectric stacks.

4. Conclusions

We reported a novel RRAM device using trilayer SiO_x/a-Si/TiO_y film stack. This RRAM device exhibits low operating voltage of 2 V, highly uniform current distribution of <13% variation, fast speed of 50-ns, low switching energy of <10 pJ, and good endurance. The good performances can be attributed to the incorporation of Ni/SiO_x/a-Si with diode-like function on TiO_y resistor, which lowers switching current through the combined effect of SiO_x tunnel barrier and hopping conduction in LRS. Moreover, the switching function of each layer was investigated. The results show that the thickness tuning of SiO_x to reduce interface trapping and TiO_y to modify interface electric field is an appropriate approach to achieve both good rectifying property and low switching power. Such low-power RRAM with interface-engineered dielectric stack and 1D1R-like structure design has the potential for a number of applications in the future, such as high-density 3D memory, programmable logic, and adaptive neuromorphic circuits.

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References

[1] K. Kim, G. Jeong, Tech. Dig. Int. Electron Devices Meet. 27 (2007).
[2] C.Y. Tsai, T.H. Lee, A. Chin, H. Wang, C.H. Cheng, F.S. Yeh, Tech. Dig. Int. Electron Devices Meet. 110 (2010).
[3] U. Russo, D. Ielmini, C. Cagli, A.L. Lacaita, S. Spiga, C. Wiemer, M. Perego, M. Fanciulli, Tech. Dig. Int. Electron Devices Meet. 775 (2007).
[4] C. Yoshida, K. Tsunoda, H. Noshiro, Y. Sugiyama, Appl. Phys. Lett. 91 (2007) 223510.
[5] N. Xu, L. Liu, X. Sun, X. Liu, D. Han, Y. Wang, R. Han, J. Kang, B. Yu, Appl. Phys. Lett. 92 (2008) 232112.
[6] B. Gao, B. Sun, H. Zhang, L. Liu, X. Liu, R. Han, J. Kang, B. Yu, IEEE Electron Device Lett. 30 (2009) 1326.
[7] X. Sun, B. Sun, L. Liu, N. Xu, X. Liu, R. Han, J. Kang, G. Xiong, T.P. Ma, IEEE Electron Device Lett. 30 (2009) 334.
[8] Q. Liu, S. Long, W. Wang, Q. Zuo, S. Zhang, J. Chen, M. Liu, IEEE Electron Device Lett. 30 (2009) 1335.
[9] W.Y. Chang, K.J. Cheng, J.M. Tsai, H.J. Chen, F. Chen, M.J. Tsai, T.B. Wu, Appl. Phys. Lett. 95 (2009) 042104.
[10] H.C. Tseng, T.C. Chang, J.J. Huang, P.C. Yang, Y.T. Chen, F.Y. Jian, S.M. Sze, M.J. Tsai, Appl. Phys. Lett. 99 (2011) 132104.
[11] C.H. Cheng, A. Chin, F.S. Yeh, Appl. Phys. Lett. 98 (2011) 052905.
[12] C.H. Cheng, A. Chin, F.S. Yeh, IEEE Electron Device Lett. 32 (2011) 366.
[13] C.H. Cheng, P.C. Chen, Y.H. Wu, F.S. Yeh, A. Chin, IEEE Electron Device Lett. 32 (2011) 1749.
[14] C.H. Cheng, A. Chin, F.S. Yeh, Adv. Mater. 23 (2011) 902.
[15] A. Chin, K. Lee, B.C. Lin, S. Horng, Appl. Phys. Lett. 69 (1996) 653.
[16] Q. Zuo, S. Long, Q. Liu, S. Zhang, Q. Wang, Y. Li, Y. Wang, M. Liu, Appl. Phys. Lett. 106 (2009) 073724.
[17] K.H. Kim, S.H. Jo, S. Gaba, W. Lu, Appl. Phys. Lett. 96 (2010) 053106.
[18] K.I. Chou, C.H. Cheng, Z.W. Zheng, M. Liu, A. Chin, IEEE Electron Device Lett. 34 (2013) 505.
[19] C.H. Cheng, S.H. Lin, K.Y. Jhou, W.J. Chen, C.P. Chou, F.S. Yeh, J. Hu, M. Huang, T. Arikado, S.P. McAlister, Albert Chin, IEEE Electron Device Lett. 8 (2008) 845.