A Silicidation-Induced Process Consideration for Forming Scale-Down Silicided Junction

H. C. Cheng, *Member, IEEE*, M. H. Juang, C. T. Lin, and L. M. Huang

***Abstract*—A process consideration for forming silicided shallow junctions, arising from silicidation process, has been discussed. The $CoSi_2$ shallow p^+n junctions formed by various schemes are characterized. The scheme that implants BF_2^+ ions into thin Co films on Si substrates and subsequent silicidation yields good junctions, but the problems about the dopant drive-in and knock-on of metal deeply degrade this scheme. In the regime that implants the dopant into Si and then Co deposition, however, a large perimeter leakage of 0.1 nA/cm is caused. Generation current, associated with a defect-enhanced diffusion of Co in Si during silicidation, dominates the leakage. A high-temperature pre-activation prior to Co deposition reduces the perimeter leakage to 0.038 nA/cm, but which deepens the junctions.**

I. Introduction

A SHALLOW junction with a self-aligned silicide (salicide) structure has been widely studied for improving the device performance in submicrometer CMOS circuits [1]–[5]. There is a trade-off in the metal thickness used during silicide formation on the ultra-shallow p^+n junction between the silicide sheet resistance and the junction leakage current [3], [6]. Conventionally, the fabrication method is the post junction salicide (PJS) regime [1] that the salicide process is executed after the junctions have been formed. In addition, several schemes have also been proposed to realize a silicided shallow junction [2], [5]. However, no comparison has been ever made with respect to the area and perimeter leakage for various processes. Furthermore, the induced leakage for silicidation on shallow junctions due to different processes remains to be clarified.

In this letter, $CoSi_2$ shallow p^+n junctions formed by various schemes have been characterized. The silicidation-induced leakage of the formed junctions is discussed. A necessary process consideration for forming silicided shallow junctions is proposed.

II. Experimental Procedure

(100) oriented, 0.55–1.1 Ω-cm, phosphorus-doped Si wafers were used. A 4500 Å-thick oxide layer was grown for patterning the active region of diodes as well as for the use of selective-etching. After the patterning, some of the specimens were deposited with 200 Å Co and 50 Å a-Si films sequentially in an electron-gun evaporation system. Then, they were BF_2^+-implanted at 50 keV to a dose of 1×10^{15} cm^{-2}. A two-step annealing was used for the salicide process. The 1st step sintering was by furnace annealing at 450 °C for 30 min in a N_2 ambient. The 2nd step annealing was at 600, 800, and 900 °C, respectively, with the same regime. The above samples were formed by implanting the dopant through the metal films (ITM). On the other hand, other blank Si samples were directly treated with implantation and then metallization. In this scheme, after the implantation, silicidation and activation (ISA) were completed simultaneously. This process is similar to the PJS scheme, but that a pre-activation is present for the PJS method. The junctions were formed with sizes of 100×100, 200×200, 500×500, 1000×1000 μm^2, respectively. The J_r value is the leakage current density at 5 V and at room temperature, with the diode size being 1000×1000 μm^2.

Manuscript received March 31, 1994; revised June 6, 1994. This research was supported in part by the Republic of China National Science Council under the Contract No. NSC 83-0404-E009-050.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, Republic of China.

IEEE Log Number 9404348.

III. Results and Discussion

In the PJS samples, the junctions were slightly degraded at high silicidation temperatures (ST) as the pre-activation temperature was not very high. Fig. 1 shows the dependencies of J_r on ST for the PJS samples pre-activated at 750, 900, and 1100 °C for 30 min, respectively. A J_r value of 1 nA/cm^2 can be achieved by the 1000 °C activation. For the 900 °C activation, good junctions were formed even for 600 °C silicidation. However, for the 750 °C activation, 800 °C silicidation was required to yield a low-leakage junction. In addition, junction degradation at ST of 900 °C was present for the 750 and 900 °C activation, whereas no high-temperature deterioration was found for the 1000 °C activation. Previously, anomalous dopant diffusion was reported to occur during annealing due to interstitial defects [7]. Moreover, DLTS analyses of the silicided junctions indicated a deep level of about 0.6 eV which is close to the trap level of Co in Si. Thereby, anomalous diffusion of Co in Si would also be induced during silicidation due to the implantation defects underneath the Co films. TEM analyses showed the presence of defects in the Si substrate after the pre-activation, and higher temperatures resulted in fewer residual defects. Hence, the samples activated at higher temperatures sustained less Co penetration at high ST, but formed deeper junctions. And thereby , thicker Co films would cause more serious Co penetration because of being closer to defect regions during silicidation. Previous studies also revealed this relation between metal thickness and junction leakage [1], [3].

On the other hand, ITM can result in good junctions at only 800 °C without any pre-activation. Scarce defects were

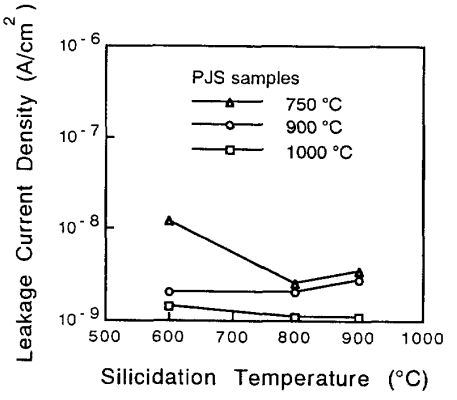

Fig. 1. Dependencies of J_r on silicidation temperature for the PJS samples pre-activated at 750, 900, and 100 °C, respectively.

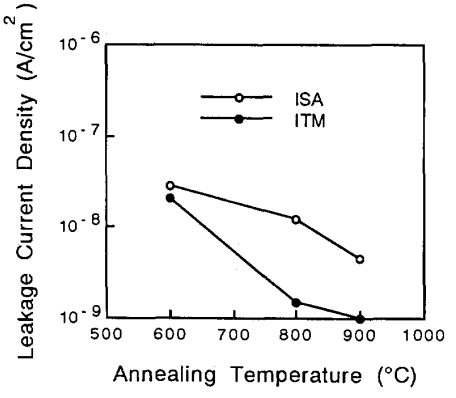

Fig. 2. Dependencies of J_r on silicidation temperature for ISA and ITM samples, respectively.

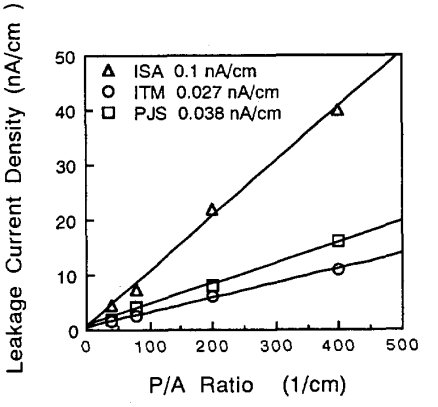

Fig. 3. Leakage current density as functions of P/A ratio for ISA (900 °C), ITM (800 °C), and PJS (pre-activation—900 °C, silicidation—800 °C) samples, respectively.

good for ITM to form good junctions at low ST. Fig. 2 shows the dependencies of J_r on ST for the ISA and ITM samples, respectively. A J_r value of 1 nA/cm^2 could be achieved by ITM, whereas ISA just led to 4.6 nA/cm^2. ISA did not exhibit worse junctions at higher ST, attributable to significantly better defect recovery and dopant activation. Since pre-activation could remove defects, less Co penetration was induced by silicidation. Thus, PJS can optimize a junction better than ISA. The sheet resistances for the formed silicides were about 2.1, 2.4, and 2.9 $\Omega/\square$ for PJS (pre-activated at 900 °C), ISA, and ITM samples silicided at 800 °C, correspondingly. The large resistance for ITM was due to a large amount of boron implanted into Co. In addition, the junction depths were about 0.22, 0.18, and 0.12 μm, correspondingly. Good shallow p^+n junctions can be achieved by the ITM scheme.

The leakage in the ISA samples was dominated by the generation current up to 70 °C, implying the considerable deep traps in junction regions. The Arrhenius plot (Log I_r/T^3 vs. $1/T$) for the junctions formed by ISA at 900 °C and ITM at 800 °C were compared. Generation current was largely caused by using ISA, but was very small for ITM. The leakage for ISA can be due to the deep trap level of Co arising from the defect-enhanced diffusion during silicidation. In addition, the PJS samples pre-activated at 900 °C and then silicided at 800 °C exhibited a current-temperature dependence close to the above ITM sample. Hence, the induced leakage for silicidation on shallow junctions due to various processes was mainly decided by the amount of defects prior to silicidation, and more defects caused more serious metal penetration during annealing. Though PJS could lead to good diodes, the high-temperature pre-activation largely deepened the junctions. On the other hand, ITM also yielded good p^+n junctions, but the dopant drive-in efficiency and uniformity [8] as well as the knock-on problem present in forming silicided shallow n^+p junctions were the large drawbacks to its usage. The knock-on metal atoms would also proceed a defect-enhanced diffusion in Si during annealing.

ISA resulted in acceptable J_r values without any pre-activation. However, the large generation current due to Co traps would cause a large leakage current density for small-area junctions, thus degrading the ULSI's applications of the regime. Fig. 3 shows the dependencies of leakage current density at -5V on P/A ratio for ISA (900 °C), ITM (800 °C), and PJS (activation—900 °C, ST—800 °C) samples, respectively, where P is the perimeter length and A is the junction area. The perimeter leakage was extracted from Fig. 3. The leakage values for ISA, ITM, and PJS were 0.1, 0.027, 0.038 nA/cm, correspondingly. For ISA, the leakage rapidly increased from 4.6 nA/cm^2 (for 1000 $\times$ 1000 μm^2) to 40 nA/cm^2 as the area was reduced to 100 $\times$ 100 μm^2. However, the changes were from 1.5 and 2 nA/cm^2 to 11.5 and 15.8 nA/cm^2 for ITM and PJS, correspondingly. As a result, anomalous leakage induced from silicidation can be lowered by reducing the defects prior to metallization.

IV. Conclusion

The ITM scheme yields good shallow p^+n junctions, but the problems about the dopant drive-in and the knock-on of metal in making n^+p junctions deeply degrade this scheme. For ISA, however, a large perimeter leakage of 0.1 nA/cm is found even for 900 °C annealing. Though the leakage is just 4.6 nA/cm^2

for a diode of 1000×1000 μm^2, the leakage becomes of 40 nA/cm^2 as the area is reduced to 100×100 μm^2. The large generation current for ISA is attributed to a defect-enhanced diffusion of Co in Si during silicidation. Thereby, thicker Co films would also cause larger leakage because of being closer to defect regions during silicidation. A high-temperature preactivation prior to Co deposition greatly reduces the defect-enhanced Co penetration and thus the perimeter leakage, but which largely deepens the junction. As a result, the process consideration arising from silicidation should be properly taken to optimize the scale-down silicided junctions.

REFERENCES

[1] C. Y. Lu, J. J. Sung, R. Liu, N. S. Tsai, R. Singh, S. J. Hillenius, and H. C. Kirsch, "Process limitation and device design tradeoffs of self-aligned $TiSi_2$ junction formation in submicrometer CMOS devices," *IEEE Trans. Electron Devices*, vol. 38, pp. 246–254, 1991.

[2] L. Rubin, D. Hoffman, D. Ma, and N. Herbots, "Shallow-junction diode formation by implantation of arsenic and boron through titanium silicide films and rapid thermal annealing," *IEEE Trans. Electron Devices*, vol. 37, pp. 183–190, 1990.

[3] J. Lin, S. Banerjee, J. Lee, and C. Teng, "Soft breakdown in titanium-silicided shallow source/drain junctions," *IEEE Electron Devices Lett.*, vol. 11, pp. 191–193, 1990.

[4] M. E. Alperin, T. C. Hollaway, R. A. Hakon, C. D. Gosmeyer, R. V. Karnaugh, and W. D. Parmantie, "Development of the self-aligned Ti silicide process for VLSI application," *IEEE J. Solid State Circuits*, vol. 20, p. 61, 1987.

[5] R. Liu, D. S. Williams, and W. T. Lynch, "A study of the leakage mechanism of silicided n^+p junctions," *J. Appl. Phys.*, vol. 63, pp. 1990–1999, 1988.

[6] J. Lebowitz, S. J. Hillenius, R. Liu, and W. T. Lynch, "Latchup suppression in silicided S/D/G CMOS by formation of modified Schottky p-channels," in *Proc. 1988 Symp. on VLSI Tech.*, pp. 53–54, 1988.

[7] T. O. Sedgwick, A. E. Michel, V. R. Deline, S. A. Cohen, and L. B. Lasky, "Transient boron diffusion in ion-implanted crystalline and amorphous silicon," *J. Appl. Phys.*, vol. 63, pp. 1452–1453, 1988.

[8] K. Maex, R. F. De Keersmaecker, G. Ghosh, L. Delaey, and V. Probst, "Degradation of doped Si regions contacted with transition-metal silicides due to metal-dopant compound formation," *J. Appl. Phys.*, vol. 66, pp. 5327–5334, 1989.