Decreasing-Size Distributed ESD Protection Scheme for Broad-Band RF Circuits

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***Abstract*—The capacitive load, from the large electrostatic discharge (ESD) protection device for high ESD robustness, has an adverse effect on the performance of broad-band RF circuits due to impedance mismatch and bandwidth degradation. The conventional distributed ESD protection scheme using equal four-stage ESD protection can achieve a better impedance match, but degrade the ESD performance. A new distributed ESD protection structure is proposed to achieve both good ESD robustness and RF performance. The proposed ESD protection circuit is constructed by arranging ESD protection stages with decreasing device size, called as decreasing-size distributed electrostatic discharge (DS-DESD) protection scheme, which is beneficial to the ESD level. The new proposed DS-DESD protection scheme with a total capacitance of 200 fF from the ESD diodes has been successfully verified in a 0.25-μm CMOS process to sustain a human-body-model ESD level of greater than 8 kV.**

***Index Terms*—Coplanar waveguide (CPW), distributed electrostatic discharge (DESD) protection, electrostatic discharge (ESD), resistive ladder, shallow-trench isolation (STI) diode.**

I. Introduction

ELECTROSTATIC DISCHARGE (ESD) is one of the most serious reliability issues to integrated circuit (IC) products. With the continuous scaling of process technology and rapid increase in circuit operating frequency, providing effective ESD protection to protect the ICs has become a challenge [1]. The main consideration on ESD protection design in wireless (RF) and high-speed (broad-band) applications is to achieve high ESD robustness, but not to affect the normal circuit performance. Therefore, the ESD protection devices in RF circuits are often designed with small device size to reduce its parasitic capacitance [2]–[4] and placed close to the I/O pins. However, with the continuous increase of circuit operation in broad-band frequencies, the traditional ESD protection design has met its limitation due to severe impedance mismatch caused by the parasitic capacitance of the ESD protection device. To improve the impedance match for broad-band RF circuits, a distributed ESD protection scheme, which employs line segments between ESD protection devices, had been reported [5]–[8], as shown in Fig. 1. Such a distributed ESD protection scheme has achieved either good ESD protection or good broad-band RF performance, but not both [5]–[8]. In [5], the ESD protection devices of gate-grounded NMOS devices were designed with series N-well resistors in the drains of NMOS, which was beneficial for uniform turn-on during ESD events to achieve a high ESD level. However, due to the large thermal noise contributed from the N-well resistors, it could not be suitable in the RF low-noise amplifier (LNA). In [6]–[8], a four-stage distributed ESD protection design by using ESD devices (p diodes and n diodes) of equal size was reported to achieve a good impedance match over a broad-band frequency range, but the ESD performance of such a design was never verified in the silicon chip.

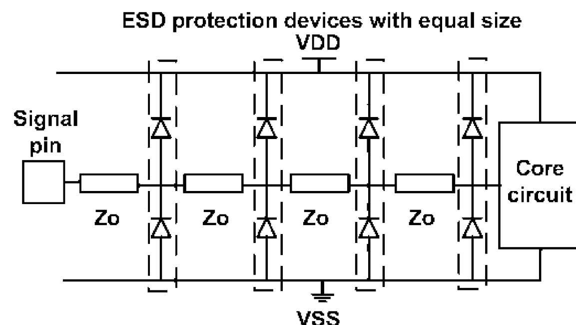

Fig. 1. Traditional distributed ESD protection design with equal-size diodes in four ESD stages [6]–[8].

In this paper, a new distributed ESD protection scheme with a decreasing-size ESD structure is proposed to achieve both excellent RF performance and ESD robustness. The new decreasing-size distributed electrostatic discharge (DS-DESD) protection scheme has been verified in a 0.25-μm CMOS process to sustain a human-body-model (HBM) ESD level of greater than 8 kV [9].

II. New Distributed ESD Protection Scheme

A. Concept of the New Distributed ESD Design

To sustain the desired ESD robustness, the traditional ESD protection devices should be drawn with large enough device size and placed near the signal pins, as shown in Fig. 2. However, for broad-band RF performance, the protection devices are preferred to be divided into numerous small units with the same device size and separated by transmission lines (T lines), coplanar waveguides (CPWs), or inductors, as that shown in Fig. 1. The dilemma can be overcome by the new proposed ESD protection scheme, as that illustrated in Fig. 3. The proposed ESD protection structure allocates the ESD protection devices with decreasing size from the signal pin to the core circuit, which is called as the DS-DESD protection scheme.

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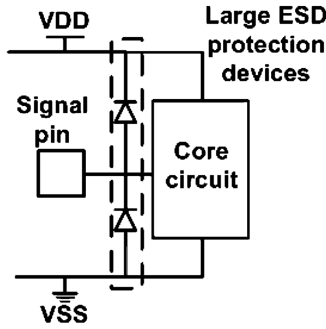


Fig. 2. Traditional ESD protection design with large ESD devices close to the signal pin to achieve a high ESD level.

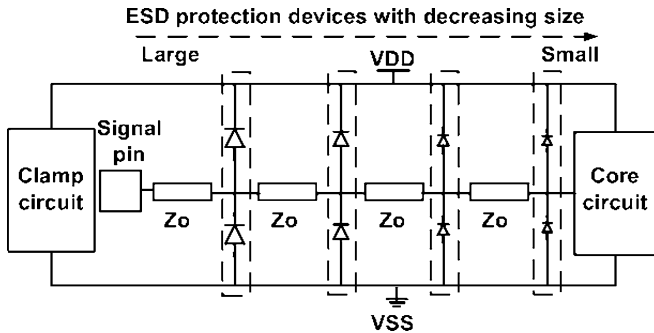


Fig. 3. New proposed DS-DESD protection scheme for broad-band RF circuits.

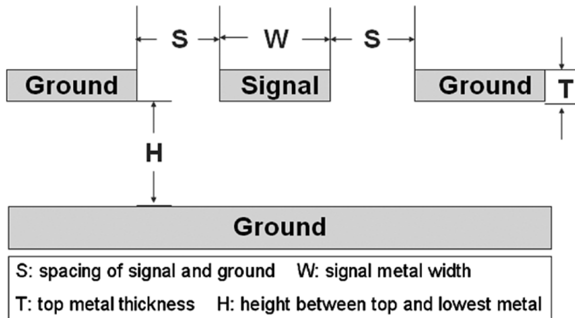


Fig. 4. Structure of CPWG realized in a CMOS process.

B. CPW With Ground Shield (CPWG)

In the distributed ESD protection design, the T lines have been often used to compensate the effect of the parasitic capacitances generated from the ESD protection devices. Here, the CPWG are used as T lines with the well-controlled characteristic impedance (Zo) and the low substrate loss [10], [11]. The structure of the CPWG is shown in Fig. 4. The thick top-layer metal is used as the signal line of the CPWG, and metal 1 (the lowest metal layer) is employed as the ground shield. Due to the limitation of the given 0.25-μm CMOS process, the thickness of the top-layer metal is only 1.5 μm and the height between the top-layer metal and metal 1 is 5.71 μm. The permittivity of the silicon dioxide is 4.1 and that of the substrate is approximately 11.7. The required spacing between the signal line and coplanar ground, as well as the width of the top-layer metal (signal line) to achieve various characteristic impedances, have been calculated and listed in Table I. Narrow widths of the signal line with large spacings yield high characteristic impedances. In this study, narrow signal lines were preferred to make it obvious that the difference of the ESD protection levels between the traditional equal-size distributed electrostatic discharge (ES-DESD) protection scheme and the new proposed DS-DESD protection scheme. However, due to the narrower signal line, the series resistor of the CPWG increased, which is adverse in RF power transfer and the ESD current conduction. The CPWG with Zo of 70 Ω was finally chosen to compromise this conflict.

TABLE I
PARAMETERS TO FORM THE CHARACTERISTIC IMPEDANCES OF THE CPWG IN A 0.25-μm CMOS PROCESS

Zo (Ω)	Width (μm)	Spacing (μm)	Height (μm)	Thickness (μm)
70	5.5	7.4	5.71	1.5
80	4.1	8.8	5.71	1.5
90	2.9	8.2	5.71	1.5
100	2.1	8.4	5.71	1.5

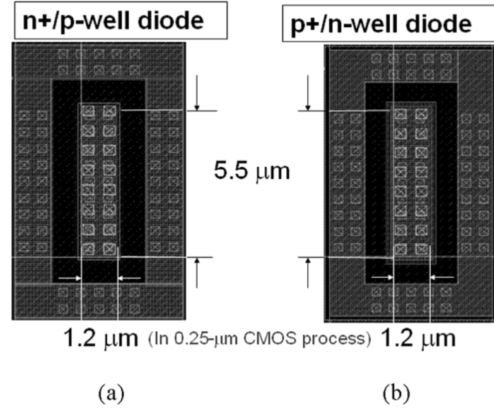


Fig. 5. Layout top views of: (a) the n+/p-well diode and (b) the p+/n-well diode, realized in a 0.25-μm CMOS process. One pair of these diodes contributes a parasitic capacitance of 25 fF.

C. Diode Design

The ESD protection devices in RF circuit should be chosen without contributing large resistances and capacitances for the noise and match concerns. Q factors are often used to evaluate the qualities of the ESD protection devices. The definition of a Q factor for a series *RC* network has been written as

$$Q = \frac{1}{\omega RC}. \quad (1)$$

As seen in (1), with the reduction of the series resistance and capacitance, the Q factor of the ESD protection device increases. The shallow-trench-isolation (STI) diodes have been often used as ESD protection elements due to their high-Q factors [12]. In this study, one pair of n+/p-well and p+/n-well STI diodes with layout dimension [(width (W)/length (L)] of 1.2 μm/5.5 μm contributes the parasitic capacitance of approximately 25 fF in the given 0.25-μm CMOS process. The layout top views of these diodes are shown in Fig. 5. If four pairs of such diodes are connected in parallel, they will totally contribute a capacitance of 100 fF.

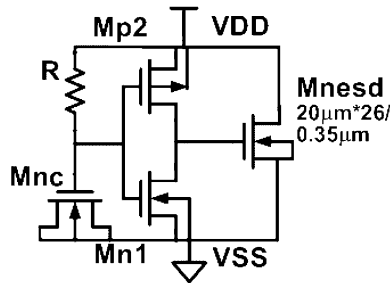


Fig. 6. Turn-on efficient VDD-to-VSS ESD clamp circuit drawn with ESD protection NMOS $Mnesd$ of large device size.

TABLE II
DEVICE SIZES USED IN THE VDD-TO-VSS ESD CLAMP CIRCUIT

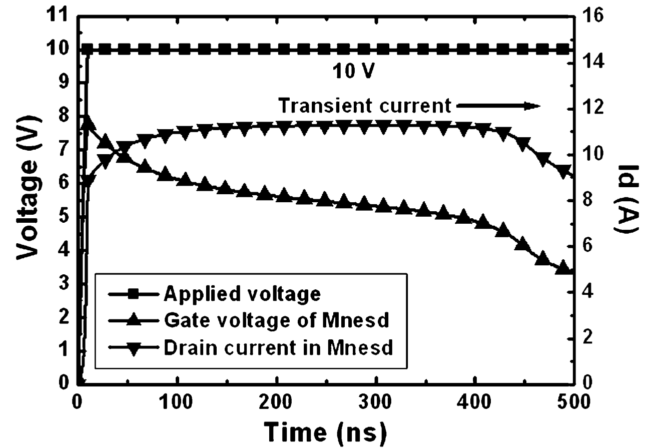
	Width (μm)	Length (μm)	Unit width (μm)	Finger number
Mnesd	520	0.35	20	26
Mn1	40	0.35	20	2
Mp2	120	0.35	20	6
Mnc	45	13	15	3
R (n-well)	3	360		

D. VDD-to-VSS ESD Clamp Circuit

In RF ESD protection design, the power-rail ESD clamp circuit is valuable to help conducting ESD currents through the forward-biased paths [4]. The turn-on efficient VDD-to-VSS ESD clamp circuit, beneficial for fast turn-on speed during ESD events, is shown in Fig. 6 [13], [14]. The *RC* time delay was chosen approximately 0.1 μs to turn on the ESD NMOS ($Mnesd$) during ESD events, and to keep it off under the normal power-on condition. *R* and *C* were realized by the N-well resistor and MOS capacitor, respectively. The inverter can trigger the gate voltage of $Mnesd$ to a high level to help $Mnesd$ being uniformly turned on while facing the ESD pulse. Hence, the conductance of the PMOS in the inverter needs to be large enough to turn on the $Mnesd$ quickly during the ESD event. The main ESD protection device ($Mnesd$) must be drawn carefully. First, the silicided diffusion is forbidden for ESD protection consideration. Second, the channel width must be drawn large enough to discharge ESD current. Third, the finger width and channel length have to be well selected according to the suggested ESD design rules in the given CMOS process. The device sizes used in this VDD-to-VSS ESD clamp circuit are listed in Table II. The simulated voltage waveforms on the gate of $Mnesd$ and the drain current of $Mnesd$ under the ESD-stress condition and the normal power-on condition are shown in Fig. 7(a) and (b), respectively. With suitable circuit design, the VDD-to-VSS ESD clamp circuit is only triggered on during the ESD-stress conditions.

E. RF Performance Analysis With Smith Chart

S-parameter matrix has been widely used in the RF system to show the performance of the network. Starting with a standard 50-Ω system, which is commonly found in RF systems, the equivalent RF circuit models of these two different ESD protection schemes are shown in Fig. 8(a) and (b). Fig. 8(a) shows the equivalent RF circuit model of the traditional ES-DESD protection scheme [6]–[8]. The equivalent RF circuit model of the new proposed DS-DESD protection scheme is shown in Fig. 8(b).



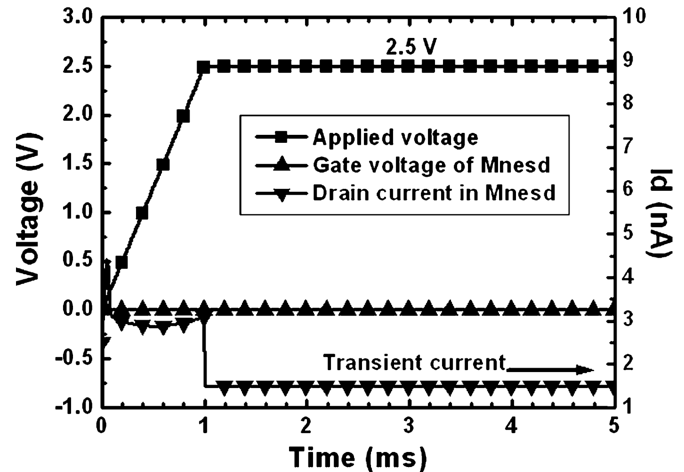


Fig. 7. Simulated voltage waveforms and the transient current of the VDD-to-VSS ESD clamp circuit under: (a) the ESD-stress condition and (b) the normal power-on condition.

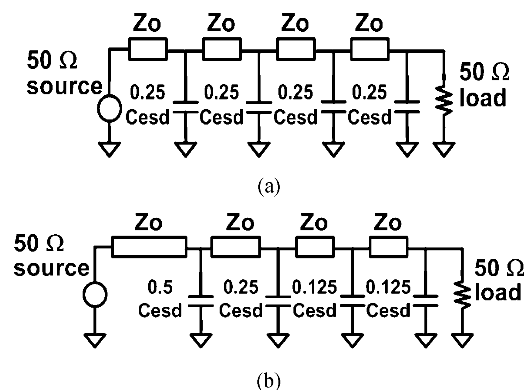


Fig. 8. Equivalent RF circuit models of: (a) the traditional ES-DESD protection scheme and (b) the DS-DESD protection scheme. The total parasitic capacitance (200 fF) of the ESD protection devices (diodes) is modeled as $Cesd$ to the ac ground.

A signal source with 50-Ω impedance drives the input node of the ESD protection schemes, and a 50-Ω output load is connected to the output node of ESD protection schemes. In each ESD protection scheme, the ESD protection diodes are modeled as capacitances $Cesd$. It had been demonstrated that the CPWG can provide excellent RF performance for operating frequency

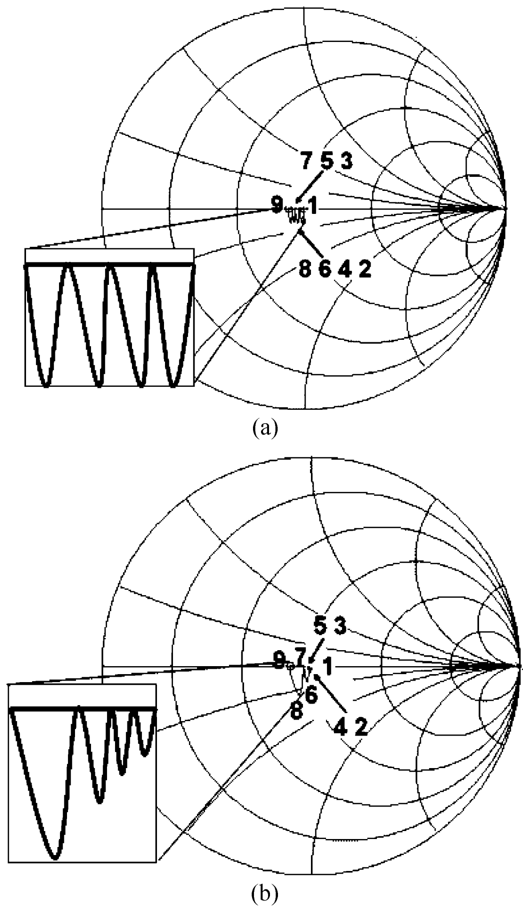


Fig. 9. Matching procedures of: (a) the traditional ES-DESD protection scheme and (b) the DS-DESD protection scheme, expressed on the Smith chart.

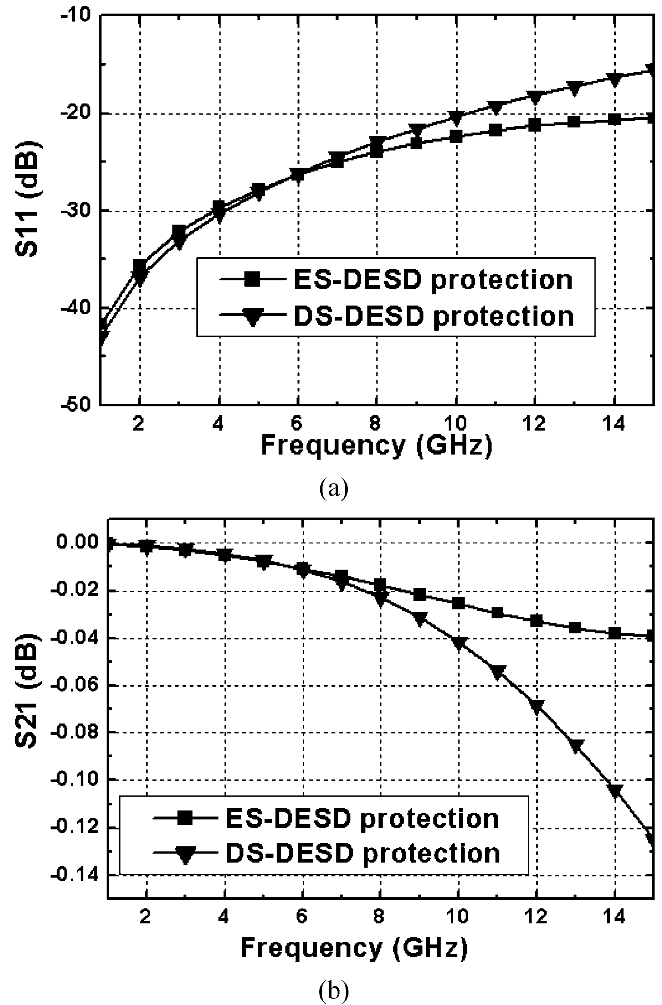


Fig. 10. Simulation results on the RF performance of: (a) $S11$– and (b) $S21$-parameters between the ES-DESD and the DS-DESD protection schemes.

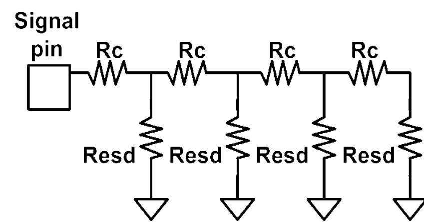


Fig. 11. Resistive ladder of the traditional ES-DESD match.

over 10 GHz [10], [11], so they are also used in the ESD protection schemes for broad-band RF circuits. STI diodes were employed as the ESD protection devices for their high-Q factors [12].

Initially, the total ESD capacitance $Cesd$ is assumed to be 200 fF, a value sufficient to achieve the 2-kV HBM ESD protection level [3]. The characteristic impedance Zo of the CPWG is employed as 70 Ω in this study. S-parameter simulations over the frequency range of 1$\sim$15 GHz are performed on these two ESD protection schemes by using the microwave circuit simulator ADS to find the reflection parameter $S11$ and the transmission parameter $S21$. With the neglect on the loss in the CPWG, $S21$ is the result of $(1-S11)$. Thus, $S11$, related to the impedance match, is the main consideration to compare these two ESD protection schemes shown in Fig. 8(a) and (b). The matching principles of the ES-DESD and DS-DESD ESD protection schemes are expressed in the Smith chart, as those shown in Fig. 9(a) and (b), respectively. The operating frequency is set to 10 GHz in Fig. 9. The centered point of the Smith chart is normalized to 50 Ω. Each CPWG length has been optimized to reach the best match in each ESD protection scheme. The serial number labeled on each point indicates the matching procedure contributed by these components from the core circuit with a 50-Ω output load to the input node of ESD protection scheme.

The matching locus on $S11$ of the ES-DESD ESD protection scheme is shown in Fig. 9(a), and that of the DS-DESD ESD protection scheme is shown in Fig. 9(b). These two ESD protection schemes have good matching results back to the real line of the Smith chart. However, the final matching points are not the original center point in the Smith chart. The simulation results on the RF performance of $S11$- and $S21$-parameters between the ES-DESD and DS-DESD protection schemes are shown in Fig. 10(a) and (b), respectively. Comparing the curves of $S11$-parameters in Fig. 10(a), the RF performances of ES-DESD and DS-DESD ESD protection schemes have a little difference when the frequency increases up to 10 GHz. Hence, the $S21$-parameters of these two ESD protection schemes in Fig. 10(b) also have a little difference when the frequency increases up to 10 GHz. Due to the lack of detailed RF parameters in the given CMOS process, the loss in the

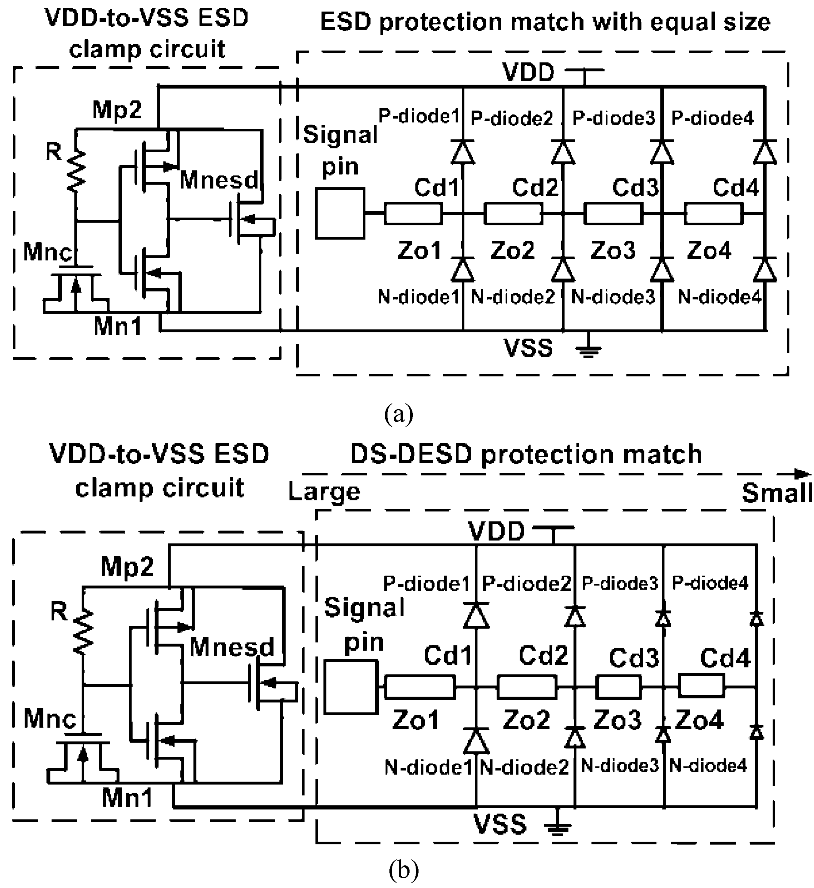


Fig. 12. (a) ES-DESD protection scheme and (b) the DS-DESD protection scheme with the VDD-to-VSS ESD clamp circuit realized in 0.25-μm CMOS technology.

narrow signal line and the loss in the substrate are not included into the simulation here. Those nonideal effects will cause a different result on $S21$ between the simulation and experimental measurement. However, according to the simulation results in Fig. 10, the DS-DESD protection scheme indeed achieves a comparable broad-band RF performance as that of the ES-DESD protection scheme over a wide frequency bandwidth.

F. RF ESD Protection Design Considerations

For an input pin, there are four modes of pin combinations during ESD stress, which are: 1) positive-to-VSS (PS mode); 2) negative-to-VSS (NS mode); 3) positive-to-VDD (PD mode); and 4) negative-to-VDD (ND mode) ESD stresses [15]. The ESD level of an input pin is defined as the lowest ESD level among the four modes of ESD stresses. Therefore, the on-chip ESD protection design should provide effective discharge paths for the four-mode ESD stresses. The turn-on efficient VDD-to-VSS ESD clamp circuit, with the *RC* inverter NMOS ESD protection circuit, is applied to ensure the ESD protection devices operating in the forward-biased condition under the four ESD-stress modes on the I/O pad [13], [14].

To compare and analyze the ESD performance, the resistive ladder model of the ES-DESD protection scheme is employed, as shown in Fig. 11. According to [5], the large values of the series resistance of CPWG (Rc) and the resistance of ESD device ($Resd$) degraded ESD robustness when the ESD-generated power across them. Therefore, in order to enhance ESD protection level, the $Resd$ and Rc should be minimized. The new proposed DS-DESD protection scheme by enlarging the size of ESD protection devices at the first ESD stage can reduce the $Resd$ of the first stage, where is usually the most possible location to be damaged. With a relatively large device size at the first ESD stage, it can discharge ESD current more quickly at the first ESD protection stage without along the CPWG of the next stages with the lengths of several hundreds micrometers. Thus, the proposed DS-DESD protection scheme will have better ESD robustness, as compared to that of ES-DESD protection scheme.

III. Chip Implementation

To investigate both the RF performance and ESD robustness of the proposed DS-DESD scheme, the advanced process would be preferred. However, limited to the resource of advanced process, which is often quite expensive, the experimental test chip of this study has been designed and fabricated in a 0.25-μm CMOS technology with five metal layers. The CPWG employed the top metal as the signal line and metal 1 as the grounded shield, hence, the thickness of the signal line and the height between the signal line and metal 1 were fixed. The ways to adjust the characteristic impedance (Zo) of the CPWG are to change the width of the signal line and the spacing between the signal line and coplanar ground. Based on the fixed dielectric constant, the required length of the CPWG to compensate the

TABLE III
COMPONENT PARAMETERS OF ESD PROTECTION ELEMENTS USED IN THE ES-DESD AND DS-DESD PROTECTION SCHEMES

Match type	ES-DESD	DS-DESD
Cd1 (fF)	50	100
Cd2 (fF)	50	50
Cd3 (fF)	50	25
Cd4 (fF)	50	25
Zo1 (Ω)	70 (L=381 μm)	70 (L=782 μm)
Zo2 (Ω)	70 (L=424 μm)	80 (L=395 μm)
Zo3 (Ω)	70 (L=482 μm)	90 (L=170 μm)
Zo4 (Ω)	70 (L=566 μm)	100 (L=145 μm)

parasitic capacitance can be determined. The impedance of 70 Ω with the signal-line width of 5.5 μm and spacing of 7.4 μm were chosen to make the resistive-ladder effect more obvious. The STI p- and n-diodes were chosen to shunt the ESD paths to VDD or VSS. Each pair of p- and n-diodes with a dimension of 5.5 × 1.2 μm^2 contributes a parasitic capacitance of approximately 25 fF. The ES-DESD and DS-DESD protection circuits with the VDD-to-VSS ESD clamp circuits have been implemented and shown in Fig. 12(a) and (b), respectively, with a total parasitic capacitance of 200 fF from the ESD diodes. These two ESD protection schemes without the VDD-to-VSS ESD clamp circuits are also fabricated in the same testchip as a comparative reference. The component parameters of the ESD protection elements and the length of the CPWG used to realize these two ESD protection schemes in a 0.25-μm CMOS process are listed in Table III.

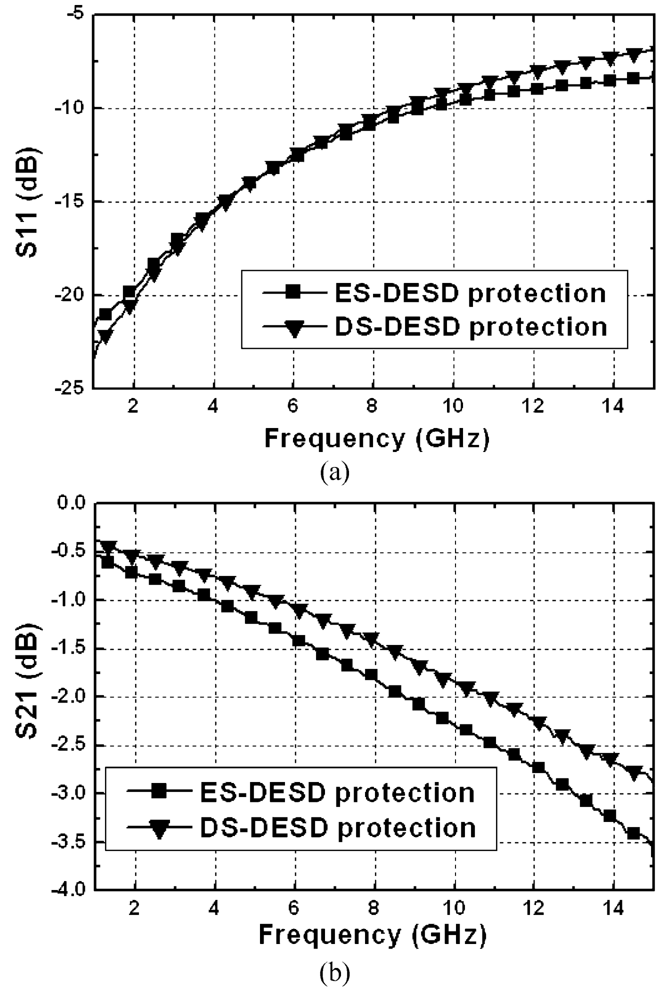


Fig. 13. Measured results of RF performance on: (a) $S11$- and (b) $S21$-parameters of the fabricated ES-DESD and DS-DESD protection schemes.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Measured S-Parameters

The S-parameters of these two ESD protection schemes have been measured on-wafer with two-port ground–signal–ground (G–S–G) probes from 1 to 15 GHz. The 20-GHz S-parameter measurement system (HP85122A) is used to characterize the circuit behavior. The voltage supply of VDD (VSS) is 2.5 V (0 V), and the input dc bias is 1.0 V. The source and load resistances to the fabricated ESD protection circuits are kept at 50 Ω. The parasitic effects from the input and output pads have been deembedded through the reference open pads to obtain the pure S-parameters of the ESD protection circuits. The measured $S11$- and $S21$-parameters versus frequency are shown in Fig. 13(a) and (b), respectively. As seen in Fig. 13(a), the $S11$-parameters between the ES-DESD and DS-DESD ESD protection schemes are different from the simulated ones due to the large power loss along the signal lines and the lossy substrate in the 0.25-μm CMOS process. Nevertheless, the $S11$-parameters of these two ESD protection schemes still display the same trend as that in the simulated ones. The $S11$ of ES-DESD scheme is a little smaller than that of DS-DESD when the frequency up to 10 GHz.

The $S21$-parameters of the ES-DESD and DS-DESD protection circuits are the mixture of the power loss and transmission along the ESD stages with CPWGs of different lengths. Due to the large loss from the narrow signal line and the lossy substrate in the given 0.25-μm CMOS process, the performance of $S21$ is almost reverse to the length of the signal line (CPWG). With a shorter total length of CPWG in the DS-DESD protection circuit, which is realized by top metal 5 in a 0.25-μm CMOS technology, the $S21$ of the DS-DESD protection scheme is better than that of the ES-DESD protection scheme, as shown in Fig. 13(b). This is due to the loss of longer CPWG in the ES-DESD scheme (the DS-DESD scheme has a shorter length of total CPWG). This situation can be further improved by employing wider signal lines and the advanced process to reduce the power loss. When the measured $S11$ can approach the simulated $S11$ under the condition employing ideal signal lines, the measured $S21$ will be positively proportional to the matching condition. However, from the experimental results in this study, the new proposed DS-DESD protection scheme has indeed achieved a good broad-band RF performance as that of the traditional ES-DESD protection scheme.

B. ESD Test Results

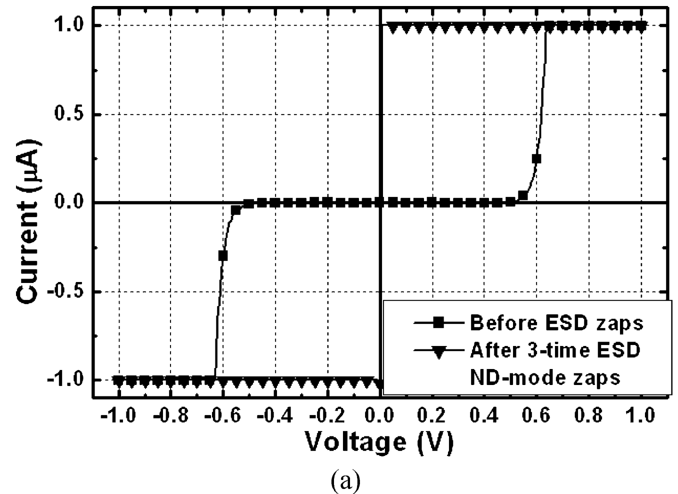
The HBM ESD test results of these two ESD protection schemes with or without the VDD-to-VSS ESD clamp

TABLE IV
HBM ESD LEVELS OF THE ES-DESD AND DS-DESD ESD PROTECTION SCHEMES WITH OR WITHOUT THE VDD-TO-VSS ESD CLAMP CIRCUITS

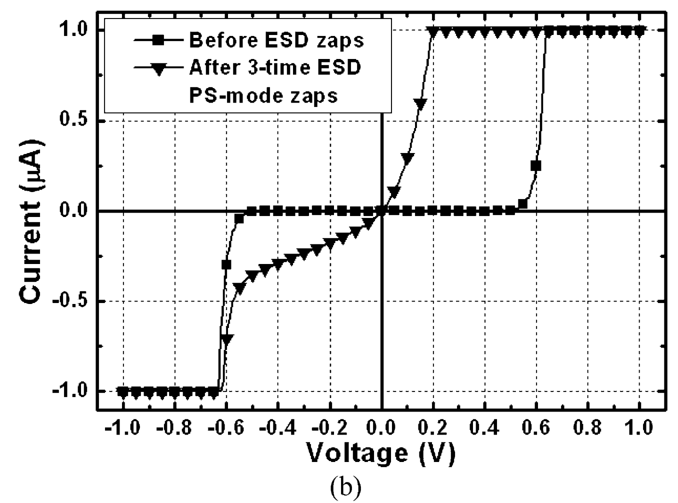
VDD-to-VSS ESD clamp circuit	Without	Without	With	With
Match type	ES-DESD	DS-DESD	ES-DESD	DS-DESD
ND-mode (kV)	0.55	0.6	5.5	> 8.0
PS-mode (kV)	0.75	0.75	5.5	> 8.0

circuits are summarized in Table IV at the failure criterion of 30% *I–V* curve shifting under 1-μA current bias. The negative-to-VDD (ND) and positive-to-VSS (PS) mode ESD stresses are the two worse ESD conditions for the ESD stresses on the I/O pin with diodes as ESD protection devices [14]. The $Mnesd$ in VDD-to-VSS ESD clamp circuit for both ES-DESD and DS-DESD ESD protection schemes is realized with device dimension of $\mathrm{W/L} = 520\ \mu\mathrm{m}/0.35\ \mu\mathrm{m}$ in the test chip. The traditional ES-DESD protection scheme can sustain the HBM ESD level of 5.5 kV, but that of the DS-ESD protection scheme can be improved up to >8 kV with the help of the VDD-to-VSS ESD clamp circuit. Without the VDD-to-VSS ESD clamp circuit, both of these two ESD protection schemes have a very low ESD level.

This has also verified the effectiveness of the active VDD-to-VSS ESD clamp circuit to improve ESD robustness of RF circuits, which are protected by the diodes with small device sizes to reduce the parasitic effect on RF signal. The typical failed *I–V* curve shifts on the ES-DESD protection circuit before and after HBM ESD stresses in the ND-mode and PS-mode ESD test are shown in Fig. 14(a) and (b), respectively. From the well-known experience of ESD failure analysis, the curve shifting in Fig. 14 can be judged from the junction leakage on the ESD protection diodes.



(a)



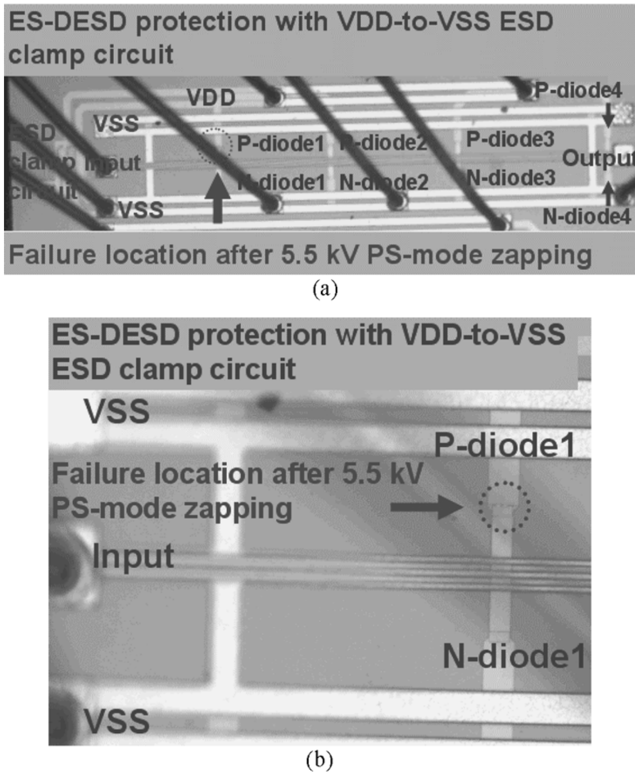
(b)

Fig. 14. *I–V* curves of the input diodes before and after: (a) the negative-to-VDD (ND-mode) and (b) the positive-to-VSS (PS-mode) ESD stresses. These *I–V* curves are monitored with both VDD and VSS relatively grounded.

In order to make sure the ESD protection results consistent with the principle of the resistive ladder model in Fig. 11, the failed circuits after ESD stresses have been de-processed to find the failure location. The EMMI (photon emission microscope) photographs on the ES-DESD protection circuit with a VDD-to-VSS ESD clamp circuit after 5.5-kV PS-mode ESD stress are shown in Fig. 15(a) (the whole view) and Fig. 15(b) (zoomed-in location on the damaged site).

The EMMI photographs have confirmed that the ESD damage is located on the p-diode junction of the first ESD stage with a shining area after the PS-mode ESD stress. The evidence in Fig. 15 has proven that the concept of the resistive-ladder model is correct. The first ESD stage is the weakest location of ESD protection along the ES-DESD ESD protection scheme. Hence, the new proposed DS-DESD ESD protection scheme with the relatively enlarged first ESD stage (but keeping the same total capacitance of ESD diodes) can actually achieve a better ESD robustness than that of ES-DESD ESD protection scheme.

To further reduce the loss of the RF signal along the longer CPWG in such ES-DESD and DS-DESD schemes, the CPWG with higher characteristic impedance will be a better selection to achieve better RF performance. The required spacing between the signal line and coplanar ground, as well as the width of the top-layer metal (signal line) to achieve various characteristic impedances have been calculated and listed in Table I. Narrow widths of the signal line with large spacings yield high characteristic impedances. However, the CPWG connected from the pad to ESD diodes drawn with a too-narrow linewidth could be burned out to open circuit by the large ESD transient current in the order of several amperes. A CPWG of 50 Ω (or even with smaller impedance) has a wider linewidth for better ESD current discharging. However, the required line length of the CPWG with smaller characteristic impedance to do RF matching for ESD diodes will become much longer, which will, in turn, cause more power loss for the RF signal through the much longer CPWG. Optimization on the CPWG between the linewidth for ESD current discharging and the characteristic impedance for RF matching (or loss) in different CMOS processes will be a design tradeoff. Thus, in this study, with real chip implementation, the characteristic impedance (Zo) of the CPWG is employed as 70 Ω to meet both considerations of RF performance and the linewidth for ESD current discharging.



(a)

(b)

Fig. 15. EMMI photographs to show the location of ESD damages in the ES-DESD protection circuit with the VDD-to-VSS ESD clamp circuit after the PS-mode stress. (a) The whole view of the ES-DESD circuit. (b) The zoomed-in view of the damaged location on the p-diode at the first ESD stage.

V. Conclusion

A new DS-DESD protection circuit with excellent broad-band RF performance and great ESD level has been proposed and verified in a 0.25-μm CMOS process. Compared to the traditional ES-DESD protection scheme, the new proposed DS-DESD protection scheme has presented a comparable good RF match and much better ESD robustness. With the help of an active VDD-to-VSS ESD clamp circuit, the device sizes of ESD protection diodes in the RF input pin can be further reduced to decrease the parasitic capacitance from ESD devices for achieving better RF circuit performance. This new broad-band ESD protection scheme is more useful for ESD design in broad-band RF ICs.

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