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Reduction of current mismatching in the switches-in-source CMOS charge pump

Miin-Shyue Shiau [a], Heng-Shou Hsu [a], Ching-Hwa Cheng [a,*], Hsiu-Hua Weng [b], Hong-Chong Wu [c], Don-Gey Liu [a]

[a] Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan, ROC
[b] Institute of Electronic Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, ROC
[c] Graduate Institute of Information Engineering, Feng Chia University, Taichung 40724, Taiwan, ROC

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ABSTRACT

In this paper, the charge pump (CP) based on a switches-in-source architecture is to be improved by gain-boosting amplifiers for phase-locked loops (PLLs). In our design, two differential amplifiers were employed in this CP to reduce the effect of the channel length modulation in MOS transistors. As a result, the up and down currents will be rather independent of the output voltage transformed by the capacitive low pass filter (LPF). This circuit was implemented using TSMC 0.18-μm CMOS technology and was investigated at a power supply of 1.8 V. The measured mismatch was less than 1% for the output voltage ranging from 0.4 to 1.4 V. This result is lower than that of the dynamic current-matching CP with feedback tuning on the same architecture. A comparison will be presented and discussed.

1. Introduction

In modern computer and communication systems, PLLs play an important role in frequency synthesis, synchronization or clock/data recovery. As the fabrication technique advances, a PLL with lower frequency jitters or reference spurs is pursued [1–3]. To achieve the desired performance, every component in a PLL needs to be improved individually. Among these components, the first issue may be the phase detection technique which is directly related to the problems of jitters and spurs.

For digital clock synthesis, a CP is usually accompanied by a capacitive LPF to generate control voltage for the voltage-controlled oscillator (VCO) at a later stage. Fig. 1 depicts the schematic diagram of a PLL with a PFD as its phase detector for frequency synthesis. According to the timing difference between the reference frequency, f_{ref}, and the feedback frequency, f_{fb}, the PFD generates two control signals, *up* and *dn*, to make the CP generate a pumping current, I_p. This current is transformed by the LPF as a voltage, V_{cp}, which then controls the VCO to generate a desired frequency, f_{out}. After division by an integer or fractional number, N, the feedback frequency f_{fb} is required to immediately follow f_{ref} [4].

The role of the PFD is to detect the differences in the phases or frequencies of the two input signals. After the system is locked, f_{fb} and f_{ref} are supposed to be the same with a fixed phase difference, $\Delta\Phi$, between them. Usually, the phase difference is designed to be zero to stop changing V_{CP} and therefore f_{out}. Fig. 2 shows a typical PFD–CP circuit with a LPF capacitor to generate V_{CP}.

For conventional designs, the transfer characteristic between $\Delta\Phi$ and the pumping current, I_p, can be shown as curve B in Fig. 2(b). There are some design issues for the PFD–CP by CMOS technologies.

First as indicated in Fig. 2(b), there is usually a dead zone for $\Delta\Phi$ close to zero where I_p is less sensitive to $\Delta\Phi$. This problem is mainly attributed to the logic operation of the PFD. Due to the inconsistent propagation delays and non-ideal switching in the Flip-Flops and the logic AND gate, the PFD cannot react linearly when f_{fb} approaches the f_{ref} phase. A proper delay applied in the reset control of the Flip-Flops in the PFD will relieve this problem [5].

The other problems are caused by the switching operations in the CP. These problems are charge injection, charge sharing, and clock feed-through, all of which are commonly encountered in the design of logic integrated circuits. With suitable switching configurations at the output stage in the CP, most interference would be largely reduced [6]. Up to now, the Switching-in-Source (SS) configuration has typically been adopted in the design of a CP because this configuration is less affected by switching transients.

Besides the switching problems, the pull-up and push-down currents, I_{up} and I_{dn}, are driven by a PMOS and an NMOS separately, so it is not easy to adjust I_{up} to strictly equal I_{dn} all the time. As a result, there will be injected charges into the LPF capacitor even when $\Delta\Phi=0$. Such non-matched currents make the obtained output frequency in the PLL vary around the target frequency and cannot converge precisely to the target, which deteriorates the reference spur.

* Corresponding author. Tel.: +886 4 24517250x4901; fax: +886 4 24510405.
E-mail addresses: msshiau@fcu.edu.tw (M.-S. Shiau), hshsu@fcu.edu.tw (H.-S. Hsu), chengch@fcu.edu.tw (C.-H. Cheng), hhweng0509@gmail.com (H.-H. Weng), hwu@fcu.edu.tw (H.-C. Wu), dgliu@fcu.edu.tw (D.-G. Liu).

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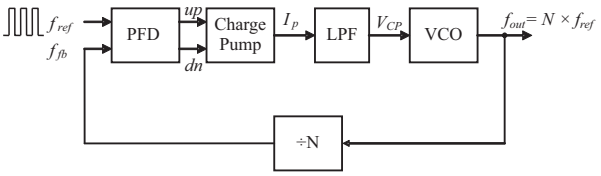

Fig. 1. A typical PLL as a frequency synthesizer.

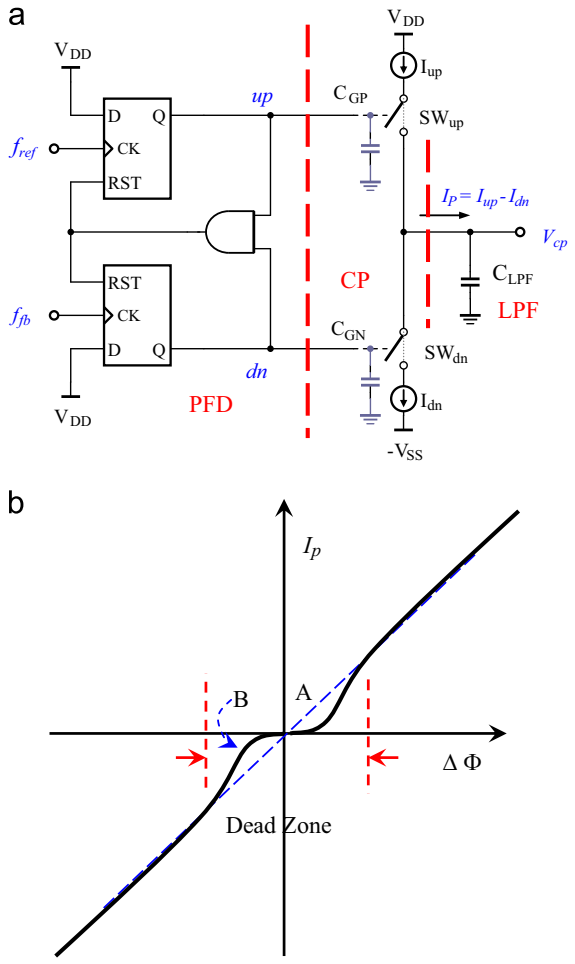

Fig. 2. (a) A typical PFD–CP circuit and (b) the possible transfer characteristics: curve A is the ideal transfer characteristic and curve B is the real characteristic in most cases.

Several methods with some area and power penalties have been proposed to minimize the current mismatch [7–10]. Huh et al. proposed a digital compensation scheme to reduce the mismatched up and down currents [7,8]. In their circuit, a replica CP was imposed in parallel to calibrate the injected charges in a capacitor. The resulting voltage on the capacitor is used by a logic controller to fine tune the down current of the main CP. With this scheme, the mismatch can be reduced to be within 1%. Another calibration technique without the replica CP was proposed by Liang et al., a technique in which the currents are fine-tuned by a more complicated digital controller [9].

In addition to the above digital techniques, some analog methods have also been proposed. Dalt and Sander proposed a differential charge pump to reduce the mismatch [10]. The difference between the pull-up current, I_{up}, in one branch and the push-down current, I_{dn}, in the other branch was amplified to tune I_{up} to equal I_{up}. Lee et al. employed a replica CP to make the pull-up and push-down currents equal to the branch current in this replica CP [11]. In the proposal of Sujatha et al., an error amplifier was used to bias the main CP adaptively. This gain boosting technique can also increase the output resistances of the transistors generating the currents [12]. With this scheme, the pull-up and push-down currents are much less sensitive to the geometry of the transistors [12,13]. Excellent results for both 0.35 and 0.18 μm CMOS technologies have been reported by simulation [14].

Recently, Tsitouras et al. investigated a 1-V CP by a 90-nm CMOS technology [15]. In their narrow design space for voltage swing, excellent performances were achieved in their post-layout simulation. With a gain-boosting amplifier, the obtained current mismatch was as low as 1% for the voltage swing up to 70% of the power supply. For problems regarding the non-ideal transient effects in digital switching, Tsitouras et al. employed a unity-gain buffer and extra floating switches at the output. The obtained charge mismatch was suppressed within 6% for the same range of voltage swing.

Lin et al. proposed another strategy by a dynamic CP to fine-tune the pull-up and push-down currents simultaneously by the feedback of the output voltage [16]. In this area efficient design, only two extra control transistors were added to adjust the pull-up and push-down currents. The mismatch was reduced to be within 1.5% for a voltage swing over 56% of the power supply. However, this method may be not as effective as the gain boosting method in dealing with channel length modulation. In our study, a modification of the dynamic CP at the expense of higher transistor counts was investigated. In our circuit, the gain boosting technique was employed to investigate its effect on this CP. In this paper, we will focus primarily on the performances of the current mismatch. The obtained results from simulation and measurement will be compared and discussed in this paper.

2. Charge pump circuits

For comparison, Lin's circuit will be introduced first. Possible issues in this circuit will be also discussed. Then, we will introduce our circuit for investigation.

2.1. Dynamic current-matching charge pump

Fig. 3 depicts the dynamic current-matching charge pump employed in ref. [16]. In this circuit, the current source is 200 μA. With this cross-mirroring scheme, the output voltage, V_{CP}, in the push-pull branch, *PP*, can be isolated from the current sources in branches *L1A* and *L2A*. Therefore, the currents in MP4 and MN4 can be kept almost constant and the same if the feedback transistors MfbP and MfbN do not disturb the currents.

In addition, the switching transistors, MP7 and MN7, are isolated from the output node by MP6 and MN6, respectively. The switching noises from MP7 and MN7 will not directly affect the output. Possible charge sharing due to the switching is also avoided. Such an arrangement of the switching devices is called SS structure [6,16].

The role of feedback control transistors, MfbP and MfbN, is to fine-tune the currents in MP4 and MN4, respectively, according to the output voltage, V_{CP}. When V_{CP} increases, the push-down current is expected to be increased due to the channel length modulation in MN6. In this case, MfbN will operate in the deeper triode region, thereby reducing the gate bias for MN6 and thus the push-down current, I_{dn}. This counter-effect will therefore prevent I_{dn} from changing too much. When V_{CP} decreases, MfbP allows the pull-up current, I_{up}, to remain nearly constant.

According to the above analysis, this smart design makes the CMOS CP less sensitive to the output voltage by adding only two transistors. However, since the output transistors, MP6 and MN6,

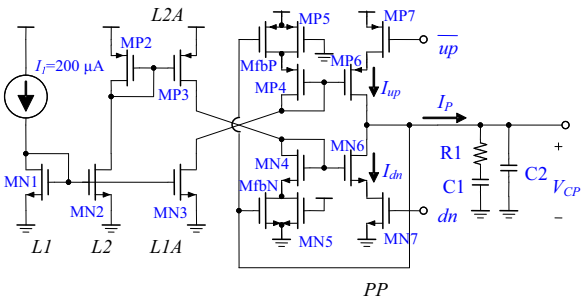

Fig. 3. Schematic of the dynamic current-matching CP [16].

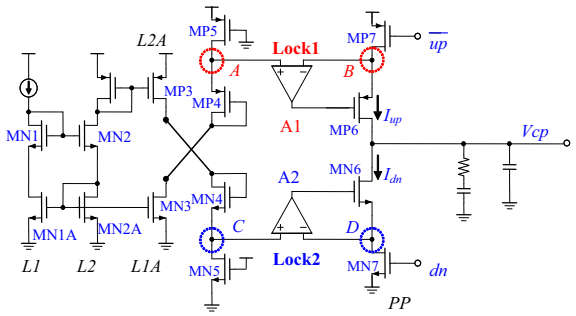

Fig. 4. Gain-boosting charge pump. The devices have the same names in Fig. 3.

directly suffer from the variation of the output voltage, and there is no mechanism to suppress the variation of V_{CP} in this circuit; the effect of channel length modulation, and thus the current mismatching is still a concerned. According to the report in Ref. [16], the simulated mismatching was reduced considerably from 8% for the CP without feedback adjustment to 3% with this area-efficient design that changes V_{CP} from 0.3 V to 1.5 V. However, for cases that pursue a lower current mismatching, the dynamic CP would have limited advantages. In our study, we investigated the effect of the gain boosting technique on the mismatching problem, though this technique would consume more layout area. Our circuit will be explained in the following section.

2.2. Proposed charge pump

In this study, the feedback control transistors, MfbP and MfbN, were removed as shown Fig. 4. In this figure, two differential voltage amplifiers, *A*1 and *A*2, were inserted to reduce the sensitivity of the pull-up and push-down currents to V_{CP}. Two extra NMOSFETs, MN1A and MN2A, were added in the source branches to make the bias conditions in branches *L*1 and *L*2 more similar to those in *L*1*A* and *L*2*A*. Therefore, the drain-to-source voltage drop, V_{DS}, of MP3 becomes similar to that of MP2, and MN2A and MN3 also have similar voltages to that of V_{DS}. This revision does not affect the source currents in *L*1 and *L*2. The primary revision is the replacement of the gate bias for MP6 and MN6 by the added differential amplifiers. With this scheme, the voltages at nodes *B* and *D* are forced to follow nodes *A* and *C*, respectively. When MP7 is turned on by the control signal, $\overline{up}$, since the bias conditions for MP5 and MP7 are very similar, the pull-up current, I_{up}, becomes the same as the branch current flowing through MP5. Similarly, current I_{dn} becomes the same as that in MN5, while MN7 is turned on by signal *dn*. To compensate for the effect caused by the variation of V_{CP}, transistors MP6 and MN6 adjust their gate voltages to keep the same current as those from the source branches.

With such a negative feedback mechanism, the voltage at node *B* is forced to follow that of node *A* when MP7 is turned on. It is the same for nodes *C* and *D* when MN7 is turned on. Therefore, I_{up} and I_{dn} are less affected by V_{CP} even at the presence of the channel length modulation effect.

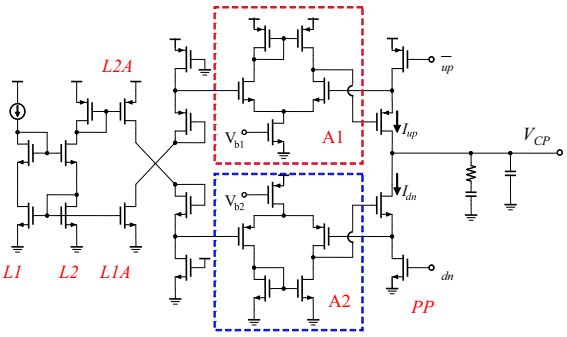

Fig. 5. Detailed circuit of the gain-boosting charge pump in Fig. 4.

Fig. 5 depicts the detailed circuit of our CP with the insertion of two gain-boosting amplifiers. In this circuit, the dimensions of the PMOS transistors were chosen to match the resistances of the NMOS transistors. In our design, the width ratio of PMOS over NMOS was 2 with the same gate length. The tail currents in the amplifiers, *A*1 and *A*2, were also chosen to be the same as the current source, I=200 μA. According to our simulation, the voltage gains were believed to be high enough to overcome possible variations due to the uncertainty of process, temperature, and supply voltage.

This circuit was verified and fabricated by the 0.18-μm 1P6M CMOS technology of TSMC. Fig. 6(a) illustrates the physical layout of the proposed design; Fig. 6(b) shows the chip die's photo. In this chip, a PFD, the gain-boosting CP, and an LPF circuit were included in an attempt to design an integrated PLL. The design of the PFD and the LPF is beyond the scope of this paper and therefore will not be discussed. However, as seen in this figure, the area of the gain-boosting CP is not large compared to the other passive elements, making it efficient, especially for the capacitors. The area of the CP is only about half that of the PFD in our design. Fig. 6(c) shows the enlarged micrograph of the PFD and CP. In this figure, the dimension of the CP is 40 × 40 μm^2. They are 100 × 30 μm^2 and 609 × 609 μm^2 for the PFD and the whole chip, respectively.

3. Simulation and measurement setups

In this study, the models for TSMC's 0.18-μm CMOS technology were employed in the simulation by HSPICE. The power supply for this circuit was set at 1.8 V. In our simulation, possible process variations were considered by combinational employing fast, slow, and typical models for PMOS and NMOS. Possible effect due to the physical layout was also considered to simulate the performances by extracting the parasitic elements, when simulating the circuit performance.

In our measurement, the same power supply was applied as in the simulation. In addition, the sample was mounted on a printed circuit board for reliable results. In this experiment, as illustrated in Fig. 7, E3631A of Agilent Inc. was used as the DC power supplier, AWG 7102 of Tektronix Inc. was used for switching control, and a source measurement unit of Keithley 2400 was employed to measure the relation between the pumping currents and the output voltage, V_{CP}. By setting the voltage source and current measurement mode in Keithley 2400, V_{CP} can be set by Keithley 2400 and the net pumping current, I_p=I_{up}–I_{dn}, can be obtained. The pull-up and push-down currents can be measured separately by turning on MP7 or MN7, as shown in Fig. 4, when the control waveforms were generated by AWG 7102.

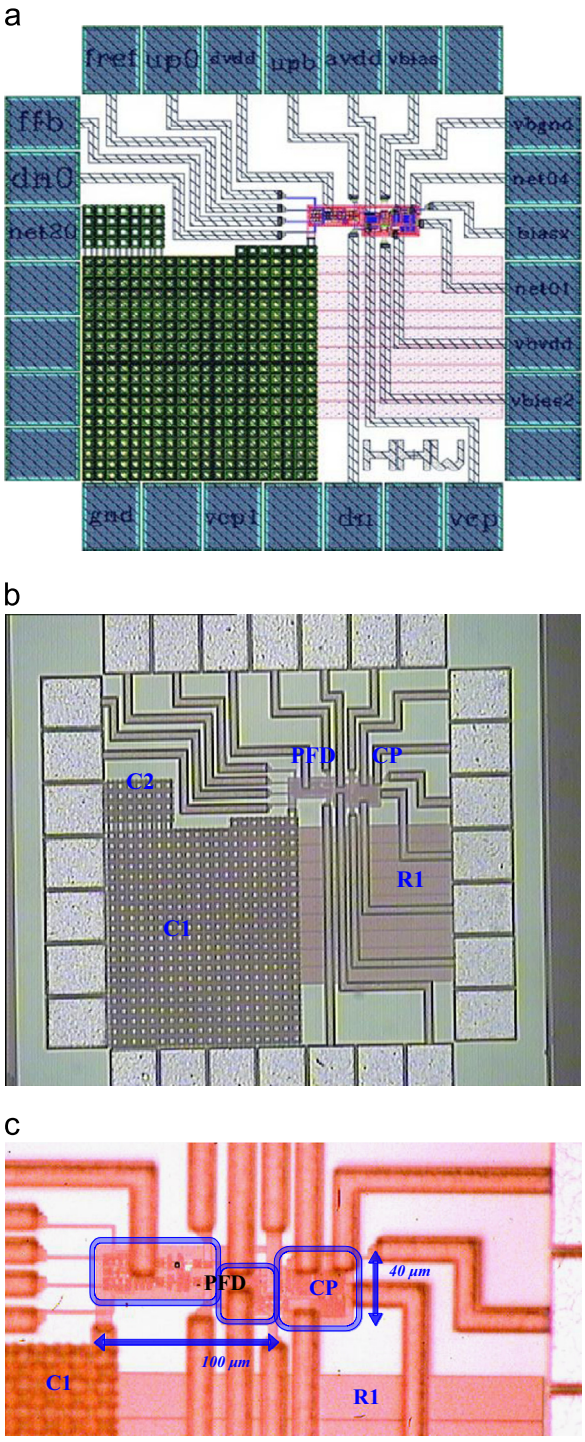

Fig. 6. (a) Physical layout of our chip (c). Micrograph of the returned chip and (b) enlargement of the PFD and CP.

4. Results and discussion

The circuit without compensation was estimated first in our study. Fig. 8 is the resulting mismatch for the circuit in Fig. 3 in which the feedback transistors, MfbP and MfbN, were removed. The simulated mismatch characteristics of the compensated CP in Figs. 4 and 5 are shown in Fig. 9.

In our simulation, the parasitic elements aroused by the physical layout were considered. Fig. 9 shows the simulation results for the circuit with and without parasitic elements. In this simulation, possible fabrication variation was not considered.

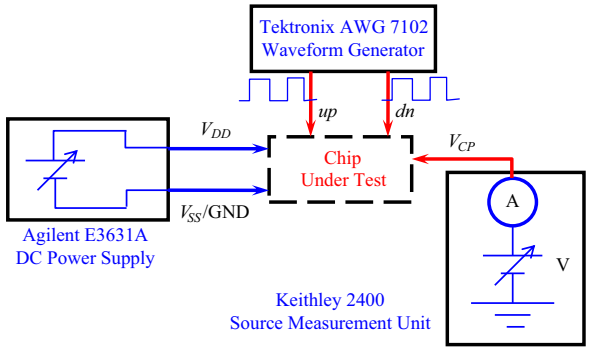

Fig. 7. Setup for mismatch measurement.

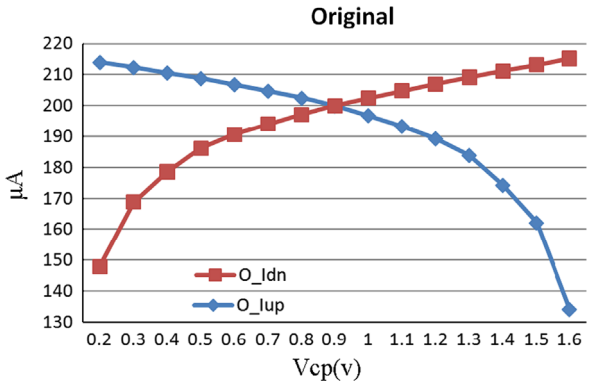

Fig. 8. Simulated current mismatch charateristic of the uncompensated charge pump.

Therefore, the models of the NMOS and the PMOS with typical characteristics were employed in this simulation. The effect of process variation will be discussed later in this section.

When considering the parasitic elements in the layout, it can be seen in Fig. 9(b) that the resulting currents increase. This finding may be attributed to the small interconnect resistance that changes the node voltages of each transistor. Nevertheless, the parasitic effect is minor in predicting the output current mismatch.

According to the results in Figs. 8 and 9, the swing range for V_{CP} was focused from 0.3 V to 1.5 V which is 67% of the power supply of 1.8 V in this study. For a smaller amount of current mismatch, V_{CP} ranging from 0.4 V to 1.4 V, i.e. 56% of V_{DD}, will also be discussed. In our study, the mismatch is defined as the ratio of the difference between I_{up} and I_{dn} at the same output voltage V_{CP} over the nominated current, I=200 μm, such that

$$\left.\frac{|I_{up}-I_{dn}|}{I}\right|_{V_{CP}} \times 100\% \quad (1)$$

For the data obtained in Fig. 8 for the uncompensated circuit, the current mismatches for V_{CP} at 0.3 V, 0.4 V, 1.4 V, and 1.5 V are 32%, 19%, 23%, and 35%, respectively. As seen in Fig. 8, one can see that the effect of channel length modulation is significant for the transistors of the 0.18 μm technology.

According to the curves in Fig. 9(b), the obtained mismatch is 2% for V_{CP}=0.3 V and 1% at 0.4 V. As seen in this figure, the voltage range for mismatches less than 1% is about 0.4–1.4 V. In this voltage range, the slopes of the curves in Fig. 9(a) and (b) are as low as 0.15 μA/V.

In addition to the current variations, our simulation showed that the power consumptions for our CP and the whole circuit without switching were 2.2 mW and 3.37 mW, respectively. The switching frequency can be operated up to 20 MHz.

Further investigation was performed to check the possible variation due to the uncertainty in fabrication. In our post-layout simulations of different corners of models, the variation for I_{up} at V_{CP}=0.3 V was within 8 μA. The variation was almost the same for I_{up} at V_{CP}=1.4 V due to the fact that I_{up} had a very low slope in the range for V_{CP} in the 0.3–1.5 V range. The result was similar for I_{dn} in the above considered voltage ranges. Table 1 lists the obtained mismatches for the corner simulations. As listed in Table 1, the worst case of mismatch is less than 5% for a swing range within 67% of the supply voltage.

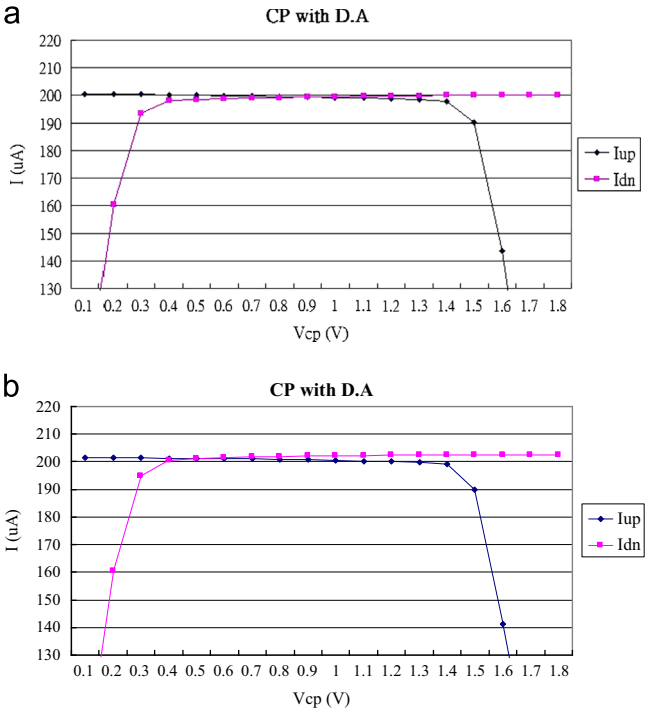

Fig. 9. Results of (a) the prelayout and (b) the post-layout simulations for the proposed charge pump. (a) Pre-Sim result and (b) Post-Sim result.

Table 1
Simulated current mismatch with respect to process variation. The maximum current mismatch for V_{CP} was estimated to be in the range from 0.3 V to 1.5 V. In the first column, *T* is the typical model for the PMOS or NMOS, *S* is the the slow model, and *F* is the fast model. There are five different combinations of models for the PMOS and NMOS in the simulation.

Corner combination of models	0.3 V		1.5 V	
	Pre-Sim (%)	Post-Sim (%)	Pre-Sim (%)	Post-Sim (%)
TT	0.1	0.1	2	3
SS	0.1	0.1	4	5
SF	1	1	3	4
FS	1	1	3	5
FF	0.1	0.5	4	5

According to the results obtained in our simulation, some performance parameters between our study and the related reports are compared in Table 2. In this table, one can find that the mismatches of our CP are consistent with those in Ref. [14] with the same gain-boosting technique. A better current mismatch can be even obtained in Ref. [15] with an advanced technology. Our mismatch results are better than those in Ref. [16], which utilized dynamic feedback compensation. By comparing the mismatches of the uncompensated CP, we find that the current mismatch of our circuit is much worse than those in the other two reports. This may be due to the fact that the sizes of the transistors in our CP were not adjusted to an optimal design. However, one can still see the advantages of the added differential amplifiers on the CP with a not-so-ideal design. From Table 2, the mismatch is improved from 35% in the uncompensated design to less than 2% for the CP, with gain-boosting compensation. According to this finding, it can be concluded that the mismatch characteristics of the CP compensated by a gain-boosting technique would be less sensitive to the sizes of the transistors. With a suitable voltage gain in the amplifiers, the current mismatch in the CP can be significantly improved. It can also be found that the minimum mismatch in Ref. [14] is smaller than ours by an order. Since the considered voltage range in Ref. [14] was from 0.5 V to 1.2 V, it is not easy to make a precise comparison between these two circuits. Nevertheless, it is believed that the mismatch characteristics between our circuit and that in Ref. [14] are similar.

All the predicted performances in our simulation were verified by measuring the fabricated chips. The measured mismatch characteristics are shown in Fig. 10. By comparing the results obtained in Figs. 9(b) and 10, we can see the variation of the currents in the voltage range from 0.3 V to 1.5 V is very small. The measured mismatches at V_{CP}=0.3 V, 0.4 V, 0.5 V 1.4 V, and 1.5 V were 8.1%, 1.9%, 1.1%, 1.2%, and 2.2%, respectively. The range of voltage swing with the mismatch in 1% was from 0.5 V to 1.4 V, which is 50% of V_{DD}. These results are very close to those obtained in our post-layout simulation.

5. Conclusion

In this study, a compensated CMOS charge pump was investigated by gain-boosting amplifiers. The circuit was fabricated by

Table 2
Comparison of current mismatch properties obtained by simulation.

CP	Ref. [16]		Ref. [15]	Ref. [14]		This work, Fig. 4	
Compensation technique	Dynamic feedback		Gain-boosting	Gain-boosting		Gain-boosting	
Fabrication technology	0.18-μm CMOS		90-nm CMOS	0.18-μm CMOS		0.18-μm CMOS	
Power supply, V_{DD}	1.8 V		1.0 V	1.8 V		1.8 V	
Output current	~100 μA		<200 μA[a]	~600 μA		200 μA	
Compensation	w/o	w/	w/	w/o	w/	w/o	w/
Mismatch at 70% of V_{DD}[a]			<1%				
Mismatch at 67% of V_{DD}[b]	<8%	<3%				<35%	<2%
Mismatch at 56% of V_{DD}[c]	<3%	<1%				<23%	<1%
Mismatch at 38% of V_{DD}[d]				<5%	<0.1%		

[a] V_{CP} swing range was from 0.15 V to 0.85 V with programmable output current.
[b] V_{CP} swing range was from 0.3 V to 1.5 V.
[c] V_{CP} swing range was from 0.4 V to 1.4 V.
[d] V_{CP} swing range was from 0.5 V to 1.2 V.

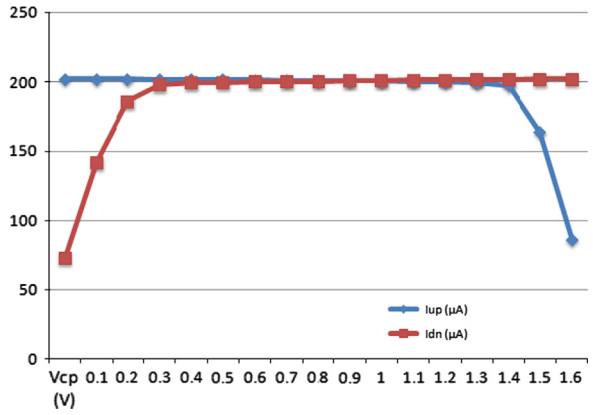

Fig. 10. The measurement of proposed current-matching charge pump.

TSMC's 0.18-μm 1P6M CMOS technology. The performance of our circuit was investigated and verified by simulations and measurements. The performances of the circuits with and without compensation were estimated by simulation. The circuits compensated by dynamic feedback in Ref. [16] and gain-boosting amplifiers were also compared with circuits with the same current mapping architecture. The obtained mismatch was less than 1% for the output voltage seeping from 0.4 to 1.4 V. This result is lower than that compensated by the dynamic feedback tuning.

According to our comparison, the gain-boosting technique exhibited excellent compensation effect on the current mismatch characteristics. For the cases in which transistor count is not an critical issue, the gain-boosting technique may be a good choice for the design of a CP to improve its mismatch chracteristics.

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