Optimal Common-Centroid-Based Unit Capacitor Placements for Yield Enhancement of Switched-Capacitor Circuits

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Yield is defined as the probability that the circuit under consideration meets with the design specification within the tolerance. Placement with higher correlation coefficients has fewer mismatches and lower variation of capacitor ratio, thus achieving higher yield performance. This study presents a new optimization criterion that quickly determines if the placement is optimal. The optimization criterion leads to the development of the concepts of C-entries and partitioned subarrays which can significantly reduce the searching space for finding the optimal/near-optimal placements on a sufficiently large array size.

Categories and Subject Descriptors: B.7.2 [**Integrated Circuits**]: Design Aids—*Placement and routing*

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1. INTRODUCTION

As semiconductor technology continues to shrink, process variation problems become inevitable. It is anticipated that the problem of uncontrollable process variation will become more serious. As a result, yield loss caused by process variation becomes an important design issue. In order to bring the process variation to the early design stage, the process variation information must be injected to the circuit simulator.

Process corners are generally considered in circuit simulation. It uses the device process boundary to simulate the yield loss phenomenon. However, the device boundaries are usually not the performance boundary. The performance space may be within or overstep the corner space [Luo et al. 2008], which results in either overkill or overpass. To improve the accuracy of yield analysis, the time-consuming Monte-Carlo analysis is commonly employed.

Devices mismatch can be attributed to two sources of errors: random mismatch and systematic mismatch [Liu et al. 2008]. Random mismatch is usually caused by process

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variation; on the other hand, systematic mismatch is mainly due to asymmetrical layout and processing gradients. The key performance of many analog integrated circuits, such as analog-to-digital converters (ADCs) and sample and hold, is directly related to accurate capacitance ratios [McNutt et al. 1994]. The capacitance ratio mismatch problem can be alleviated by using parallel unit capacitances [Khalil et al. 2005], and the precision of the unit capacitance array can be further improved by common centroid structures [Khalil et al. 2005; Khalil and Dessouky 2002; Ma et al. 2007; Hastings 2000]. These structures significantly reduce the effects of gradients and random errors in fabrication.

Perfectly matched devices in the common centroid structure must satisfy the following four conditions [Hastings 2000]: coincidence, symmetry, dispersion, and compactness. A number of layout rules were developed for guiding designers to develop an appropriate layout that meets these conditions [Khalil et al. 2005; Khalil and Dessouky 2002; Ma et al. 2007; Hastings 2000]. However, the layout shape must be rectangular to meet these four conditions. Moreover, which condition achieves better matching is generally difficult to determine without performing the time-consuming yield evaluation process [Chen et al. 2009, 2010; Luo et al. 2011].

In reality, there exist some correlations among devices which highly depend on their spatial locations [Xiong et al. 2007; Doh et al. 2005]. The closer devices generally have the similar parameter variation. It has been shown that placement with higher correlation coefficients has fewer mismatches and lower variation of capacitor ratio, and thus higher yield performance [Luo et al. 2008]. The optimization criterion was proposed in Chen et al. [2010] to quickly generate optimal/near-optimal placements with the highest/near-highest correlation coefficients for the ratio of two capacitors or a continuous capacitor ratio (multiple capacitors). The algorithm has been successfully implemented to a charge-redistribution (CR) successive-approximation register (SAR) analog-to-digital converter (ADC) design for yield enhancement [Lin et al. 2011]. The optimal/near-optimal placements were generated without the need of the Monte-Carlo simulations.

However, the optimization criteria in Chen et al. [2010] and Lin et al. [2011] were oversimplified. It may not be always true that the higher correlation coefficients result in lower variance of ratio. The use of Pearson's correlation coefficient [Chen et al. 2010] to define the optimization criterion is too optimistic. Counterexamples will be presented shortly to illustrate the contradiction. On the other hand, the optimization criterion in Lin et al. [2011] only considers the maximization of R, the sum of cross-correlation coefficients between any pair of unit capacitance. Counterexamples will also be provided to show that placement with larger values of R may not always result in smaller standard deviation or smaller variance. This leads to the development of a new optimization criterion which can quickly and effectively identify the better placement. The resultant placement is confirmed by Monte-Carlo simulations. Based on the optimization criterion, a simple yet effective placement generation process is developed.

In the next section, the impact of spatial correlation in yield analysis and the spatial correction model are briefly reviewed. In addition, the optimization criterion proposed [Chen et al. 2010; Lin et al. 2011] is also discussed. Section 3 presents the proposed optimization criterion. Based on the optimization criterion, capacitor placement generation is discussed in Section 4. Finally, a brief concluding remark is given in Section 5.

2. PRELIMINARY

Let μ_{Cs} and μ_{Ct} be the nominal values of two capacitors C_s and C_t, respectively. $\mathrm{Var}(C_s)$ and $\mathrm{Var}(C_t)$ are respectively their variances, and $\mathrm{Cov}(C_s, C_t)$ is the covariance. The

variation of capacitance ratio, Var(C_s/C_t), can be expressed as follows [Luo et al. 2008].

$$Var\left(\frac{C_s}{C_t}\right) = \left(\frac{\mu_{C_s}}{\mu_{C_t}}\right)^2 \left(\frac{VarC_s}{\mu_{C_s}^2} + \frac{VarC_t}{\mu_{C_t}^2} - \frac{2Cov(C_s, C_t)}{\mu_{C_s}\mu_{C_t}}\right). \quad (1)$$

Let C_s and C_t be implemented with p and q unit capacitors (UC), respectively, that is, $C_s = \{C_{s1}, C_{s2}, \ldots, C_{sp}\}$ and $C_t = \{C_{t1}, C_{t2}, \ldots, C_{tq}\}$. The ratio is $C_s : C_t = p : q$. Without loss of generality, the $(p + q)$ UCs are placed on an m-by-n array structure. The self-correlation $\rho_{s(i,j)}$ and $\rho_{t(i,j)}$ denote as the correlation coefficients between C_{si} and C_{sj}, between C_{ti} and C_{tj}, respectively, while the cross-correlation $\rho_{st(i,j)}$ is the correlation coefficients between C_{si} and C_{tj} [Luo et al. 2008]. Let S_{cs} and S_{ct} be the sum of total self-correlation coefficients of C_s and C_t, respectively, and S_{cst} be the sum of the cross-correlation coefficients, that is,

$$S_{cs} = \sum_{i=1}^{p-1} \sum_{j=i+1}^{p} \rho_s(i, j);\ S_{ct} = \sum_{i=1}^{q-1} \sum_{j=i+1}^{q} \boldsymbol{\rho}_t(i, j);\ S_{cst} = \sum_{i=1}^{p} \sum_{j=1}^{q} \boldsymbol{\rho}_{st}(i, j). \quad (2)$$

Let μ_{Cu} and σ_{Cu} denote the nominal value and standard deviation of a UC, respectively. With the assumption that all UC's have the same means and variances, Var(C_s/C_t) can be expressed as follows [Luo et al. 2008]:

$$Var\left(\frac{C_s}{C_t}\right) = \left(\frac{p}{q}\right)^2 \left(\frac{\sigma_{cu}}{\mu_{cu}}\right)^2 \left(\frac{p + 2S_{cs}}{p^2} + \frac{q + 2S_{ct}}{q^2} - \frac{2S_{cst}}{pq}\right). \quad (3)$$

Consider the Pearson's correlation coefficient [Luo et al. 2008],

$$\rho_{cst} = \frac{Cov(C_s, C_t)}{\sqrt{Var(C_s)\,Var(C_t)}}. \quad (4)$$

By substituting Eq. (1) to Eq. (3), we obtain

$$\rho_{cst} = \frac{S_{cst}}{\sqrt{(p + 2S_{cs})(q + 2S_{ct})}}. \quad (5)$$

Based on Eq. (5), the following property was concluded in Luo et al. [2008] that the higher correlation coefficient ρ_{cst} results in a smaller Var(C_s/C_t). Since the smaller variance of the capacitor ratio generally results in higher yield performance, hence, the higher correlation coefficient will result in higher yield performance. Thus, the correlation coefficient ρ_{cst} was employed in Chen et al. [2010] to quickly determine which placement may achieve higher yield performance without executing the time-consuming Monte-Carlo simulations.

To deal with the continuous ratio C_1:C_2:. . .:C_N, the ratio of multiple capacitors, several evaluation functions have been recently proposed [McNutt et al. 1994; Khalil et al. 2005; Khalil and Dessouky 2002; Ma et al. 2007]; an effective capacitor placement methodology based on spatial correlation has been proposed [Chen et al. 2010] and implemented to the design of SAR ADCs [Lin et al. 2011]. More specifically, let ρ_{ij} be the correlation coefficient of a pair of capacitors, C_i and C_j. The placement optimization problem was formulated to maximize the value of R [Chen et al. 2010], where

$$R = \left\{\sum \boldsymbol{\rho}_{ij} \mid i, j = 1, 2, \ldots, n, \text{and } i < j\right\}. \quad (6)$$

The UC placement with the maximum R will be the optimal or near-optimal one.

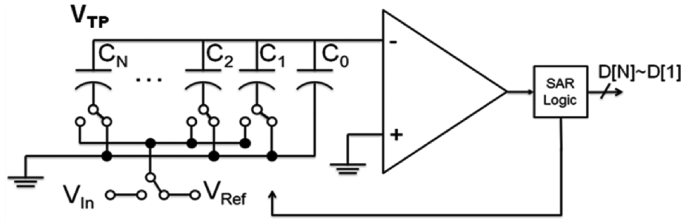

Fig. 1. A common N-bit charge redistribution SAR ADC.

3. OPTIMIZATION CRITERIA

We first present the variance analysis used to examine the optimization criteria in Chen et al. [2010] and Lin et al. [2011] for a pair of capacitance ratio and a continuous capacitance ratio. Then, the counterexamples for both criteria proposed in [Chen et al. 2010; Lin et al. 2011] are illustrated. Finally, a new optimization criterion is presented with the confirmation of Monte-Carlo simulation results.

3.1. Variance Analysis

Eq. (1) can also be written as

$$Var\left(\frac{C_s}{C_t}\right) = \left(\frac{1}{\mu_{C_t}^4}\right)\left(\mu_{C_t}^2 Var C_s + \mu_{C_s}^2 Var C_t - 2\mu_{C_s}\mu_{C_t} Cov(C_s, C_t)\right). \tag{7}$$

Similarly, we can also obtain

$$Var\left(\frac{C_t}{C_s}\right) = \left(\frac{1}{\mu_{C_s}^4}\right)\left(\mu_{C_t}^2 Var C_s + \mu_{C_s}^2 Var C_t - 2\mu_{C_s}\mu_{C_t} Cov(C_s, C_t)\right). \tag{8}$$

By Eqs. (7) and (8), one can derive

$$Var\left(\frac{C_s}{C_t}\right) = \left(\frac{\mu_{C_s}^4}{\mu_{C_t}^4}\right) Var\left(\frac{C_t}{C_s}\right), \tag{9}$$

and

$$Var\left(\frac{C_s + C_t}{C_s}\right) = Var\left(\frac{C_t}{C_s} + 1\right) = Var\left(\frac{C_t}{C_s}\right). \tag{10}$$

Thus, the following property holds.

PROPERTY 1.

(a) *Minimizing* $Var(C_s/C_t)$ *is equivalent to the minimization of* $Var(C_t/C_s)$.
(b) *Minimizing* $Var(C_s/(C_s + C_t))$ *is equivalent to the minimization of* $Var(C_s/C_t)$.

3.2. Examining Optimization Criterion *R*

Figure 1 shows a CR-SAR-ADC [Lin et al. 2011] which is comprised of a capacitor array, a comparator, and control units.

Consider an N-bit SAR ADC that includes the capacitors $C_i, i = 0, 1, \ldots, N$. The capacitance ratios are

$$C_{\mathrm{N}} : C_{N-1} : \ldots : C_2 : C_1 : C_0 = 2^{N-1} : 2^{N-2} : \ldots : 2 : 1 : 1 \tag{11}$$

Let C_i^* denote the sum of all capacitances excluding $C_i, i = 1, 2, \ldots, N$.

$$C_i/(C_i + C_i^*) = 2^{i-1}/2^N = 1/2^{N-i+1}., i = 1, 2, \ldots, N \tag{12}$$

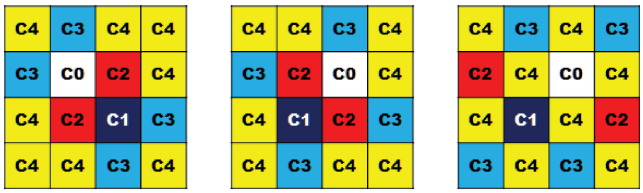

Fig. 2. Placements of four-bit SAR ADC: (a) and (b) placements in Lin et al. [2011]; and (c) proposed.

Table I. Standard Deviation and R

Placement	Std(C_j/C_{total})				R
	$j=1$	$j=2$	$j=3$	$j=4$	
Fig. 2(a)	0.0021	0.0027	0.0034	0.0049	9.3015
Fig. 2(b)	0.0021	0.0027	0.0028	0.0045	9.3199
Fig. 2(c)	0.0021	0.0027	0.0036	0.0029	9.2572

Table II. MC Simulation with $\mu_{C_u} = 100$ fF, $\sigma_{C_u} = 10$ fF, and $\rho_0 = 0.9$

Placements	Std(C_j/C_{total})			
	$j=1$	$j=2$	$j=3$	$j=4$
Fig. 2(a)	0.0022	0.0028	0.0035	0.0050
Fig. 2(b)	0.0022	0.0028	0.0028	0.0046
Fig. 2(c)	0.0022	0.0027	0.0037	0.0029

By Property 1(b), minimizing Var(C_i/(C_i+C_i*)) is equivalent to the minimization of Var(C_i/C_i*).

Example 1. Consider the placements [Lin et al. 2011] in Figures 2(a) and 2(b) with continuous ratio C_4:C_3:C_2:C_1:C_0 = 8:4:2:1:1. The unit capacitor C_u is 100 fF, the standard deviation of unit capacitor is 10 fF, and the unit correlation coefficient ρ_0 is 0.9.

One can generate a 16-by-16 correlation coefficient matrix [Luo et al. 2008] and calculate the variance and covariance of the capacitances. For the placement in Figure 2(c), $C_4^* = C_0 + C_1 + C_2 + C_3$ and $C_{Total} = C_4 + C_4^*$. By Eq. (2), we obtain Var(C_4) = Var(C_4^*) = 5228.5, and Cov(C_4, C_4^*) = 5186.6. By Eq. (3), the variance of ratio Var(C_4/C_{Total}) = 8.1913e-6. Thus, the standard deviation is Std(C_4/C_{Total}) is 0.0029. Similarly, one can compute the standard deviations of C_1/C_{Total}, C_2/C_{Total}, and C_3/C_{Total}, and the R values for the placements, as shown in Table I. The mean values of C_1/C_{Total}, C_2/C_{Total}, C_3/C_{Total}, and C_4/C_{Total} are 0.0625, 0.125, 0.25, and 0.5, respectively. Note that, for simplicity, the systematic mismatch was ignored because the array size is small and the capacitors, (C_2, C_3, C_4), with even numbers of unit capacitors, have the common center point.

Similarly, one can derive the standard deviations of the other placements, as shown in Table I. Results show that both placements in Figures 2(a) and 2(b) have higher values of R than that in Figure 2(c), so is the standard deviation of the most significant bit (MSB), that is, C_4/C_{Total}. The situation becomes significant when the bit number increases.

In order to confirm the correctness of the computed values in Table I, the Monte-Carlo (MC) simulation was conducted to compute the variance. With 10,000 samples, the simulation results are tabulated in Table II.

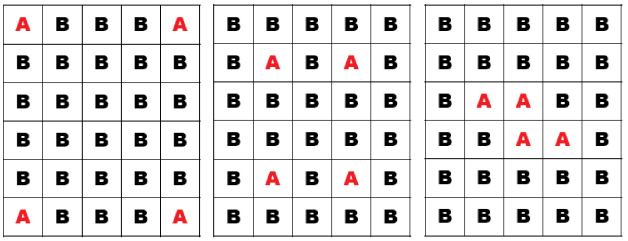

Fig. 3. Common-centroid-based placements.

Table III. Calculated Values with $\rho_0 = 0.5$

Placements	$p+2S_{cs}$	$q+2S_{ct}$	$2S_{cst}$	ρ_{cst}	$\mathrm{Var}(C_s/C_t)$
Fig. 3(a)	4.4224	160.7778	28.4144	0.5328	5.7042E-5
Fig. 3(b)	5.8288	142.1754	45.6104	0.7922	3.2203E-5
Fig. 3(c)	8.9254	138.2296	46.4596	0.6613	7.4696E-5

3.3. Examining Optimization Criterion ρ_{cst}

Let C_s and C_t be implemented with 4 and 26 unit capacitors which are placed on a 6-by-5 array structure, that is, $p = 4$ and $q = 26$, Figure 3 shows three different placements and the associated values are computed and tabulated in Table III, where $\mu_{Cu} = 100$ fF, $\sigma_{Cu} = 10$ fF and the $\rho_0 = 0.5$ were assumed. Results show that the placement in Figure 3(b) results in the highest correlation coefficient ρ_{cst} and the lowest variance of ratio, $\mathrm{Var}(C_s/C_t)$. This endorses that the placement with higher correlation coefficient results in lower variance of ratio [Luo et al. 2008].

However, for the placements in Figures 3(a) and 3(c), the former has lower ρ_{cst} than the latter, by the conclusion [Luo et al. 2008], the former should have higher variance of ratio than the latter. By Table III, the former one has lower $\mathrm{Var}(C_s/C_t)$. This contradicts the conclusion in Luo et al. [2008]. In fact, to obtain higher ρ_{cst}, by Eq. (5), the terms $(p+2S_{cs})^*(q+2S_{ct})$ must be reduced, and the term S_{cst} should be increased. Moreover, to obtain lower $\mathrm{Var}(C_s/C_t)$, by Eq. (3), both $(p+2S_{cs})$ and $(q+2S_{ct})$ must be decreased and S_{cst} should be increased. Both conditions may not be linearly dependent. Therefore, the criterion may not be always true. To further verify the simulation results of the example, the MC simulation with 10,000 samples is adopted for various ρ_0, as shown in Figure 4.

As shown in Figure 4, the placement in Figure 3(a) has lower $\mathrm{Var}(C_s/C_t)$ than Figure 3(c). In addition, Figure 4 also confirms the accuracy of the estimated variance that is calculated by Eq. (3).

3.4. New Optimization Criterion

This sub section presents the proposed optimization criterion.

PROPERTY 2. *Let C_s and C_t be implemented with p and q unit capacitors, respectively, and let the $(p+q)$ unit capacitors be completely placed on an n-by-m array. The sum*

$$\kappa = (p+2S_{cs}) + (q+2S_{ct}) + 2S_{cst} \tag{13}$$

is a constant for any placements of the $(p+q)$ units on this array.

Example 2. Consider the two different placements in Figures 5(a) and 5(b), where $p = q = 4$ on a 2-by-4 array structure. Their correlation matrices are shown in Figures 5(c) and 5(d), respectively.

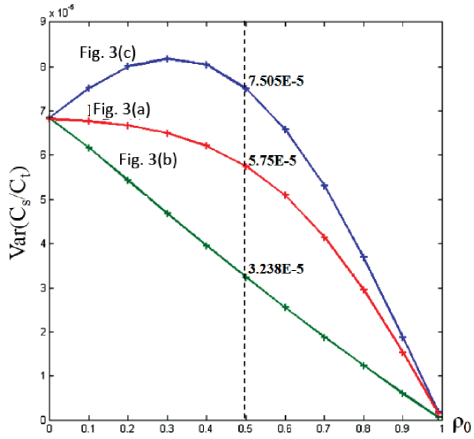

Fig. 4. MC simulation results of the placements in Figure 3.

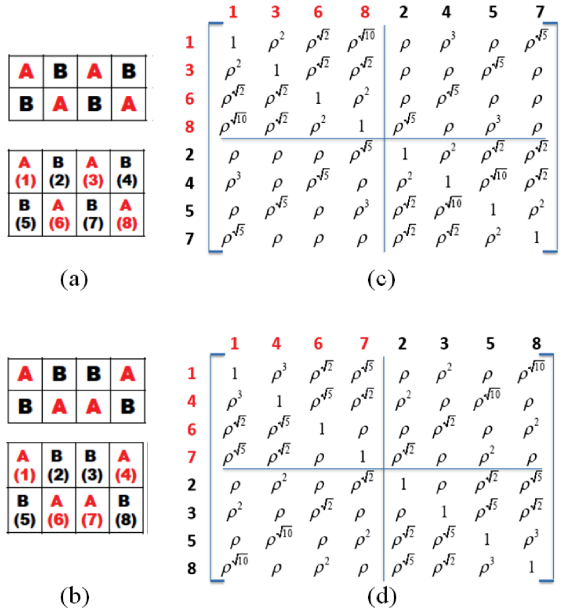

Fig. 5. Common-centroid placements.

Based on the correlation matrices in Figure 5, the correlation coefficients of both cases can be expressed as follows.

$$S_{cs}(a) = S_{ct}(a) = 2\rho^2 + 3\rho^{\sqrt{2}} + \rho^{\sqrt{10}},$$

$$S_{cst}(a) = 10\rho + 2\rho^3 + 4\rho^{\sqrt{5}},$$

$$S_{cs}(b) = S_{ct}(b) = \rho + \rho^3 + 2\rho^{\sqrt{2}} + 2\rho^{\sqrt{5}},$$

$$S_{cst}(b) = 8\rho + 4\rho^2 + 2\rho^{\sqrt{2}} + 2\rho^{\sqrt{10}}.$$

Let k(a) be the coefficient sum of all entries of the matrix in Figure 5(c), then

$$\begin{aligned}\kappa(a) &= (p + 2S_{cs}(a)) + (q + 2S_{ct}(a)) + 2S_{cst}(a)\\ &= 8 + 20\rho + 8\rho^2 + 4\rho^3 + 12\rho^{\sqrt{2}} + 8\rho^{\sqrt{5}} + 4\rho^{\sqrt{10}}.\end{aligned}$$

Similarly, let κ(b) be the coefficient sum of all entries of the matrix in Figure 5(d), and

$$\kappa(b) = 8 + 20\rho + 8\rho^2 + 4\rho^3 + 12\rho^{\sqrt{2}} + 8\rho^{\sqrt{5}} + 4\rho^{\sqrt{10}},$$

that is, κ(b) = κ(a). For $\rho = 0.5$, κ(a) = κ(b) = 25.3686. The matrix in Figure 5(d) is a matrix permutation of that in Figure 5(c). Thus, the total sums of the correlation coefficients for both cases are the same.

PROOF (PROPERTY 2). If two placements have the same number of $(p + q)$ unit capacitors which are placed on the same array, their corresponding correlation matrices have the permutation relationship, that is, one matrix can be obtained from a permutation of the other. Thus, the total sums of the correlation coefficients at all entries in both matrices are the same. □

Based on Property 2, a new optimization criterion can be summarized as the following property.

PROPERTY 3. Given an n-by-m array, both capacitors C_s and C_t contain p and q unit capacitors, respectively. Among the placements on the same array, the one with the lower ω-value will result in the lower variation of ratio,

$$\omega = \frac{S_{cs}}{p} + \frac{S_{ct}}{q}. \tag{14}$$

PROOF. Eqn. (3) can be rewritten as

$$Var(C_s/C_t) = G_1 * (G_2 + 2G_3),$$

where

$$G_1 = \left(\frac{p}{q}\right)^2 \left(\frac{\sigma_{cu}}{\mu_{cu}}\right)^2, G_2 = \left(\frac{1}{p} + \frac{1}{q}\right), G_3 = \frac{S_{cs}}{p^2} + \frac{S_{ct}}{q^2} - \frac{S_{cst}}{pq},$$

Note that p, q, σ_{Cu}, and μ_{Cu} are constants as are G_1 and G_2. Thus, minimizing Var(C_s/C_t) is equivalent to the minimization of G_3. By Eq. (13), we can derive

$$\frac{\kappa - p - q}{2} = S_{cs} + S_{ct} + S_{cst}, or\ S_{cst} = \frac{\kappa - p - q}{2} - (S_{cs} + S_{ct}).$$

Thus,

$$G_3 = \frac{S_{cs}}{p}\left(\frac{1}{p} + \frac{1}{q}\right) + \frac{S_{ct}}{q}\left(\frac{1}{p} + \frac{1}{q}\right) - \frac{(\kappa - p - q)/2}{pq},$$

that is,

$$\frac{S_{cs}}{p} + \frac{S_{ct}}{q} = \left[G_3 + \frac{(\kappa - p - q)/2}{pq}\right] \Big/ \left(\frac{1}{p} + \frac{1}{q}\right).$$

Since p, q, and κ are constants, minimizing $G3$ is equivalent to the minimization of $\omega = S_{cs}/p + S_{ct}/q$. □

By Eq. (13), we have

$$\begin{aligned}\frac{S_{cs}}{p}+\frac{S_{ct}}{q} &= \frac{p(\kappa-p-q)/2+(q-p)S_{cs}-pS_{cst}}{pq}\\ &= \frac{p(\kappa-p-q)/2+(p+q)S_{cs}-p(p+2S_{cs}+S_{cst})+p^2}{pq}\\ &= \frac{\kappa-q+p}{2q}+\left(\frac{1}{p}+\frac{1}{q}\right)S_{cs}-\frac{1}{q}\left(\sum_{i=1}^{p}f(r_i,s_i)\right)\\ &= \frac{\kappa-q+p}{2q}+\frac{1}{q}\left[\left(\frac{q}{p}+1\right)S_{cs}-\sum_{i=1}^{p}f(r_i,s_i)\right],\end{aligned}$$

where (r_i, s_i), $i = 1, 2, \ldots, p$, are the locations of the p unit capacitors of C_s. Let (r, s) be any entry of the n-by-m array,

$$f(r,s)=\sum_{i=1}^{n}\sum_{j=1}^{m}\rho^{\sqrt{(r-i)^2+(s-j)^2}}. \tag{15}$$

The function $f(r, s)$ is referred to as the weight of the entry (r, s) on the n-by-m array [Chen et al. 2009, 2010; Luo et al. 2011]. This concludes that minimizing ω in Eq. (14) is equivalent to the minimization of ω_p, where

$$\omega_p=\left(\frac{q}{p}+1\right)S_{cs}-\sum_{i=1}^{p}f(r_i,s_i),$$

or

$$\omega_p=\frac{n\times m}{p}S_{cs}-\sum_{i=1}^{p}f(r_i,s_i), \tag{16}$$

that is, minimizing the variance of ratio is equivalent to the minimization of ω_p.

4. OPTIMAL COMMON-CENTROID PLACEMENTS

Consider an array size of 2^R by 2^C, without loss of generality, let $C \geqq R$. Both capacitances C_s and C_t contain p and q unit capacitances, respectively, where $p + q = 2^{R+C}$.

Let (r_i, s_i), $i = 1, 2, \ldots, p$, be the locations of the p unit capacitors of C_s on the array. By Eq. (16),

$$\omega_p=\frac{2^{R+C}}{p}S_{cs}-\sum_{i=1}^{p}f(r_i,s_i). \tag{17}$$

Thus, for $p = 1$, we have $S_{cs} = 0$ and, by Eq. (17), $\omega_1 = -f(r_1, s_1)$. Minimizing ω_1 is equivalent to the maximization of $f(r_1, s_1)$.

The entry weights of the 8-by-8 array are illustrated in Figure 6(a), where there are ten distinct entry weights, w1–w10, which can be calculated by Eq. (15), and the computed values for $\rho_0 = 0.5$ are listed in Figure 6(b), where the maximum entry weight w1 = 10.7038.

We denote the entry/entries located at the center of the array as central entry/entries, or *C-entry* or *C-entries*. Figure 6 shows that array containing four C-entries, labeled by w1 and colored in yellow. Figure 6(b) shows that the C-entries have the highest entry

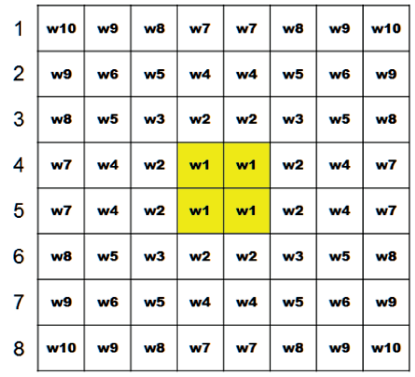

Fig. 6. Computed entry weights.

weight. (The maximum entry weight was defined in Chen et al. [2009, 2010] and Luo et al. [2011] in a similar way.) Thus, the following property holds.

PROPERTY 4. Let $p = 1$, a placement is generated in such a way that the only one-unit capacitor of Cs is placed on the C-entry/C-entries of the array, and the q unit capacitors of C_t are placed on the remaining entries of the array. Then, the placement results in the lowest variation of ratio among the placements on the same array.

PROOF. For $p = 1$, $S_{cs} = 0$. Thus, by Eq. (17), $\mathrm{w}_1 = -f(r, s)$. Since $f(r, s)$ is the highest entry weight of the array, the maximum of $f(r, s)$ results in the lowest w_1 and corresponding variation of ratio. □

For $p = 2$, let (r_1, s_1) and (r_2, s_2) be the locations of the two unit capacitors of C_s on the 2^R-by-2^C array. By Eq. (17), we obtain

$$\omega_2 = 2^{R+C-1} S_{cs} - [f(r_1, s_1) + f(r_2, s_2)]. \tag{18}$$

Consider the 8-by-8 array of $p = 2$. We partition array into two 8-by-4 subarrays, as shown in Figure 7(a). The two unit capacitors for C_s will be respectively placed on the C-entries, marked in yellow, of both subarrays. Similarly, for $p = 4$, let (r_i, s_i), i = 1,2,3,4 be the locations of the two unit capacitors of C_s on the 2^R-by-2^C array. By Eq. (17), we obtain

$$\omega_4 = 2^{R+C-2} S_{cs} - [f(r_1, s_1) + f(r_2, s_2) + f(r_3, s_3) + f(r_4, s_4)]. \tag{19}$$

Figure 7(b) shows that an 8-by-8 array is partitioned into four 4-by-4 subarrays. The C-entries are colored in yellow.

Note that the partitioned subarrays are either the square or rectangular shapes. With the C-entries, the placements meet the rules of *compactness*, *symmetry*, and *dispersion*. If the C-entries near the center are chosen, the placements will meet the rule of *coincidence*.

Placing two unit capacitors on two subarrays, each having four entries, will result in 16 combinations, referred to as *candidate placements*. This has demonstrated that the searching space for optimal placements is significantly reduced from the number of 2-out-of-64, C(64,2) = 2016, to C(4,1)*2 = 16, for the 8-by-8 array. In fact, due to the symmetry of the array, the 16 candidate placements can be categorized into only six distinct placements, as shown in Figure 8, where the $p = 2$ unit capacitors are placed

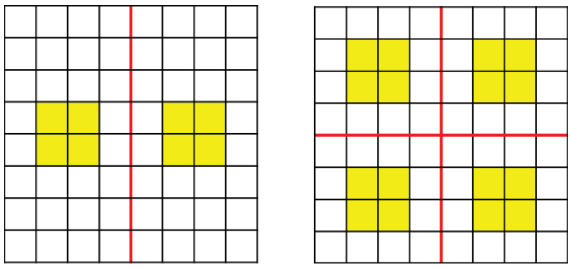

Fig. 7. 8-by-8 array.

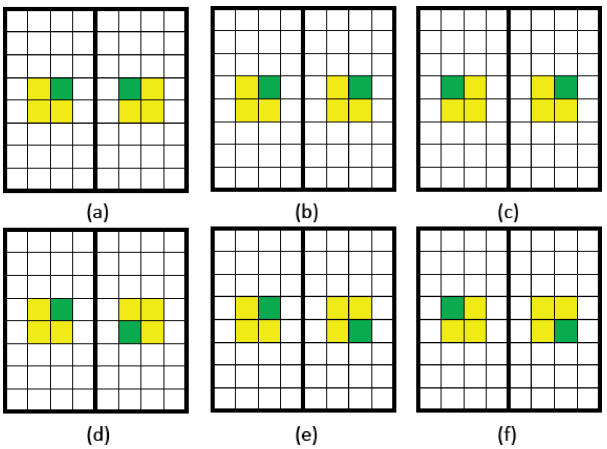

Fig. 8. 8-by-8 array with $p = 2$.

on the locations marked in green. By the rules of common centroid, symmetry, and dispersion, the placements in Figures 8(a)–8(c) will never be the optimal placements.

By Eq. (18), we can easily find that the placements in Figures 8(a) and 8(d) have the same value of $[f(r_1, s_1) + f(r_2, s_2)]$. However, the placement in Figure 8(d) has lower S_{cs} than that in Figure 8(a) thus resulting in lower ω_2. Similarly, for the pairs of the placements in Figures 8(b) and 8(e) and those in Figures 8(c) and 8(f), the placement in Figure 8(e) (Figure 8(f)) has lower ω_2 than that in Figure 8(b) (Figure 8(c)). In addition, lower S_{cs} is also caused by placing the two unit capacitors on the locations with larger distance. The placements in Figures 8(d)–8(f) meet the rules of dispersion and symmetry of common centroid.

Figure 9(a) shows the curve family for all possible placements. The optimal placement is the one in Figure 8(f). Figure 9(b) compares the variances of ratio for the placements with the patterns in Figures 8(d)–8(f). Results show that the one in Figure 8(d) is the optimal solution for $\rho_0 = 0$ to 0.5, while the one in Figure 8(e) is the optimal solutions for $\rho_0 > 0.8$. Thus, the candidate placements in Figures 8(d)–8(f) are optimal/near-optimal solutions depending upon the values of ρ_0.

Similarly, Figure 10(a) shows a 4-by-4 array which is partitioned into four subarrays. Figure 10(b) illustrates a candidate placement. Figure 10(c) plots the variances of ratio with $\rho_0 = 0$ to 1 for all possible placements for placing $p = 4$ to this 4-by-4 array. Results show that the candidate placement in Figure 10(b) is the optimal solution.

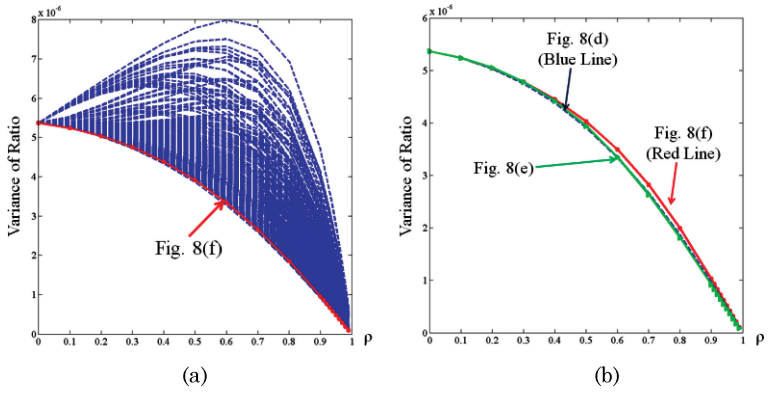

Fig. 9. 8-by-8 array with $p = 2$.

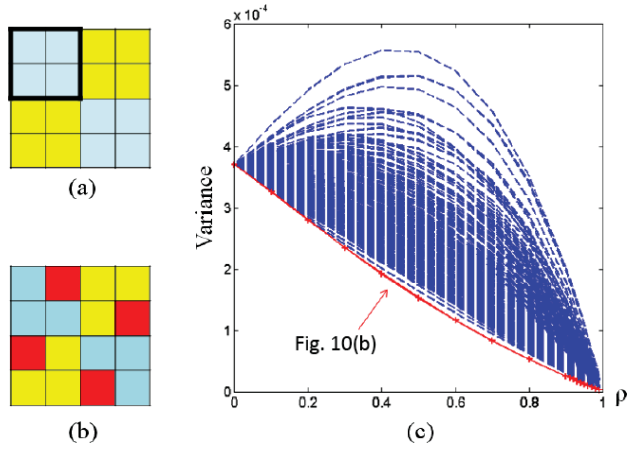

Fig. 10. 4-by-4 array with $p = 4$.

5. CONCLUSION

The yield is defined as the probability that the circuit under consideration meets with the design specification within the tolerance. In practice, however, a circuit generally includes several design variables which are treated as random variables when taking the process variation into consideration. Thus, the variance of the random variables may affect the circuit yield.

The placement with higher correlation coefficients has fewer mismatches and lower variation of capacitor ratio, thus achieving higher yield performance. This study presents a new optimization criterion which can significantly reduce the searching space for finding the optimal/near-optimal solutions for a sufficiently large array size. It should be mentioned that routability of the resulting array is also an important issue to be addressed. A simple routing scheme has been proposed in Huang et al. [2011]; however, systematically considering both placement and routing of the capacitor array is being developed for further yield enhancement.

The concept of C-entries of the partitioned subarrays plays an important role for automatically generating the optimal/near-optimal common-centroid capacitor placement on a reasonably large array. The concept of the C-entries and partitioned subarrays significantly reduces the searching space for the optimal solutions. Even though the

preceding discussions place the emphasis on the 2^R-by-2^C array, the concept of C-entries can be applied for any array size. A simple yet effective automatic placement generation process is being developed [Huang to appear], where partitioning and merging schemes are being implemented to meet the rules of coincidence, dispersion, symmetry, and compactness.

REFERENCES

CHEN, J.-E., LUO, P.-W., AND WEY, C. L. 2009. Yield evaluation of analog placement with arbitrary capacitor ratio. In *Proceedings of the 10th International Symposium on Quality of Electronic Design*, 179–184. DOI: http://dx.doi.org/10.1109/ISQED.2009.4810290.

CHEN, J.-E., LUO, P.-W., AND WEY, C. L. 2010. Placement optimization for yield improvement of switched-capacitor analog integrated circuits. *IEEE Trans. Comput. Aid. Des. Integr. Circ. Syst. 29*, 2, 313–318. DOI: http://dx.doi.org/10.1109/TCAD.2009.2035587.

DOH, J. S., KIM, D. W., LEE, S. H., LEE, J. B., PARK, Y. K., YOO, M. H., AND KONG, J. T. 2005. A unified statistical model for inter-die and intra-die process variation. In *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices*. 131–134. DOI: http://dx.doi.org/10.1109/SISPAD.2005.201490.

HASTINGS, A. 2000. *The Art of Analog Layout*. Prentice Hall, Upper Saddle River, NJ.

HUANG, C.-C., CHEN, J.-E., LUO, P.-W., AND WEY, C. L. 2011. Yield-aware placement optimization for switched-capacitor analog integrated circuits. In *Proceedings of the 24th IEEE International SOC Conference*. 170–173. DOI: http://dx.doi.org/10.1109/SOCC.2011.6085127.

HUANG, C.-C. To appear. Common-centroid-based unit capacitor placement generation for switched-capacitor integrated circuits, Ph.D. dissertation, Department of Electrical Engineering, National Central University, Jhongli, Taiwan.

KHALIL, D. AND DESSOUKY, M. 2002. Automatic generation of common-centroid capacitor arrays with arbitrary capacitor ratio. In *Proceedings of the Conference on Design, Automation and Test in Europe*. 576–580.

KHALIL, D., DESSOUKY, M., BOURGUET, V., LOUERAT, M. M., CATHELINE, A., AND RAGAI, H. 2005. Evaluation of capacitor ratios in automated accurate common centroid capacitor arrays. In *Proceedings of the 6th International Symposium on Quality of Electronic Design*. 143–147. DOI: http://dx.doi.org/10.1109/ISQED.2005.54.

LIN, C.-W., LIN, J.-M., CHIU, Y.-C., HUANG, C.-P., AND CHANG, S.-J. 2011. Common-centroid capacitor placement considering systematic and random mismatches in analog integrated circuits. In *Proceedings of the 48rd Annual Design Automation Conference*. 528–533.

LIU, J., DONG, S., HONG, X., WANG, Y., HE, O., AND GOTO, S. 2008. Symmetry constraint based on mismatch analysis for analog layout in SOI technology. In *Proceedings of the Asia and South Pacific Design Automation Conference*. 772–775. DOI: http://dx.doi.org/10.1109/ASPDAC.2008.4484055.

LUO, P.-W., CHEN, J.-E., HUANG, M.-Y., AND WEY, C. L. 2011. Design methodology for yield enhancement of switched-capacitor analog integrated circuits. *IEICE Trans. Fund. Electron. Commun. Comput. Sci.* E94-A, 1, 352–361.

LUO, P.-W., CHEN, J.-E., WEY, C. L., CHENG, L.-C., CHEN, J.-J., AND WU, W.-C. 2008. Impact of capacitance correlation on yield enhancement of mixed-signal/analog integrated circuits. *IEEE Trans. Comput. Aid. Des. Integr. Circ. Syst. 27*, 11, 2097–2101. DOI: http://dx.doi.org/10.1109/TCAD.2008.2006139.

MA, Q., YOUNG, E. F. Y., AND PUN, K. P. 2007. Analog placement with common centroid constraints. In *Proceedings of the International Conference on Computer-Aided Design*. 579–585. DOI: http://dx.doi.org/10.1109/ICCAD.2007.4397327.

MCNUTT, M. J., LEMARQUIS, S., AND DUNKLEY, J. L. 1994. Systematic capacitance matching errors and corrective layout procedures. *IEEE J. Solid-State Circ. 29*, 5, 611–616. DOI: http://dx.doi.org/10.1109/4.284714.

XIONG, J., ZOLOTOV, V., AND LEI, H. 2007. Robust extraction of spatial correlation. *IEEE Trans. Comput. Aid. Des. Integr. Circ. Syst. 26*, 4, 619–631. DOI: http://dx.doi.org/10.1109/TCAD.2006.884403.

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