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Influence of channel layer and passivation layer on the stability of amorphous InGaZnO thin film transistors

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ABSTRACT

The electrical stability of amorphous InGaZnO (a-IGZO) TFTs with three different channel layers was investigated. Compared with the single channel layer, the a-IGZO TFT with double stacked channel layer showed the lowest threshold voltage shift with slightly change in field effect mobility and sub-threshold swing under positive and negative gate bias stress tests. Moreover, sputtered SiN_x thin film was served as passivation layer where the V_{th} shift in bias stress effect evidently became less. It was found that the passivated a-IGZO TFT with double stacked channel layer still exhibited the best stability. The results prove that the stability of a-IGZO TFTs can be effectively improved by using double stacked channel layer and passivation layer.

1. Introduction

Amorphous oxide semiconductors especially amorphous InGaZnO (a-IGZO) are being used as channel materials in thin film transistors(TFTs) for the applications of next generation active matrix flat panel displays because of their advantages including high mobility, room temperature deposition, excellent uniformity, high flexibility, and good transparency to visible light, etc. [1]. Recently, several prototype displays, such as high definition liquid crystal displays (LCDs), active matrix (AM) flexible displays, and active matrix organic light emitting diode (AMOLED) displays, with a-IGZO TFTs used as driving circuits have been demonstrated [2,3]. Despite of the great progress in the device and process development, the instability of a-IGZO TFTs is still a concern for their practical applications [3,4].

To produce good and stable TFTs, appropriate deposition conditions for channel layer should be considered. For the n-type oxide semiconductor, it is well known that oxygen plays an important role in the properties of thin films and TFT devices [5–7]. For instance, the electrical stability of a-IGZO TFTs with excess oxygen in their active layers degrades due to the defects in the channel layer/gate insulator layer interface and/or acceptor-like defects in the bulk of channel layer [8,9]. Moreover, because of the instability induced by ambient effect for the TFTs with exposed back channel, passivation layer is usually used to improve the stability of oxide semiconductor TFTs [10–12]. However, the effect of the passivation process on the performance of channel layer from plasma damage should be considered in depth.

In this work, the electrical stability of a-IGZO TFTs with three types of channel layers was investigated. More specifically, we fabricated a double stacked channel layer with different deposition conditions and studied their influence on the performance of TFTs. The bias stress effect for the TFTs was studied. Furthermore, TFTs with a sputtered SiN_x passivation layer was studied, and the corresponding passivation effect was discussed.

2. Experimental

The TFTs with bottom gate staggered structure, as shown in Fig. 1, were fabricated on the substrates of n-type silicon (Si) wafers, which were also used as common gate. A 100-nm-thick SiO_2 layer was grown by thermal oxidation of Si wafer. The channel layer and source/drain electrodes were patterned using shadow masks. The fabricated TFTs had a channel length (L) of 200 μm and width (W) of 1000 μm. As a channel layer, a-IGZO film was deposited by RF magnetron sputtering using a target of polycrystalline $In_2Ga_2ZnO_7$ (In_2O_3:Ga_2O_3:ZnO = 1:1:1, mol%) at room temperature. A flow rate of 10 sccm for argon and different oxygen flow rates were used to study the impact of channel layer on the device performance. Three types of channel layers were studied: for sample I, a-IGZO (Ar) thin film as channel layer was deposited without oxygen, called as oxygen-poor IGZO film; for sample II, a-IGZO(Ar + O_2) thin film was deposited with an oxygen flow rate of 2.0 sccm, called as oxygen-rich IGZO film; specially, for sample III with a double stacked channel layer, 20-nm-thick oxygen-poor a-IGZO(Ar) and 10-nm-thick oxygen-rich a-IGZO(Ar + O_2) thin films were served as the front and back channel layers, respectively. The entire channel thickness for three types of TFTs was 30 nm. In deposition the total pressure was fixed at 3 m Torr and the RF

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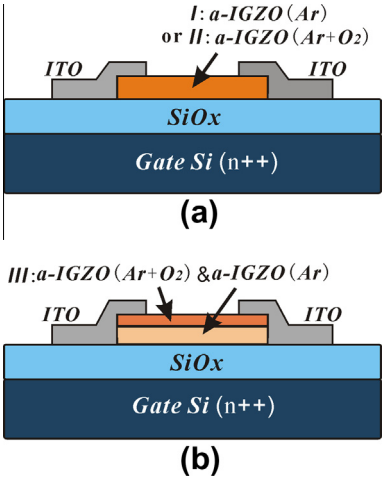

Fig. 1. Schematic diagrams of bottom gate structures for three types of a-IGZO TFTs: (a) samples I and II, and (b) III.

power density was 1.76 W/cm^2. Before the deposition of source/drain electrodes, channel layers were annealed to improve the film quality. Annealing process was performed in nitrogen atmosphere with a thermal furnace at 350 °C for 1 h. Then, a 40-nm-thick ITO thin film was deposited by RF magnetron sputtering to serve as the source/drain electrodes. For the passivated TFTs, 30-nm-thick SiN_x thin films were deposited by RF sputtering using a target of Si_3N_4 (99.99%) at room temperature following the deposition of ITO electrodes. Appropriate conditions including an argon flow rate of 10 sccm, a chamber pressure of 3 m Torr and a RF power density of 1.32 W/cm^2 were selected to reduce the negative effect of passivation process on the TFT performances. Finally, the TFTs were annealed in nitrogen atmosphere at 350 °C for 1 h to improve their electrical properties.

The thickness of channel layer was measured by atomic force microscopy (AFM, Vecco Nanoscope IIIA). X-ray photoemission spectroscopy (XPS, Thermal-fisher ESCLAB 250) was used to analyze the oxygen contents in a-IGZO thin films deposited without and with oxygen incorporation. The electrical performance and stability of a-IGZO TFTs were characterized at room temperature in the ambient atmosphere using Keithley 4200 semiconductor parameter analyzer.

3. Results and discussion

3.1. Thin films' characteristics

To examine the oxygen contents of a-IGZO thin films deposited without and with oxygen incorporation, we performed XPS measurement. The XPS spectra of O 1 s signals in a-IGZO films deposited with and without oxygen are shown in Fig. 2. The O 1 s peak can be fitted by three nearly Gaussian distributions, approximately centered at 530.5, 531.6, and 532.4 eV [13,14]. The low binding energy peak (O_L) at 530.5 eV was related to the O^{2-} ions combined with the Zn, Ga and In atoms in the IGZO compound system. The high binding energy peak (O_H) at 532.4 eV was associated with the loosely bonded oxygen on the surface of IGZO film termed the specific chemisorbed oxygen, such as $-CO_3$, absorbed H_2O or absorbed O_2. The binding energy component (O_M) at 531.6 eV was attributed to O^{2-} ions that were in oxygen deficient region in the IGZO matrix. Compared with the oxygen-poor film, the decrease in the O_M peak for the oxygen-rich film was attributed to the reduction in oxygen vacancies, where the film was compensated with O atoms. The result implies that a-IGZO thin films deposited without oxygen possess more oxygen vacancies than those deposited with oxygen.

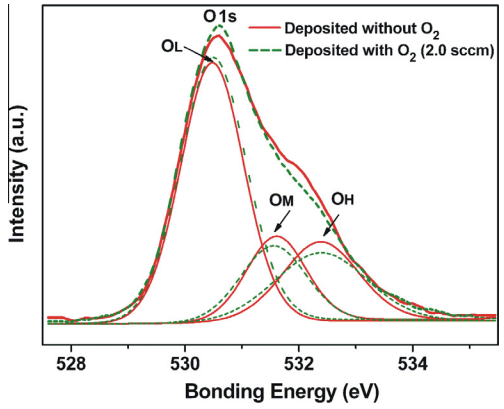

Fig. 2. XPS spectra of the O 1 s region in the a-IGZO films.

3.2. Device characterization

Electrical characteristics of the three types of a-IGZO TFTs (samples I, II, and III) are depicted in Fig. 3, including the transfer characteristics [drain-source current (I_{ds}) versus gate-source voltage (V_{gs})] at V_{ds} = 0.1 V (linear region) and V_{ds} = 10 V (saturation region). All devices were n-type enhancement mode TFTs. Threshold voltage was estimated from the intercept of $I_{ds}^{1/2}$–V_{gs} curve using the standard saturation current equation in the saturation region [15]. Sub-threshold swing (S) and field effect mobility (μ_{FE}) were extracted from the I_{ds}–V_{gs} curve in the linear regime [15]. S is defined as the change in V_{gs} required to change the subthreshold drain current by one decade, given by $S = dV_{gs}/d(\log I_{ds})$ (V/dec).

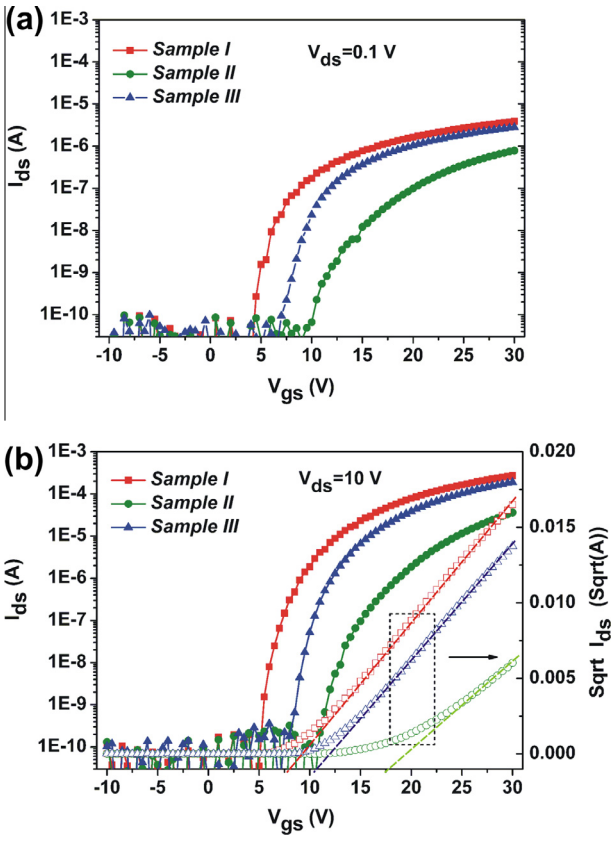

Fig. 3. Transfer curves for a-IGZO TFTs: samples I, II and III, at (a) V_{ds} = 0.1 V (linear region) and (b) V_{ds} = 10 V (saturation region).

Table 1
Electrical characteristics of three a-IGZO TFTs: samples I, II, and III.

Samples	I	II	III
μ_{FE} (cm^2/Vs)	4.00	1.74	3.65
S (V/dec)	0.80	2.62	0.87
V_{th} (V)	8.76	17.40	11.67
$R_{on/off}$	5.20×10^6	1.26×10^6	2.39×10^6
N_{ss} (cm^{-2}/eV)	2.68×10^{12}	9.27×10^{12}	2.93×10^{12}

Here, the S was extracted from one half of the V_{gs} required to increase the threshold current by two orders of magnitude (from 10^{-10} to 10^{-8} A). μ_{FE} was calculated using the following relation: $\mu_{FE}=[g_m L/(WV_{ds}C_i)]$, where g_m is the maximum channel transconductance, and C_i is gate insulator capacitance per unit area. $R_{on/off}$ was defined as the ratio of the maximum to the minimum I_{ds} when V_{ds} was applied at 10 V. The minimum I_{ds} was given by the maximum leakage current, while the maximum I_{ds} was obtained from the highest drain-source current based on the experimental I_{ds}–V_{gs} curves. Besides, the equivalent maximum interface-state trap density N_{ss} at the channel layer-gate insulator interface can be calculated by

$$N_{ss} = \left[\frac{Sig(e)}{\kappa T/q} - 1\right]\frac{C_i}{q} \quad (1)$$

where q is electron charge, κ is Boltzmann constant, T is temperature, and C_i is gate insulator capacitance per unit area [16].

The electrical parameters of three types of a-IGZO TFTs are summarized in Table 1. μ_{FE} of sample I was 4.00 cm^2/Vs, the highest among the three types of devices. It was reported that μ_{FE} considerably increased with the increase of free electron concentration, which was related to the oxygen vacancies in a-IGZO thin films [1]. According to the above XPS results, the a-IGZO thin film deposited without oxygen incorporation had more oxygen vacancies leading to a higher free electron concentration. Therefore, the highest μ_{FE} was obtained for sample I, which was consistent with the previous reports [5]. In addition, sample III showed a lower μ_{FE} and a higher V_{th} than those of sample I. Compared with sample I, sample III using oxygen-rich IGZO film as the back channel layer, has less oxygen vacancies in the entire channel layer, thereby leading to a lower free electron density in the bulk of channel layer. In this case, a less fraction of interface traps and/or traps in the channel layer could be filled, resulting in a larger density of defects at the channel layer/gate insulator interface and thus a corresponding increase in V_{th}. Besides, a lower μ_{FE} for sample II was not only attributed to a lower free electron density in the channel layer, but also a higher channel resistive and a higher contact resistance between channel layer and source/drain electrodes owing to the oxygen-rich film as the back channel layer [17]. Moreover, the equivalent maximum interface-state trap densities of three types of TFTs were shown in Table 1. It was observed that sample III exhibited a similar interface states with sample I, which was better than that of sample II. For sample II, with the introduction of oxygen to produce oxygen-rich channel layer more traps could be created at the channel layer-gate insulator interface by the oxygen plasma damage, causing an increase in N_{ss} [12]. The results indicated that an improved interface between channel layer and gate insulator can be achieved by using IGZO film deposited without oxygen incorporation.

3.3. Effect of electrical bias stress

To investigate the device stability under electrical bias stress, DC positive and negative gate bias stresses (PBS/NBS) at room temperature in the atmosphere for 1500 s were applied. The variation of transfer curves for three types of a-IGZO TFTs under PBS condition of V_{gs} = 20 V and V_{ds} = 0 V are illustrated in Fig. 4a–c respectively. All the devices exhibited positive shifts of V_{th} with little change in S and μ_{FE}. The values of ΔV_{th} obtained at 1.5 k s for samples I, II, and III were 4.15, 5.19, and 3.08 V, respectively. Generally,

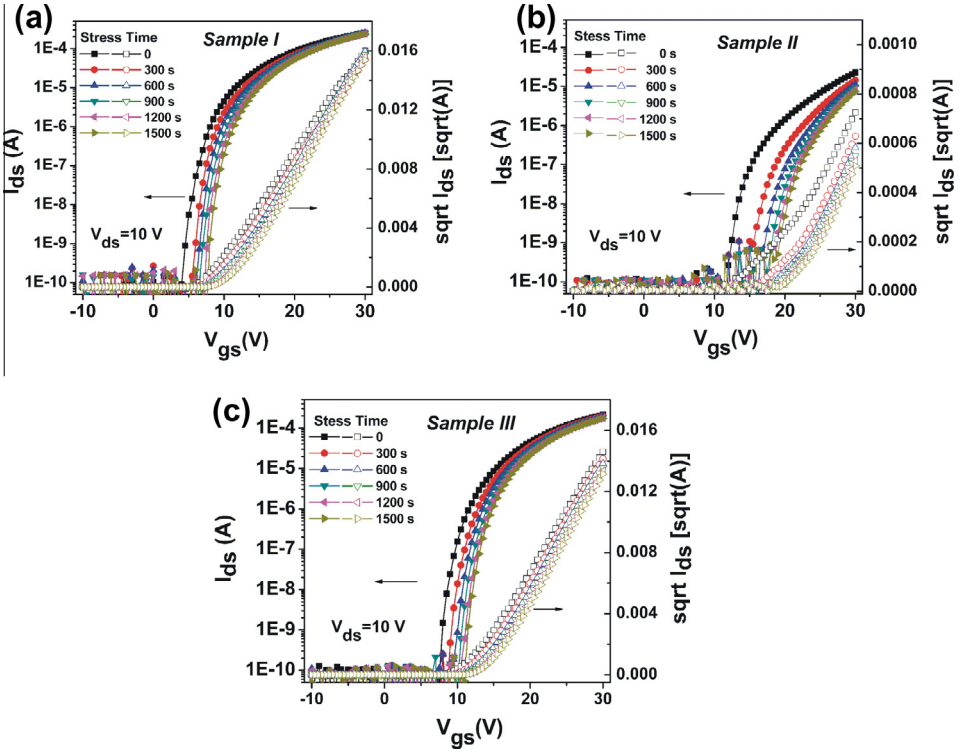

Fig. 4. Variation of transfer curves for three types of a-IGZO TFTs under positive bias stress (V_{gs} = 20 V, V_{ds} = 0 V): samples (a) I, (b) II, and (c) III, respectively.

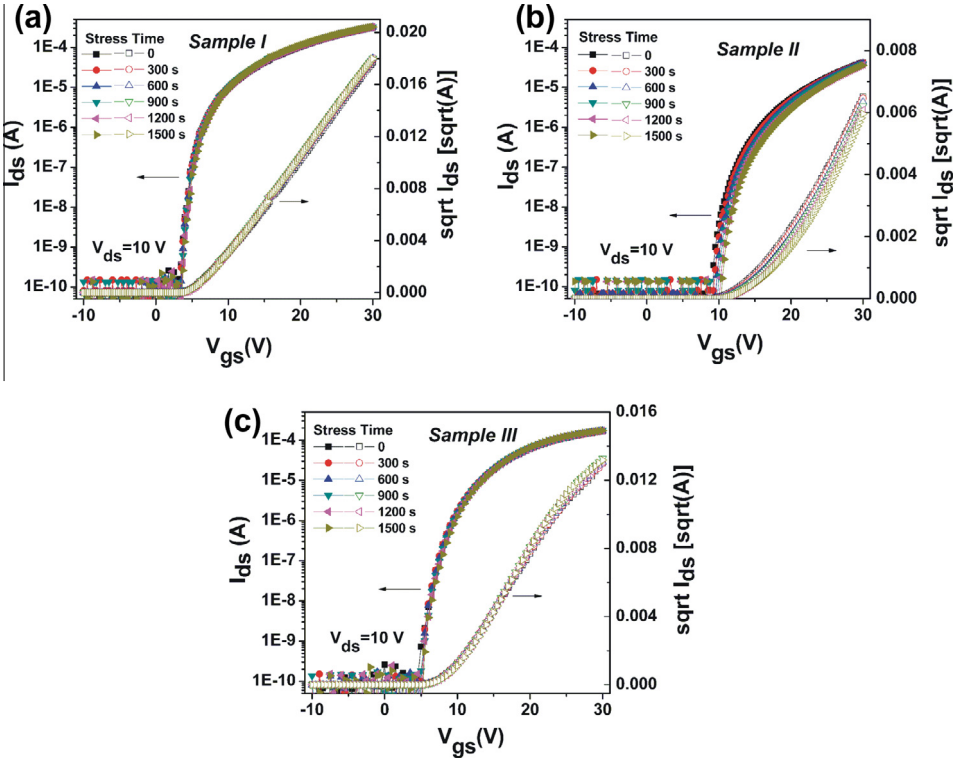

Fig. 5. Transfer curves for samples (a) I, (b) II, and (c) III as a function of duration time under negative bias stress (V_{gs} = −20 V, V_{ds} = 0 V).

the positive V_{th} shift with little or no change in S and μ_{FE} under PBS is dominantly attributed to the electron trapping at or near the channel layer/gate insulator interface without the creation of new defects [18]. Among the three types of TFTs, the largest interface traps for sample II resulted in the largest value of V_{th} shift. Although samples I and III showed similar interface trap densities, a lower value of V_{th} shift was obtained for sample III. This might be related to the different back-channel layers between samples I and III, because the surface/ambience interaction can also impact the stability of unpassivated TFTs. It was reported that the adsorbed oxygen atoms on the a-IGZO exposed back-channel surface could introduce an acceptor-like surface state and cause charge trapping [10]. According to the XPS result, it suggested that a-IGZO thin films deposited with oxygen incorporation might show less oxygen adsorption in the ambience due to more oxygen content and less oxygen vacancies in the film. Therefore, a higher stability of V_{th} was obtained for sample III. The results implied that using IGZO film deposited with high oxygen flow rate as back-channel layer appeared to be as a barrier layer to improve the stability of a-IGZO TFTs.

The transfer curves for samples I, II, and III under NBS condition of V_{gs} = −20 V and V_{ds} = 0 V are shown in Fig. 5. Samples I and III exhibited fairly small negative V_{th} shifts of −0.05 and −0.01 V, with nearly no change in μ_{FE} and S, which were similar with the report [19]. Contrary to the case in a-Si:H TFTs [20], the hole trapping at either the gate insulator or at the channel layer/gate insulator interface can be ignored under NBS in a-IGZO TFTs due to the negligible holes in the n-type oxide semiconductor valence bands[19]. However, unlike samples I and III, sample II showed a positive shift of 1.54 V with a slight degradation of S and almost no change in μ_{FE}. These results indicated that the NBS-induced instability was dominated by the variation of oxygen vacancies at or near the channel layer/gate insulator interface. For sample II, sputtering at higher oxygen pressure could passivate oxygen vacancies and create accepter-like defects, e.g. metal vacancies, at or near the channel layer/gate insulator interface. These defects could easily transform to fix negative charges after trapping electrons [12] and cause an effect of screening the gate voltage. In this case, an additional voltage had to be applied at the gate terminal to form a channel after exciting the trapped electrons, thereby causing a

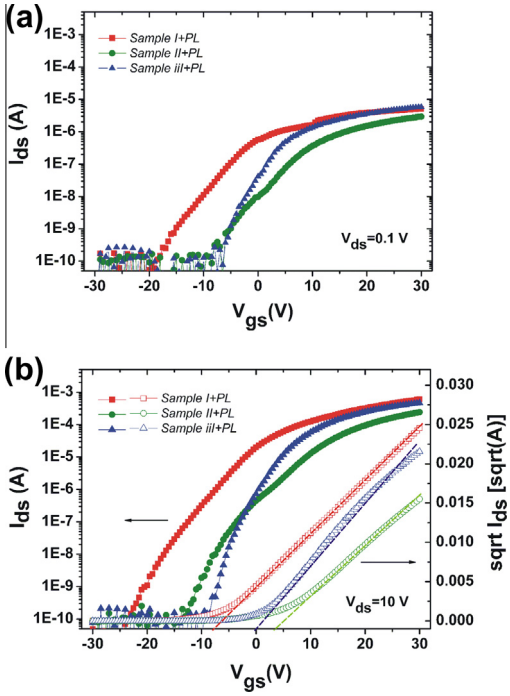

Fig. 6. Electrical characteristics of a-IGZO TFTs with sputtered SiN_x thin film as the passivation layer: samples I+PL, II+PL, and III+PL. Transfer curves (I_{ds}–V_{gs}) (a) at V_{ds} = 0.1 V (linear region) and (b) at 10 V (saturation region).

Table 2
Electrical characteristics of a-IGZO TFTs with passivation layers: samples I+PL, II+PL, and III+PL.

Samples	μ_{FE} (cm^2/Vs)	S (V/dec)	V_{th} (V)	$R_{on/off}$
I+PL	6.37	4.53	−7.38	8.70×10^6
II+PL	4.17	4.28	4.12	7.00×10^6
III+PL	5.19	2.40	0.29	2.86×10^7

positive shift in V_{th}. The specific mechanism will be elucidated by further experiments.

3.4. Effect of passivation layer

As oxide semiconductor and source/drain electrodes were deposited by sputtering, a 30 nm-thick SiN_x thin film was also deposited by RF sputtering to serve as a passivation layer, achieving all-sputtered a-IGZO TFTs at room temperature. Here, three types of TFTs: samples I+PL, II+PL, and III+PL, were fabricated to study the influence of sputtered SiN_x passivation layer on the device performance.

Fig. 6 shows the electrical characteristics of three types of a-IGZO TFTs with passivation layer. Compared with non-passivation TFTs, transfer characteristics of all devices with passivation layers exhibited a negative shift. Electrical parameters of the three types of a-IGZO TFTs with passivation layer are listed in Table 2. Not only the degradation of S but also a lower threshold voltage and a higher mobility were obtained for the passivated TFTs, which could be attributed to the effect of the deposition process of passivation layer [12]. In the deposition process of sputtered SiN_x passivation layer, more defects, such as oxygen vacancies induced by the broken metal–oxygen bond, were generated in the channel layer by the ion bombardment. Therefore, more free electrons were produced in channel layer, which resulted in a higher mobility. In addition, more interface traps could be filled by the increased free electrons, causing a better interface and a lower V_{th}. On the other hand, the increased defects in the channel layer for passivated TFTs, led to a higher value of S than that of non-passivated ones.

Besides, among the three types of TFTs, sample III+PL showed the least S value. Generally, S value reflects not only the bulk trap density of the channel layer, but also the interface trap density at or near the interface between channel layer and gate insulator [1]. Since samples I+PL and III+PL had similar channel layer-gate insulator interface states, the critical change in the S value for sample I+PL was ascribed to more defect generation in the back channel than that of sample III+PL. Therefore, it can be concluded that using oxygen-rich thin film as back channel layer could reduce the plasma damage to channel layer during the passivation process. The one reason may be that the defects such as oxygen vacancies can be passivated by oxygen atoms in the oxygen-rich IGZO film, which played the same role as that in the post-treatment on the back channel, such as the N_2O treatment [21] or the oxygen supply during the passivation process [12].

Figs. 7 and 8 exhibit the variation of transfer curves for samples I+PL, II+PL, and III+PL under PBS (V_{gs} = 20 V and V_{ds} = 0 V) and NBS (V_{gs} = −20 V and V_{ds} = 0 V) tests, respectively. It was observed that all the devices showed a smaller threshold voltage shift than the devices without passivation layer, which was consistent with the previous report [10]. For PBS, the ΔV_{th} obtained at 3.0 ks for samples I+PL, II+PL, and III+PL were 0.33, 0.46, and 0.01 V, respectively. For NBS, ΔV_{th} obtained at 3.0 ks for samples I+PL, II+PL and III+PL were −0.56, −0.77 and −0.54 V, respectively. The results indicated that the improvement in the stability of a-IGZO TFTs was obtained by sputtered SiN_x passivation layer.

The little V_{th} shift of passivated TFT was supposed to be related to the following reasons. One was that the sputtered SiN_x passivation layer could isolate the surface of a-IGZO thin film to the ambience, thus the absorption/desorption of oxygen and/or moisture on the a-IGZO can be prevented. The other one may be related to the interface states between channel layer and passivation layer,

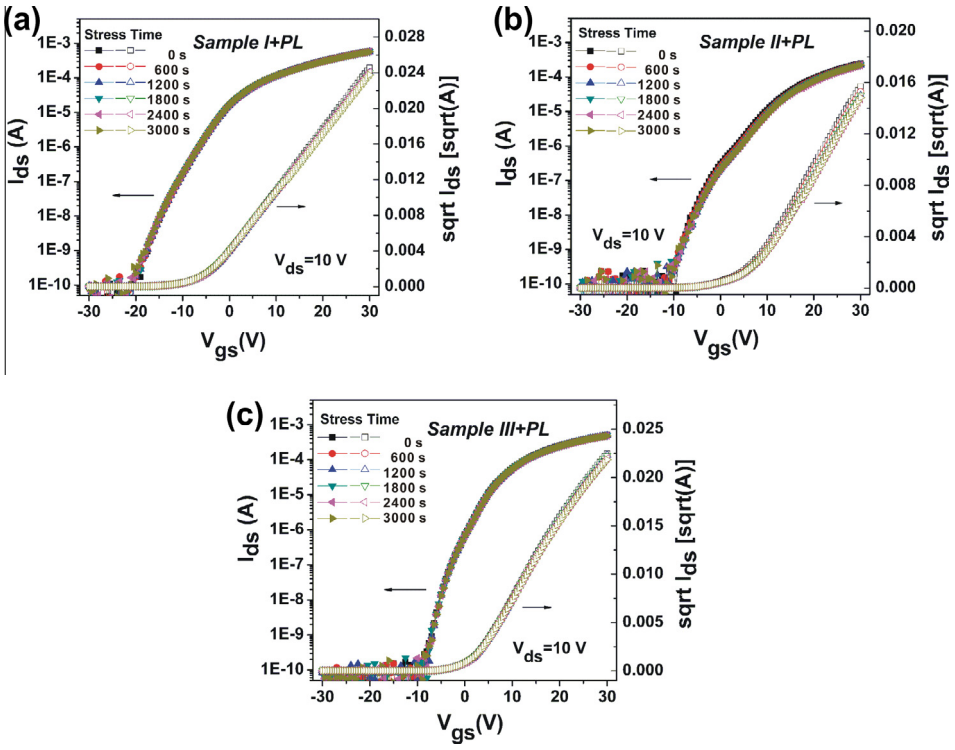

Fig. 7. Stress time dependence of transfer curve shifts in three different TFTs with passivation layer under positive gate bias stress (V_{gs} = 20 V, V_{ds} = 0 V): samples (a) I+PL, (b) II+PL, and (c) III+PL.

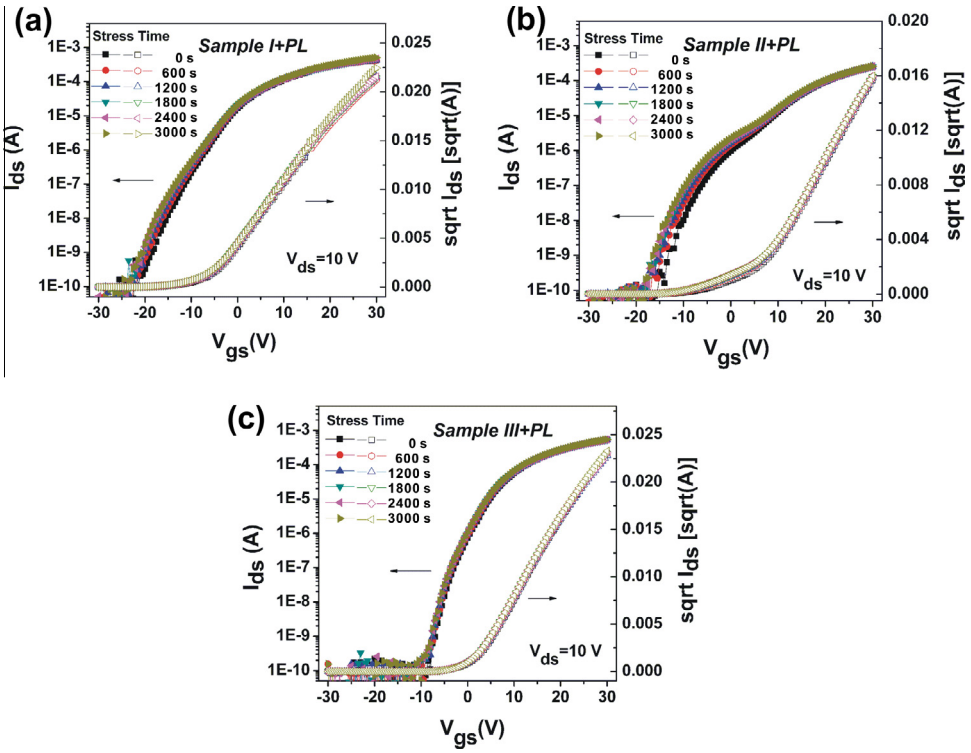

Fig. 8. Stress time dependence of transfer curve shifts in three different TFTs with passivation layer under negative gate bias stress (V_{gs} = −20 V, V_{ds} = 0 V): samples (a) I+PL, (b) II+PL, and (c) III+PL.

where there existed traps induced by ion bombardment [12]. When the PBS test was applied, the channel layer/passivation layer interface was supposed to be positive charges trapped at the interface when electrons were accumulated in the front a-IGZO/insulator interface under the PBS, resulting in some free electron accumulated near or in the back channel. The effect compensated the electrons trapped in the a-IGZO/insulator interface or injected to the gate dielectric. Therefore, the devices with passivation layer had a smaller V_{th} shift under the PBS. While the NBS test was applied, the electrons were trapped at the channel layer/passivation layer interface, resulting in an additional current pathway on the back channel surface and less gate voltage to turn on the device. Thus, it can be deduced that both the channel layer/gate insulator and the channel layer/passivation layer interfaces play important roles in the device stability of passivated TFTs. Since sample III+PL showed the least traps at the channel layer/gate insulator and the channel layer/passivation layer interfaces, as mentioned above, the best stability could be obtained for sample III+PL among the three types of a-IGZO TFTs.

4. Conclusion

In conclusion, it was found that the stability of a-IGZO TFTs was improved by double stacked channel layer. For positive and negative bias stress test, the smallest shift value of V_{th} for the TFT with stacked channel layer was achieved (3.08 V for PBS and −0.01 V for NBS). Moreover, with the sputtered SiN_x thin film served as the passivation layer, the stability of a-IGZO TFTs was improved effectively. For positive and negative bias stress test, the TFT with stacked channel layer still showed the smallest V_{th} shift (0.01 V for PBS, −0.54 V for NBS). The improvement in the device characteristics was attributed to lower trap density at channel layer/gate insulator interface by using a-IGZO film deposited without oxygen incorporation, and the improvement of back channel layer by using a-IGZO film deposited with high oxygen incorporation which may behave as a barrier layer to reduce oxygen adsorption induced by ambient effect and/or damage caused by ion bombardment. However, it should be noted that further work to optimize the passivation layer deposition layer process is necessary because inadvertent damage to the TFT due to the insufficiently optimized passivation layer deposition layer process has been observed in our samples. Anyway the experimental results exhibit that the proper control of the front channel and back channel plays an important role in improving the stability of a-IGZO TFTs.

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References

[1] Kamiya T, Nomura K, Hosono H. Present status of amorphous InGaZnO thin film transistors. Sci Technol Adv Mater 2010;11:044305.
[2] Hsieh HH, Lu HH, Ting HC, Chuang CS, Chen CY, Lin Y. Development of IGZO TFTs and their applications to next generation flat panel displays. J Inf Display 2010;11:160.
[3] Jeong JK. Status and perspectives of metal oxide thin film transistors for active matrix flexible displays. Semicond Sci Technol 2010;26:034008.
[4] Conley JF. Instabilities in amorphous oxide semiconductor thin film transistors. IEEE T Device Mat Re 2010;4:460.
[5] Yao JK, Xu NS, Deng SZ, Chen J, She JC, Shieh HPD, et al. Electrical and photosensitive characteristics of a-IGZO TFTs related to oxygen vacancy. IEEE Trans Elec Dev 2011;58:1121.
[6] Kim S, Jeon YW, Kim Y, Kong D, Jung HK, Bae MK, et al. Impact of oxygen flow rate on the instability under positive bias stresses in DC sputtered amorphous InGaZnO thin film transistors. IEEE Electron Dev Lett 2012;33:62.
[7] Kang D, Lim H, Kim C, Song I, Park J, Park Y, et al. Amorphous gallium indium zinc oxide thin film transistors: sensitive to oxygen molecules. Appl Phys Lett 2007;90:192101.

[8] Jeong JK, Yang HW, Jeong JH, Mo YG, Kim HD. Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. Appl Phys Lett 2008;93:123508.
[9] Ide K, Kikuchi Y, Nomuar K, Kimura M, Kamiya T, Hosono H. Effects of excess oxygen on operation characteristics of amorphous InGaZnO thin film transistors. Appl Phys Lett 2011;99:093507.
[10] Hong D, Wager JF. Passivation of zinc-tin-oxide thin film transistors. J Vac Sci Technol B 2005;23:L25.
[11] Cho DH, Yang S, Shin J, Ryu MK, Cheong WS, Park SHK, et al. Post annealing and passivations of transparent bottom gate IGZO thin film transistors. Proc SID 2008;2008:1243.
[12] Park SHK, Ryu MK, Yoon SM, Yang S, Hwang CS, Jeon JH. Device reliability under electrical stress and photo response of oxide TFTs. J Soc Inf Display 2010;18:779.
[13] Kim GH, Jeong WH, Kim HJ. Electrical characteristics of solution-processed InGaZnO thin film transistors depending on Ga concentration. Phys Status Solidi A 2010;207:1677.
[14] Lee KW, Kim KM, Heo KY, Park SK, Lee SK, Kim HJ. Effects of UV light and carbon nanotube dopant on solution-based indium gallium zinc oxide thin-film transistors. Curr Appl Phys 2011;11:280.
[15] Fung TC, Chuang CS, Nomuar K, Shieh HPD, Hosono H, Kanicki J. Photofield-effect in amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors. J Inf Display 2008;9:21.
[16] Kagan CR, Andry P. Thin-film transistors. New York: Marcel Dekker Inc.; 2003. p. 87.
[17] Jung C, Kim D, Kang YK, Yoon DH. Effect of heat treatment on electrical properties of amorphous oxide semiconductor InGaZnO film as a function of oxygen flow rate. Jpn J Appl Phys 2009;48:08HK02.
[18] Cho EN, Kang JH, Kim CE, Moon P, Yun I. Analysis of bias stress instability in amorphous InGaZnO thin film transistors. IEEE T Device Mat Re 2011;11:112.
[19] Chen TC, Chang TC, Hsieh TY, Lu WS, Jian FY, Tsai CT, et al. Investigating the degradation behavior caused by charge trapping effect under DC and AC gate-bias stress for InGaZnO thin film transistor. Appl Phys Lett 2011;99:022104.
[20] Zhou D, Wang M, Zhang S. Degradation of amorphous silicon thin film transistors under negative gate bias stress. IEEE Trans Electron Dev 2011;58:3422.
[21] Tsai CT, Chang TC, Chen SC, Lo I, Tsao SW, Hung MC, et al. Influence of positive bias stress on N_2O plasma improved InGaZnO thin film transistor. Appl. Phys. Lett. 2010;96:242105.