Investigation and Comparison of the GaN-Based Light-Emitting Diodes Grown on High Aspect Ratio Nano-Cone and General Micro-Cone Patterned Sapphire Substrate

Jhih-Kai Huang, Da-Wei Lin, Min-Hsiung Shih, *Member, IEEE, Member*, Kang-Yuan Lee, Jyun-Rong Chen, Hung-Weng Huang, Shou-Yi Kuo, Chung-Hsiang Lin, Po-Tsung Lee, *Member, IEEE*, Gou-Chung Chi, and Hao-Chung Kuo, *Senior Member, IEEE*

***Abstract*—In this paper, we demonstrated the high performance GaN-based LEDs by using a high aspect ratio cone-shape nano-patterned sapphire substrate (HAR-NPSS). We utilized nano-imprint lithography (NIL) and dry-etching system to fabricate a high depth HAR-NPSS. The micro-scale patterned sapphire substrate (PSS) was also used for comparison. A great enhancement of light output was observed when GaN-based LEDs were grown on a HAR-NPSS or a PSS. The light output power of LEDs with a HAR-NPSS and LEDs with a PSS were enhanced of 49 and 38% compared to LEDs with a unpatterned sapphire substrate. The high output power of the LED with a HAR-NPSS indicated that the technology of NAR-NPSS not only can improve the crystalline quality of GaN-based LEDs but also a promising development to a NPSS.**

***Index Terms*—GaN, light-emitting diodes (LEDs), nano-imprint lithography (NIL), nano-patterned sapphire substrate (NPSS).**

I. Introduction

THE GaN-based LEDs have been widely used for light source, backlight in liquid crystal displays, and solid state lighting [1], [2] and became popular in the study. GaN is a very hard and mechanically stable material. However, there is actually few suitable substrate can be used to grow GaN because of the specific hexagonal lattice. Considering the high quality, high throughput, low cost and mass production for GaN-based LEDs, sapphire substrates is a well known solution. Although sapphire substrate is a very common substrate to GaN epitaxy, the lattice mismatch between GaN and sapphire still limited the light output and resulted in a low internal quantum efficiency (IQE) and a poor external quantum effciency (EQE). The low IQE is directly related to the threading dislocations (TDs)in the GaN film. In order to decrease the TDs density and improve the crystalline quality, a micro-scale patterned sapphire substrate (PSS) is recommended to solve the problem [3], [4]. A PSS served as a GaN template and the pattern could be scattering centers for the guided light to improve GaN crystalline quality and the light extraction efficiency. Recently, nano-scale patterned sapphire substrate (NPSS) are investigated as a new substrate to GaN-based LEDs. It was proposed that NPSS can be a high potential template and provide a new type substrate for GaN epitaxy [5]–[12]. The use of NPSS resulted in TDs density reduction [9]–[11] and reduction in screw dislocation density fraction [12] in GaN template. These reductions in both dislocation density and screw dislocation density from the use of NPSS resulted in improved IQE in InGaN QW LEDs attributed to the reduced non-radiative recombination rate. In addition to the dislocation density reduction, several methods had been pursued for achieving improved IQE in InGaN-based QW LEDs by suppressing the charge separation in active regions [13]–[18]. The charge separation suppression had been pursued by using non/semi-polar QWs [13]–[15], and polar QWs with large overlap designs [16]–[18]. The surface patterning based on photonic crystals [19], [20] and self-assembled microlens arrays [21], [22] had been reported for achieving large increase in light extraction efficiency (LEE) in III-Nitride LEDs. Recently, the effect of pattern density in PSS had been also shown to affect the light extraction in GaN-based LEDs [23]. Although the technology of NPSS has been reported to play an important role for improving LEDs efficiency, there are few reports on the relation between the efficiency and the NPSS geometry. Due to the hardness of sapphire, the etching depth is usually a bottleneck to modify the profile for the dry-etching methods or wet-etching methods for the NPSS patterns. The pattern profile is also a key issue to the GaN quality when growing GaN layers on a patterned substrate. In this study, the high aspect ratio cone-type nano-patterned sapphire substrate (HAR-NPSS) was used to decrease the defect density and improve the quality of GaN LEDs.

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J.-K. Huang, D.-W. Lin, J.-R. Chen, H.-W. Huang, P.-T. Lee, G.-C. Chi, and H.-C. Kuo are with the Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: hckuo@faculty.nctu.edu.tw).

M.-H. Shih is with the Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan, and also with the Research Center for Applied Sciences (RCAS), Academia Sinica, Taiwan (e-mail: mhshih@gate.sinica.edu.tw).

S.-Y. Kuo is with the Department of Electronic Engineering, Chang Gung University, TaoYuan 333, Taiwan.

K.-Y. Lee and C.-H. Lin are with the Luxtaltek Corporation, Miaoli 350, Taiwan.

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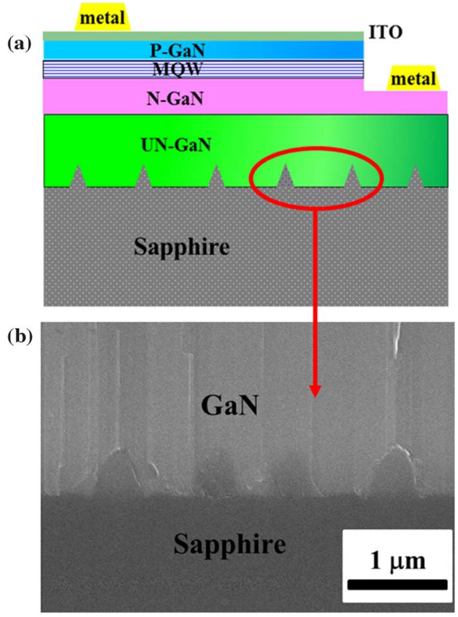

Fig. 1. (a) Schematic diagram of LED structure with a HAR-NPSS. (b) Cross-view SEM image of GaN/HAR-NPSS interface.

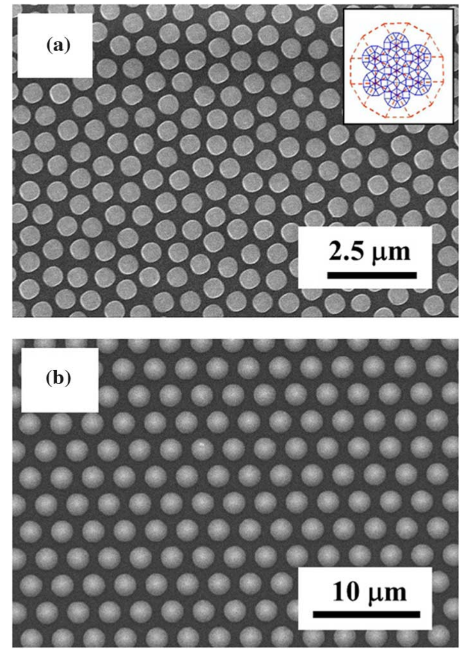

Fig. 2. (a) Top-view SEM image of a HAR-NPSS with a 12-fold PQC pattern. (b) Top-view SEM image of a PSS.

A nano-imprint lithography (NIL), which is a high throughput, rapid and repeating process for mass production, was utilized to fabricate a HAR-NPSS with a 12-fold a photonic quasi-crystal (PQC) pattern [24]–[27].

II. Experiments

Fig. 1(a) shows the schematic diagram of the GaN-based LEDs with a HAR-NPSS and Fig. 1(b) is the SEM cross-view image around an interface of the GaN film and HAR-NPSS.

In order to fabricate a high depth HAR-NPSS, the NIL was processed with a deep imprint-mold with a high depth of 700 nm. The following is the detail of the HAR-NPSS process flow by using NIL and dry-etching system. First, an imprint-resist was coated onto sapphire substrate surface. Then, a deep patterned mold was placed onto sapphire substrate with an imprint-resist film to transfer pattern by applying a high pressure at a transition temperature. Second, the sapphire substrate and the mold were cooled down to room temperature to release the mold from the substrate. The thickness of the imprint-resist after NIL process is approximately 800 nm. Finally, we used an inductively coupled plasma reactive ion etching (ICP-RIE) with the chemical mixture $BCl_3/Cl_2/Ar$ of 50/20/5 sccm to transfer the pattern onto sapphire substrate by a RF power of 450 W and an ICP power of 200 W. The fabricated HAR-NPSS samples were patterned as a 12-fold PQC with a 450 nm diameter, a 250 nm spacing distance and a 530 nm high etching depth. The aspect ratio of HAR-NPSS is as high as 1.17 and the profile of HAR-NPSS is cone-like type which is similar to the profile of PSS. A sample with the PSS pattern and a flat sapphire substrate were also prepared as the references in the experience. The PSS was fabricated by the photo-lithography process. The photo-resist AZ-5214-E was used as the etching mask and apply the same ICP-RIE system to transfer pattern onto the sapphire. The PSS pattern is with a diameter of 2 μm, a spacing distance of 1 μm and an etching depth of 1.3 μm. The aspect ratio of PSS is 0.65. Fig. 2 shows the top-view images of the HAR-NPSS with a 12-fold PQC pattern and PSS.

All LED structure were fabricated by the metal organic chemical vapor deposition (MOCVD) system. The LED structure was described by following. The LED consists of a 50 nm-thick GaN nucleation layer grown at 500 °C, a 3 μm-thick un-doped GaN (UN-GaN) buffer layer grown at 1050 °C, a 3 μm-thick Si-doped GaN (N-GaN) layer grown at 1050 °C, an unintentionally doped InGaN/GaN multiple quantum well (MQW) active region grown at 770 °C, a 50 nm-thick Mg-doped p-AlGaN electron blocking layer grown at 1050°C, and a 120 nm-thick Mg-doped p-GaN contact layer grown at 1050 °C. The MQW active region consists of 14 periods of 3 nm/10 nm thick $In_{0.18}Ga_{0.82}N$/GaN quantum well layers and barrier layers.

The LED devices were fabricated by standard LED chip processes with a chip size of $575 \times 250\ \mu m^2$. A indium-tin-oxide (ITO) thin film with a thickness of 240 nm is deposited onto p-GaN surface. The n-contact and p-contact metal are Cr/Pt/Au layers with thickness of 30/50/1400 nm.

III. Results and Discussion

The transmission electron microscopy (TEM) images were employed to investigate the crystalline quality of GaN layers grown on a flat sapphire substrate, a PSS and a HAR-NPSS. Fig. 3(a)–(c) show the TEM images of GaN-Based LEDs grown on a flat sapphire, a PSS and a HAR-NPSS, respectively. It can be seen that the TDs density of GaN epilayer were drastically reduced by using PSS and HAR-NPSS (Fig. 3(b) and (c)) as compared with GaN epilayer grown on a flat sapphire substrate [Fig. 3(a)]. The reduction of TDs density for GaN epilayer grown on PSS can be attributed to epitaxial lateral overgrowth (ELOG) mechanism, which results in the dislocation bending to lateral direction and preventing them reaching the MQWs to

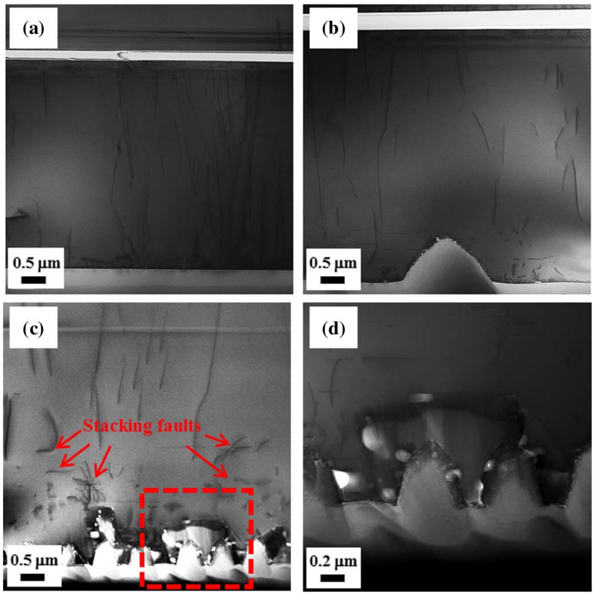

Fig. 3. (a) TEM image of GaN-based LEDs grown on a flat sapphire substrate. (b) TEM image of GaN-based LEDs grown on a PSS. (c) TEM image of GaN-based LEDs grown on a HAR-NPSS. (d) GaN/HAR-NPSS interface corresponding to the red dash-line area.

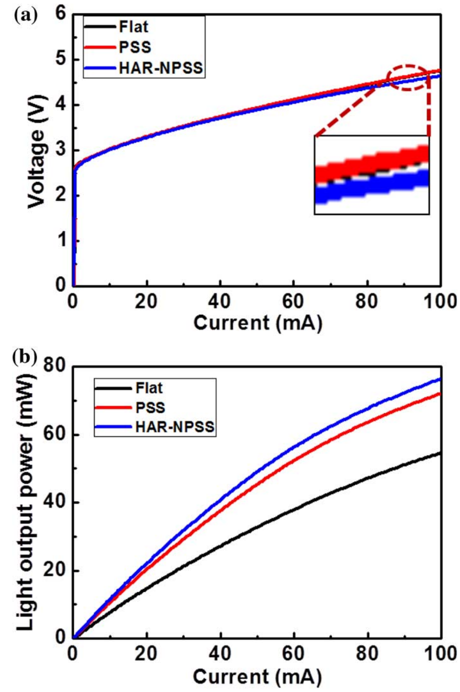

Fig. 4. (a) Current–voltage (*I*–*V*) characteristics of conventional LEDs with a flat sapphire substrate, a PSS and a HAR-NPSS. (b) Intensity–current (*L*–*I*) characteristics of conventional LEDs with a flat sapphire substrate, a PSS and a HAR-NPSS.

degrade light output efficiency. Moreover, Fig. 3(d) shows the magnified figure of the red dashed line region in Fig. 3(c). From Fig. 3(d), one can see that a number of stacking faults occurred above the nano-lens patterns, these stacking faults were believed to be a channel which could block the propagation of TDs [28]. As a result, the TDs were rarely observed above the stacking faults; while they were dense underneath the stacking faults. The dislocation densities of LEDs grown on a HAR-NPSS, PSS, and flat sapphire substrate are estimated to 1.6×10^8, 2.2×10^8, and 1.1×10^9 cm^{-2}, respectively. One can find out that the dislocation densities of LEDs grown on a HAR-NPSS and PSS are greatly decreased as compared with LEDs grown on a flat sapphire substrate. In addition, the LEDs grown on a HAR-NPSS even has a slightly improvement than LEDs grown on a PSS.

Fig. 4 shows the characteristics of a typical current–voltage (*I*–*V*) and intensity–current (*L*–*I*) characteristics of conventional LEDs with a flat sapphire substrate, LEDs with a PSS and LEDs with a HAR-NPSS for transistor outline-can (TO-can) package. It is found that the measured forward voltages under a injection current of 20 mA at room temperature for conventional LEDs with a flat sapphire substrate, LEDs with a PSS and LEDs with a HAR-NPSS are 3.29, 3.3, 3.28 V, respectively. The voltages of LEDs with a flat sapphire substrate, LEDs with a PSS and LEDs with a HAR-NPSS are very close under a driving current of 20 mA. It indicates the good electrical propertisy of LEDs with a PSS and LEDs with a HAR-PSS. In addition, the I-V curves of LEDs devices with a flat sapphire substrate, a PSS and a HAR-NPSS are very similar even under a high injection current. There is no influence to *I*–*V* characteristics of device when we used a PSS or a HAR-PSS. At a an injection current of 20 mA and peak wavelength of 460 nm for TO-can package, the light output powers of conventional LEDs with a flat sapphire substrate, LEDs with a PSS and LEDs with a HAR-NPSS are measured of 14.7, 20.3 and 22 mW by a integrating sphere measurement system. Hence, the enhancement percentages of LEDs with a PSS and LEDs with a HAR-NPSS are 38 and 49% which are compared to conventional LEDs with a flat sapphire. The optical enhancements are attributed to the improvement of GaN crystal quality by PSS and HAR-NPSS, and the pattern geometry of PSS or HAR-PSS is not critical factor to reduce the defects in the GaN layers. The calculated value of wall plug efficiency (WPE) are 22.3, 30.7 and 33.5% for conventional LEDs with a flat sapphire substrate, LEDs with a PSS and LEDs with a HAR-NPSS. The enhancement of the WPE of LEDs with a HAR-NPSS can be attributed to IQE and LEE of the device. The IQE of LEDs grown on a HAR-NPSS and PSS are similar due to they have almost the same dislocation densities. On the other hand, the LED with a HAR-NPSS has a higher output power than the LED with a NPSS, which is attributed to the light scattering effect by nano-scale HAR-NPSS.

As compared to the previous work [29], the aspect ratios of the structure with NPSS and embedded SiO_2 nanorod array and the structure with HAR-NPSS in this paper are indeed much different. The aspect ratio of the former structure is approximately 0.4, while it of the current structure is approximately 1.12. However, we should note that the 48% of light output power enhancement is contributed from both effects of the NPSS and embedded SiO_2 nanorod array. For the LED only with the NPSS structure, the light output power enhancement is only 35% [29]. In addition, the chip sizes between these two researches are different. The LEDs with the NPSS and embedded SiO_2 nanorod array are 300×300 μm^2, while the LEDs with the HAR-NPSS are 575×250 μm^2. In addition, the advantages of using the HAR-NPSS as the epitaxial substrate is that it can further improve the crystalline quality and LEE without the complicated process of NPSS, embedded SiO_2 nanorod array, and regrowth technique. The light output power enhancement of LEDs with HAR-NPSS can achieve the same level (49%) as compared with the previous work (48%). However, the layer thickness of un-doped GaN should be increased, so the GaN epi-layer can effectively coalesce. But we consider that the layer thickness increase is acceptable because the thicker epi-layer is also needed as using the commercial micro-scale PSS.

IV. Conclusion

In short, GaN-based LEDs with a high aspect ratio cone-shape nano-patterned sapphire substrate (HAR-NPSS) are demonstrated with the nano-imprint lithography (NIL). The light output power of the GaN-based LEDs grown on a HAR-NPSS showed better performance as compared to LEDs with a PSS and a unpatterned sapphire substrate. The high output power of the LED with a HAR-NPSS indicated that using NAR-NPSS as epitaxial substrate to grow LED structure can not only improve the crystalline quality of GaN-based LEDs but also enhance the light extraction efficiency. This work verified that the HAR-NPSS has a promising potential to improve performances of GaN-based LEDs. It also proved that the NIL system is advantaged to fabricate a HAR-NPSS for mass production.

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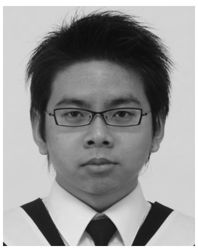


Jhih-Kai Huang received the B.S. degree in Department of Electrical Engineering, from National Central University and the M.S. degree in electro-optical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2007 and 2009, respectively, and is currently working toward the Ph.D. degree in the Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan.

His research areas include GaN-based device fabrication and nano-imprint technology and nano-structure process for GaN-based light-emitting diodes.

Da-Wei Lin received the B.S. and the M.S. degrees in Department of Photonics from National Chiao Tung University, Hsinchu, Taiwan, in 2009 and 2010, respectively, and is currently working toward the Ph.D. degree in the Department of Photonics.

His research areas include the epitaxy of III-V compound semiconductor materials by MOCVD and analysis for GaN-based light-emitting diodes.

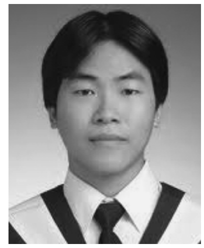
Min-Hsiung Shih (A'10–M'12) received B.S degree in physics from the National Cheng Kung University, Tainan, Taiwan, in 1995, the M.S. degree in physics from the National Tsing Hua University (NTHU), Taiwan in 1997, and the Ph.D. degree in electrical engineering/electrophysics from the University of Southern California (USC), Los Angeles, USA, in 2006.

He is currently an Associate Research Fellow in the Research Center for Applied Sciences (RCAS), Academia Sinica, Taiwan, and an Adjunct Associate Professor in Department of Photonics, National National Chiao Tung University (NCTU), Taiwan. His research interests include integrated photonic circuits, photonic crystals, GaN-based lasers, surface plasmonics, and cavity quantum electrodynamics. He had authored more than 80 journal and conference publications.

Prof. Shih is a member of the Optical Society of America (OSA).

Kang-Yuan Lee received the B.S. degree in physics from the National Sun Yat-sen University, Kaohsiung, Taiwan, in 1996, and the M.S. and Ph.D degrees in electro-optical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1998 and 2005, respectively.

From 2000 to 2001, he was an Engineer with the Photo Lithography Division in TSMC. From 2006 to 2008, he was the R&D section Manager with Asia Optical Corporation. He is currently working in the Luxtaltek Corporation, Chunan, Taiwan. His research interests include optical measurement, GaN-based light-emitting devices and nano-structure fabrication.



Jyun-Rong Chen was born in Taichung, Taiwan, on October 23, 1980. He received the B.S. degree in physics from the National Changhua University of Education (NCUE), Changhua, Taiwan, in 2004, and the M.S. degree in optoelectronics from the Institute of Photonics, NCUE, in 2006, and is currently working toward the Ph.D. degree at the Department of Photonics and the Institute of Electro-Optical Engineering, National Chiao Tung University (NCTU), Hsinchu, Taiwan.

In 2006, he was with the Semiconductor Laser Technology Laboratory, NCTU, where he was engaged in research on III-V semiconductor materials for LEDs and semiconductor lasers. His current research interests include III-nitride semiconductor lasers, epitaxial growth of III-nitride materials, and numerical simulation of III-V optoelectronic devices.

Hung-Weng Huang, photograph and biography not available at time of publication.

Shou-Yi Kuo was born in Taiwan, R.O.C. He received the B.S. degree in Electrical and Control Engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1995, and the M.S. and Ph.D. degrees in Electro-Optical Engineering from NCTU, in 1997 and 2002, respectively.

After he received his Ph.D. degree, he joined Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu Taiwan, as an associate researcher since January 2003. His main research interests and working experiences are focused on fabrication and characterizing of III-V and II-V wide-bandgap semiconductors, including GaN, ZnO, InN and dilute nitrides. He has been authored and co-authored more than 35 international Journals and 2 patents related to III-V compound semiconductor devices technology

Chung-Hsiang Lin received the B.S. and M.S. degrees in physics from National Taiwan University, Taipei, Taiwan. He also received the M.S. degree in electrical and computer engineering and the Ph.D. degree in physics from Polytechnic Institute of New York University, New York, USA.

He is the President of New Business Unit of Luxtaltek Corporation, Miaoli, Taiwan, and serves as an adjunct professor at the Institute of Electro-Optical Engineering, National Chiao Tung University (NCTU), Taipei, Taiwan. He has over 10 years of experience in the LED industry, specifically photonic crystal modeling and nano-fabrication on optoelectronic devices. He has over 30 professional publications related to photonic crystal devices. Prior to joining Luxtaltek, he held several research positions including a visiting scholar with Jet Propulsion Laboratory, Pasadena, CA, USA.

Po-Tsung Lee (M'06) received the B.S. degree from the Department of Physics, National Taiwan University (NTU), Taipei, Taiwan, in 1997 and the M.S. and Ph.D. degrees from the Department of Electrical Engineering-Electrophysics, University of Southern California (USC), Los Angeles, USA, in 1998 and 2003, respectively. During the Ph.D. study, she was engaged in photonic crystal microcavity lasers.

In 2003, she joined the Institute of Electro-Optical Engineering, National Chiao Tung University (NCTU), Hsinchu, Taiwan, as an Assistant Professor. In 2007, she became an Associate Professor in the Department of Photonics, NCTU. Her recent research interests are semiconductor photonic crystal active and passive devices and their applications, metallic nanostructures with localized surface plasmon resonances, and silicon-based solar cell technologies.

Prof. Lee was the recipient of the University of Southern California Women in Science and Engineering (WISE) Award in 2000–2001. She received the "Outstanding Young Electrical Engineer Award" from the Chinese Institute of Electrical Engineering in 2011.

Gou-Chung Chi was born on September 8, 1946, in Kaohsiung, Taiwan, R.O.C. He received the B.S. degree from the National Taiwan Normal University, Taiwan, in 1970, and the M.S. and Ph.D. degrees in solid state physics and materials, Department of Engineering and Applied Science from Yale University, new Haven CT, USA, in 1973 and 1976, respectively.

From 1977 to 1990, he was a Member of the Technical Staff at AT&T Bell Laboratories. From 1990 to 1994, he was a director of the division of optoelectronics materials and devices at Opto-Electronics & Systems Laboratories (OES) of Industrial Technology Research Institute (ITRI), Taiwan. From 1994, he had been a professor and director of Optical Sciences Center, National Central University. Since 2009, he is a professor of Department of Photonics, National Chiao Tung University, Hsinchu, Taiwan. His recent research interests are wide band gap semiconductor and devices (A1GaInP, InGaAsP, GaN-based materials), and microoptics integrated system.

Dr. Chi is also a member of Materials Research Society, Physical Society (Taiwan), Electrocins Devices and Materials Association (Taiwan).

Hao-Chung Kuo (S'98–M'99–SM'06) received the B.S. degree in physics from the National Taiwan University, Taipei, Taiwan, in 1990, the M.S. degree in electrical and computer engineering from Rutgers University, Camden, NJ, in 1995, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, Illinois, in 1999.

He has an extensive professional career both in research and industrial research institutions. From 1995 to 1997, he was a Research Consultant with Lucent Technologies, Bell Lab, Holmdel, NJ. From 1999 to 2001, he was an R&D Engineer with the Fiber-Optics Division, Agilent Technologies. From 2001 to 2002, he was the R&D Manager with LuxNet Corporation. Since September 2002, he has been a member of the faculty at the Institute of Electro-Optical Engineering, National Chiao Tung University (NCTU), Hsinchu, Taiwan. He has authored or coauthored over 60 publications. His current research interests include the epitaxy, design, fabrication, and measurement of high-speed InPand GaAs-based vertical-cavity surface-emitting lasers, as well as GaN-based lighting-emitting devices and nanostructures.

Dr. Kuo is a Fellow of OSA.