A Novel Forward AC/DC Converter With Input Current Shaping and Fast Output Voltage Regulation Via Reset Winding

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***Abstract*—This paper presents a novel simple forward ac/dc converter with harmonic current correction and fast output voltage regulation. In the proposed ac/dc converter, a transformer incorporating reset winding provides two main advantages. First, the bulk inductor used in the conventional boost-based power-factor-correction cell is omitted in the proposed converter, allowing significant volume and weight of magnetic material to be saved. Second, the voltage across the bulk capacitor can be held under 450 V by adjusting the transformer winding ratio, despite the converter operating in a wide range of input voltages (90∼265 V/ac). This new converter complies with IEC 61000-3-2 under a load range of 200 W and has fast output voltage regulation.**

***Index Terms*—AC/DC converter, IEC 61000-3-2, input current shaper, power-factor correction (PFC).**

I. Introduction

In modern electronic products, including personal computers, computer peripherals, and test instruments, ac/dc converters have become the primary power supplies. The ac/dc converters use switching circuits to achieve high-power transfer efficiency and ac/dc converter controllers can be designed flexibly. Improving power quality considerations requires two things: achieving high power factor and low high-frequency harmonics. Many studies have examined the relevant issues and numerous topologies have been proposed. The proposed solutions of these studies can be classified into two groups: those designed such that the input line current is sinusoidal and those designed such that it is nonsinusoidal [1], [2]. The group of topologies with the sinusoidal line current almost achieves the requirement of unity power factor but requires a complex topology or control circuit [3], [4]. Thus, the sinusoidal line current topologies are more costly to implement. Fig. 1 shows the block diagram of the ac/dc converter with sinusoidal input line current.

The ac/dc converter with nonsinusoidal line current employs a simple topology, such as single-stage–single-switch, and costs less in practical applications [6]–[9]. Although the circuits [7]–[9] lack a unity power factor, they comply with IEC 61000-3-2 [4]. A family of such circuits was described in [1] and [2]. In this family a boost circuit accompanied by a dc/dc converter was introduced to form the so-called single-stage single-switch ac/dc converters. The family circuits have PFC function, as illustrated in Fig. 2. This concept successfully simplifies a conventional power-factor corrector by changing it from two stages to one stage. However, this concept employs a bulk inductor in the boost section, which occupies significant volume and weight.

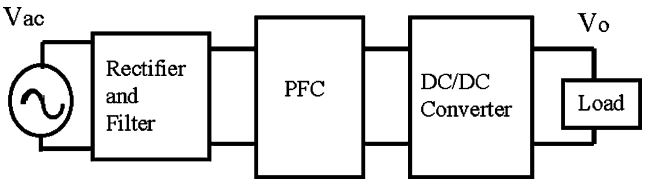

Fig. 1. Classical ac/dc converter with power-factor-correction (PFC) function.

This study proposes a new converter. Fig. 3 shows the topology of this new converter. The new converter satisfies the input harmonic current limits required by IEC 61000-3-2 and also has fast output response. A multiwinding transformer is employed in the proposed converter. The additional winding in the primary side is known as a reset winding in the forward-type converter. The reset winding of the transformer replaces the boost inductor presented in [6]–[9]. Moreover, the proposed converter design reduces the volume and weight of the magnetic material by almost half compared to existing boost-based single-stage PFC converters. Furthermore, the voltage across the bulk capacitor can be reduced to a reasonable value by adjusting the turns ratio of the windings N_1 and N_3. Therefore, this design can adapt to significant line voltage variation. The structure and operating principles of the proposed converter are presented in Sections II and III, and the practical experimental results are presented in Section V.

II. Proposed Circuit

Fig. 4 illustrates the proposed forward ac/dc converter with harmonic current elimination and fast output regulation speed. The proposed circuit is a single-switch single-stage ac/dc converter, which comprises a single switch S_1, an input filter C_1, bulk capacitor C_2, soft-switching inductor L_1, and a transformer with two primary windings N_1 and N_2. The reset winding N_1, inductor L_1, diodes D_1 and D_2, switch S_1, and bulk capacitor C_2 form a boost circuit. Moreover, the windings N_2 and N_3, a bulk capacitor C_2, switch S_1, diodes D_3 and D_4, inductor

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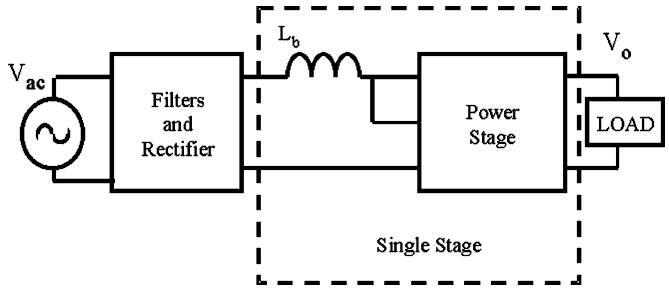


Fig. 2. Prior single-stage ac/dc PFC converter.

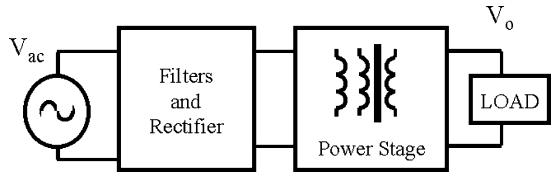


Fig. 3. Proposed single-stage ac/dc converter with ICS.

L_2, and output capacitor C_3 form a forward converter. The circuit connection of the reset winding N_1 differs from that in the classical forward converter. In the proposed design, the reset winding N_1 has two functions: to recycle the magnetic current generated by the winding N_2 and, also, to form a magnetic feedback for shaping line current.

A turns ratio of n_1/n_2 can determine not only the corner angle of the line current, but also the voltage across a bulk capacitor C_2. More detailed effects of turns ratio of n_1/n_2 are discussed in the following section. The inductor L_1 provides a soft-switching function for diodes D_1 and D_2. The current i_{N1} of L_1 gradually reducing to zero, as illustrated in Fig. 6, results in D_1 (in mode M_1) or D_2 (in mode M_2) turning off switching loss. Additionally, the inductance and volume of L_1 are significantly smaller than the primary windings N_1 or N_2 of the transformer.

The control circuit can be designed using either a simple fixed-frequency voltage-mode control or a conventional peak-current-mode control. The experimental results have demonstrated that even if a simple control method is used, the line current of the proposed ac/dc converter can comply with the standard IEC 61000-3-2 and the converter also can exhibit a fast dynamic response to the load.

III. Analysis of Circuit Operation

The operating principle of the proposed converter resembles the boost-based ac/dc single-switch single-stage isolated PFC power supply (S^4IP^2). The energy, stored in winding N_2 while switch S_1 turns on, is delivered to bulk capacitor C_2 via N_1 when switch S_1 turns off. The energy stored in winding N_2 comes from the magnetizing current when switch S_1 turns on. Furthermore, windings N_2 and N_3 are based on the same operating principle as the conventional forward converter. The current i_{N1} gives more magnetizing current to charge C_2 and causes V_{C2} to increase during (t_1, t_3), as illustrated in Fig. 5. Furthermore, a lower magnetizing current in i_{N1} causes V_{C2} to decrease during both periods (t_3, $T_l/2$) and (t_0, t_1) in Fig. 5. In this converter the capacitance of C_2 is designed to have the same value used in conventional ac/dc forward converter to maintain V_{C2} almost constant in a line cycle. Since the capacitance of C_2 is large, V_{C2} remains almost constant during the whole line period. Furthermore, the inductance of the regulation inductor L_2 in secondary side is set sufficiently large to keep L_2 working in the continuous conduction mode, and also to keep the duty cycle D almost constant during these two operation modes.

Fig. 5 shows that the proposed circuit has two operation modes M_1/M_4 and M_2/M_3 where M_4 and M_3 are mirror symmetric to M_1 and M_2. Fig. 6 illustrates the relative voltage and current waveforms in a single switching cycle in two operation modes.

A. Operation Modes M_1 or M_4 (During $t_0 \sim t_1$ or $t_3 \sim T_l/2$)

Within this mode, the converter acts as the conventional forward converter. However, the magnetizing current i_{Lm} generated by winding N_2 is transferred to winding N_1 and the capacitor C_2 is charged when S_1 is switched off. The current i_{N1} linearly reduces to zero when S_1 is turned off. V_{C2} denotes the voltage across the bulk capacitor C_2. If C_2 is sufficiently large, then V_{C2} can approximate a constant during a line cycle in the steady state, and can be calculated as follows:

$$V_{C2} \times \frac{n_3}{n_2} \times D = V_o. \tag{1}$$

At time t_1, the magnetic flux energized by winding N_2 releases to zero via winding N_1. Thus, the time bound of mode M_1 can be obtained as follows:

$$t_1 = \frac{1}{\omega} \times \sin^{-1}\left[\frac{V_{C2}}{V_m} - \frac{V_{C2} \times D \times n_2 \times L_{N_1}}{V_m \times (1-D) \times n_1 \times L_m}\right] \tag{2}$$

or

$$\omega t_1 = \sin^{-1}\left[\frac{V_o}{V_m} \times \frac{n_2}{n_3}\left(\frac{1}{D} - \frac{n_1}{(1-D)n_2}\right)\right] \tag{3}$$

where $V_m|\sin(\omega t)|$ is a rectified power source, $|V_{\rm ac}|$.

Fig. 7 illustrates the current loop in three intervals in mode M_1 or M_4. The winding currents and voltages are calculated as follows:

$$i_{N1} = \begin{cases} 0, & t_{0,M1} \sim t_{1,M1} \\ \frac{V_{C2} \times T_s D \times n_2 \times L_{N1}}{L_m \times n_1 \times (L_{N1}+L_1)} - \frac{V_{C2}-V_{in}}{L_{N1}+L_1} \times t, & t_{1,M1} \sim t_{2,M1} \end{cases} \tag{4}$$

$$i_{N2} = \begin{cases} i_{Lm} + i_{N3} \times \frac{n_3}{n_2}, & t_{0,M1} \sim t_{1,M1} \\ 0, & t_{1,M1} \sim t_{3,M1} \end{cases} \tag{5}$$

where $i_{Lm} = (V_{C2}/L_m) \times t$

$$i_{N3} = \begin{cases} \left(Io - \frac{\Delta Io}{2}\right) + \frac{V_{C2} \times \frac{n_3}{n_2} - V_o}{L_2} \times t, & t_{0,M1} \sim t_{1,M1} \\ 0, & t_{1,M1} \sim t_{3,M1} \end{cases} \tag{6}$$

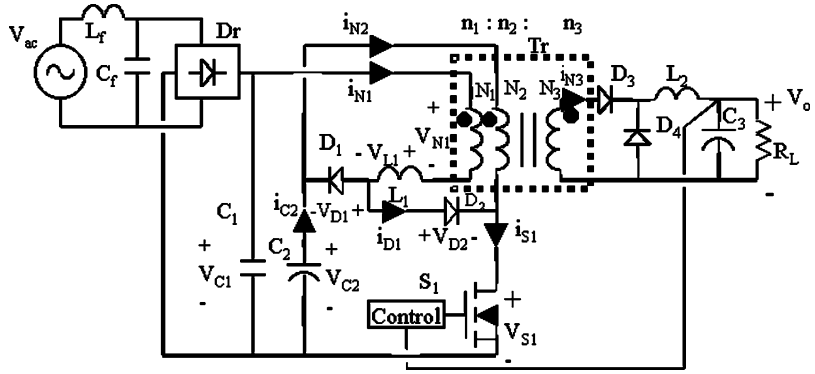


Fig. 4. Proposed forward ac/dc converter with ICS.

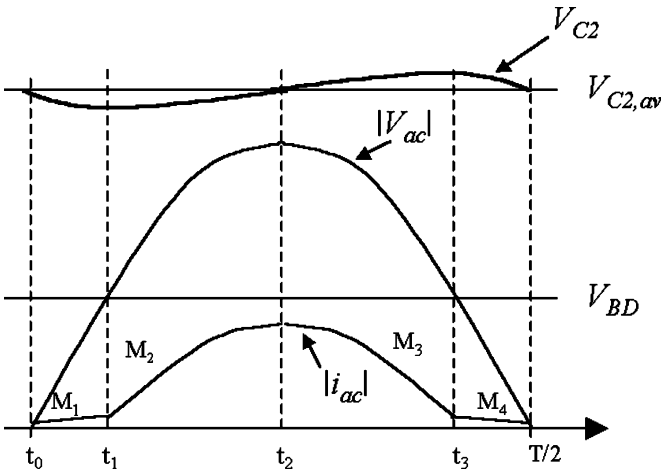


Fig. 5. Operation modes in the half of line cycle.

where $Io = \overline{V}_o/R_L$ and ΔIo is a load ripple current

$$V_{N1}=\begin{cases} V_{C2}\times\frac{n_1}{n_2}, & t_{0,M1}\sim t_{1,M1} \\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}, & t_{1,M1}\sim t_{2,M1} \\ 0, & t_{2,M1}\sim t_{3,M1} \end{cases} \quad (7)$$

$$V_{N2}=\begin{cases} V_{C2}, & t_{0,M1}\sim t_{1,M1} \\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}\times\frac{n_2}{n_1}, & t_{1,M1}\sim t_{2,M1} \\ 0, & t_{2,M1}\sim t_{3,M1} \end{cases} \quad (8)$$

$$V_{N3}=\begin{cases} V_{C2}\times\frac{n_3}{n_2}, & t_{0,M1}\sim t_{1,M1} \\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}\times\frac{n_3}{n_1}, & t_{1,M1}\sim t_{2,M1} \\ 0, & t_{2,M1}\sim t_{3,M1} \end{cases} \quad (9)$$

$$V_{L1}=\begin{cases} 0, & t_{0,M1}\sim t_{1,M1} \\ -(V_{C2}-V_{in})\times\frac{L_1}{L_{N1}+L_1}, & t_{1,M1}\sim t_{2,M1} \\ 0, & t_{2,M1}\sim t_{3,M1}. \end{cases} \quad (10)$$

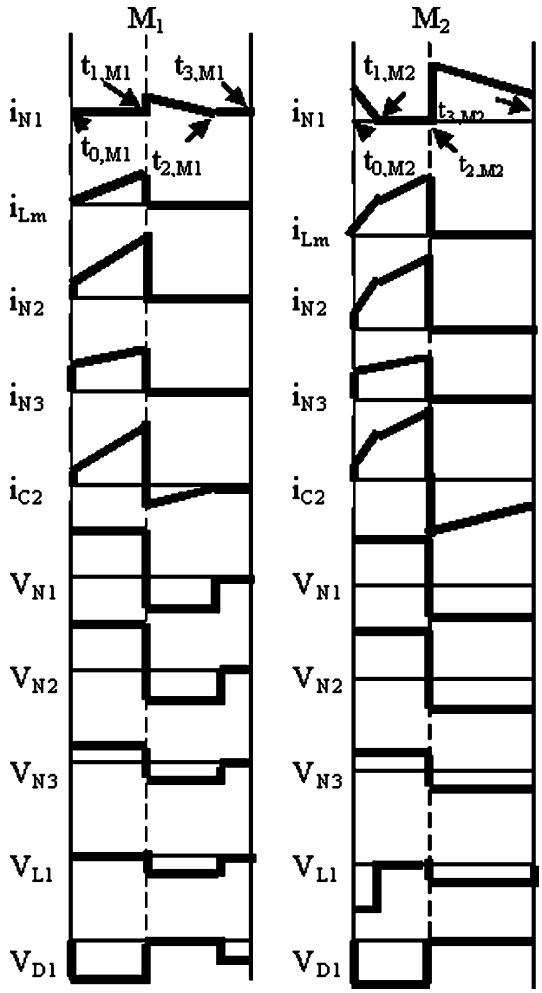


Fig. 6. Voltage and current waveforms in two modes.

B. Operation Modes M_2 or M_3 (During $t_1 \sim t_2$ or $t_2 \sim t_3$)

In this mode, $V_{\rm ac}$ is sufficiently large to turn D_2 on when S_1 is turned on. Current i_{N1} flows through the winding N_1, L_1, D_2, and S_1. Moreover, the capacitor C_2 supplies current i_{N2} which flows through winding N_2 and S_1. Therefore, the induced voltage across winding N_1 forces i_{N1} to linearly decrease to zero. Simultaneously, D_3 turns on and the transformer delivers the power to the output circuit. When S_1 turns off, the magnetizing current i_{Lm} induces i_{N1} and charges capacitor C_2 via winding N_1, L_1, and D_1. The induced current i_{N1} linearly decreases to $i_{N1}(t_{3,M2})$ at the end of the duty off period of switch S_1, where both $i_{N1}(t_{3,M2})$ and $i_{N1}(t_{3,M3})$ are nonzero in this mode. Fig. 8 shows the current loops for three operating stages in M_2/M_3.

The corresponding currents and voltages are obtained as follows:

$$i_{N1}=\begin{cases} i_{N1}(t_{0,M2})-\frac{V_{C2}\times\frac{n_1}{n_2}-V_{in}}{L_1}\times t, & t_{0,M2}\sim t_{1,M2} \\ i_{N1}(t_{2,M2})-\frac{V_{C2}-V_{in}}{L_{N1}+L_1}\times t, & t_{2,M2}\sim t_{3,M2}. \end{cases} \quad (11)$$

For L_1 is employed, i_{N1} will be continuous at the time $t_{3,M2}$; that is, $i_{N1}(t_{3,M2}) = i_{N1}(t_0, M2)$. Since proper L_2 is used,

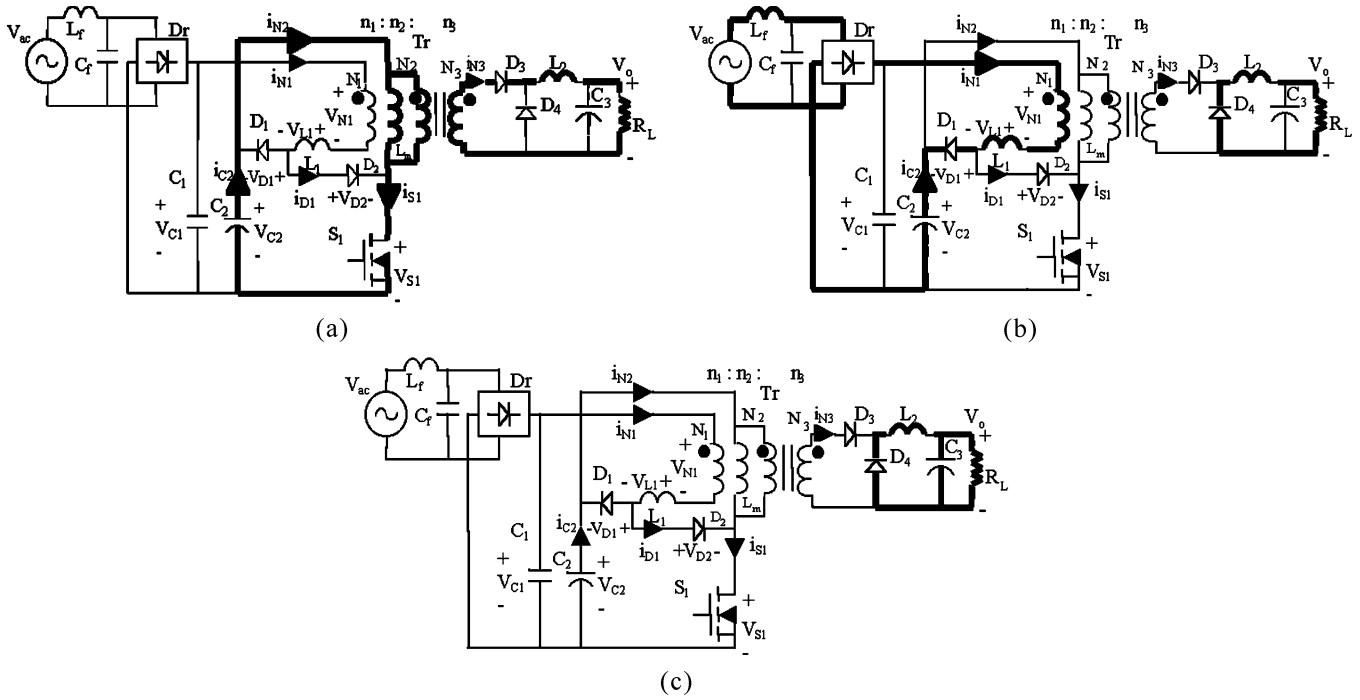


Fig. 7. Current loops when S_1 (a) turns on $(t_{0,M1} \leq t < t_{1,M1})$, (b) turns off $(t_{1,M1} \leq t < t_{2,M1})$, and (c) turns off $(t_{2,M1} \leq t < t_{3,M1})$ in mode M_1/M_4.

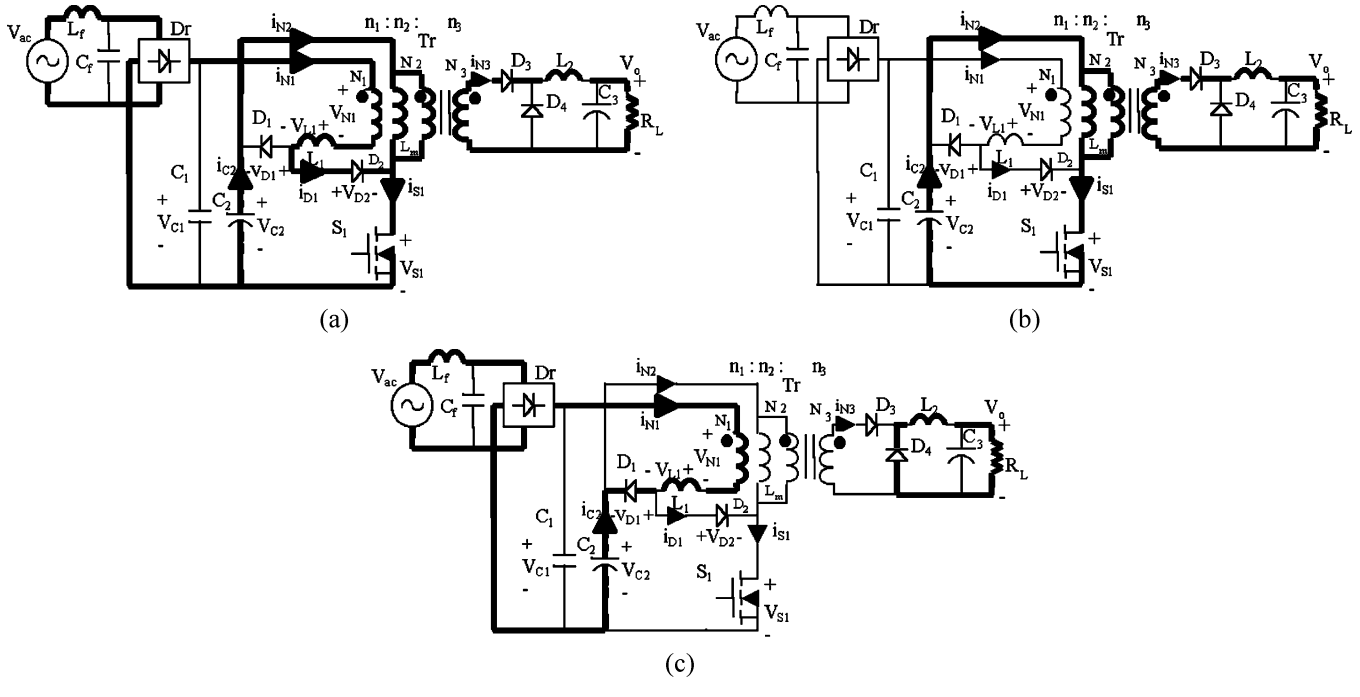


Fig. 8. Current loops when S_1 (a) turns on $(t_{0,M2} \leq t < t_{1,M2})$, (b) turns on $(t_{1,M2} \leq t < t_{2,M2})$, and (c) turns off $(t_{2,M2} \leq t < t_{3,M2})$ in mode M_2/M_3.

the current i_{N3} is almost constant. Considering the magnetic flux generated and applied between winding N_1 and N_2 we can yield

$$i_{N1}(t_{2,M2}) = \left(\frac{V_{C2} \times \frac{n_1}{n_2} - V_{in}}{L_1} \times \frac{n_1}{n_2} + \frac{V_{C2}}{L_m}\right) \times \frac{DT_s \times n_2 \times L_{N1}}{n_1 \times (L_{N1} + L_1)}. \quad (12)$$

Substituting (12) into (11) yields $i_{N1}(t_{3,M2})$, or $i_{N1}(t_{0,M2})$. For the other winding currents, the following is obtained:

$$i_{N2} = \begin{cases} i_{Lm} + i_{N3} \times \frac{n_3}{n_2}, & t_{0,M2} \sim t_{1,M2} \\ 0, & t_{1,M2} \sim t_{3,M2} \end{cases} \quad (13)$$

where

$$i_{Lm} = \frac{V_{C2} \times \frac{n_1}{n_2} - V_{in}}{L_1} \times \frac{n_1}{n_2} \times t + \frac{V_{C2}}{L_m} \times t \quad (14)$$

$$i_{N3}=\begin{cases}\left(Io-\frac{\Delta Io}{2}\right)+\frac{V_{C2}\times\frac{n_3}{n_2}-V_o}{L_2}\times t, & t_{0,M2}\sim t_{2,M2}\\ 0, & t_{2,M2}\sim t_{3,M2}\end{cases} \quad (15)$$

$$V_{N1}=\begin{cases}V_{C2}\times\frac{n_1}{n_2}, & t_{0,M2}\sim t_{2,M2}\\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}, & t_{2,M2}\sim t_{3,M2}\end{cases} \quad (16)$$

$$V_{N2}=\begin{cases}V_{C2}, & t_{0,M2}\sim t_{2,M2}\\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}\times\frac{n_2}{n_1}, & t_{2,M2}\sim t_{3,M2}\end{cases} \quad (17)$$

$$V_{N3}=\begin{cases}V_{C2}\times\frac{n_3}{n_2}, & t_{0,M2}\sim t_{2,M2}\\ -(V_{C2}-V_{in})\times\frac{L_{N1}}{L_{N1}+L_1}\times\frac{n_3}{n_1}, & t_{2,M2}\sim t_{3,M2}\end{cases} \quad (18)$$

$$V_{L1}=\begin{cases}-\left(V_{C2}\times\frac{n_1}{n_2}-Vin\right), & t_{0,M2}\sim t_{1,M2}\\ 0, & t_{1,M2}\sim t_{2,M2}\\ -(V_{C2}-V_{in})\times\frac{L_1}{L_{N1}+L_1}, & t_{2,M2}\sim t_{3,M2}.\end{cases} \quad (19)$$

IV. Design Considerations

A. Line Current and Duty Ratio

The line current $i_{\rm ac}$ is a low-frequency component of i_{N1} flowing through the low-pass filter L_r-C_r. Mathematically, the line current $i_{\rm ac}$ is the average current of i_{N1} within a switching cycle. Equation (4) demonstrates that the average current of i_{N1}, namely, $i_{\rm ac}$, varies slightly with $V_{\rm in}$ in both modes M_1 and M_4. Moreover, (11) demonstrates that the line current $i_{\rm ac}$ varies markedly with the line voltage $V_{\rm in}$ in both modes M_2 and M_3. Accordingly, the nonzero current $i_{N1}(t_{3,M2})$, that is, $i_{N1}(t_{0,M2})$, also varies with $V_{\rm in}$. Therefore, the resultant line current is produced, as illustrated in Fig. 5. Moreover, according to Fig. 6, the current i_{N1} is discontinuous in mode M_1 and M_2. Therefore, the current i_{N1} of the proposed converter operates in DCM.

In the control the duty ratio D approximates a constant in modes M_1 through M_4 since the inductor L_2 is large and operates in a continuous current mode. Additionally, the voltage V_{C2} is almost constant because of the use of a bulk capacitor C_2. Equation (1) shows the relationship between V_{C2} and duty ratio D.

B. Corner Angle of Line Current

Line current corner angle (CA) is defined as $\omega(t_1-t_o)$. Equation (3) demonstrates the relation between CA and parameters, duty ratio D, n_1/n_2, n_2/n_3, and V_o/V_m. Moreover, (1)–(3) demonstrate the relation of CA and V_o/V_m in different n_1/n_3 and duty ratio D. CA is larger in the high line voltage than the low line voltage given constant output power P_o. Furthermore, the CA also infects the power factor. Low CA is associated with high power factor.

C. Voltage Across Bulk Capacitor

V_{C2} denotes the voltage across bulk capacitor C_2. The influences on the voltage V_{C2} include n_1/n_2, duty ratio D, corner angle CA, input voltage $V_{\rm in}$, and output voltage V_o. The relation is illustrated in (20) and also demonstrates that V_{C2} increases slightly faster than the line voltage. Consequently, the corner angle produced in a high line voltage exceeds that produced in a low line voltage. Smaller CA is known to produce higher power factor and lower total harmonic distortion (THD). Furthermore, in practical applications V_{C2} should be below 450 V/dc with wide range input, 90 V$\sim$265 V/ac, and parameters, $n_1/n_2/n_3$ and D, also must meet the requirement (V_{C2} below 450 V/dc) to produce a given output V_o

$$\omega t_1 = Sin^{-1}\left[\frac{V_{C2}}{V_m}\left(1-\frac{V_o\times n_1}{V_{C2}\times n_3-V_o\times n_2}\right)\right]. \quad (20)$$

Fig. 4 illustrates that the bulk capacitor voltage V_{C2} can be determined as follows:

$$V_{C_2}=\frac{1}{C_2}\int_0^{T_l}-i_{C_2}\cdot dt$$

where $-i_{C_2}=i_{D_1}-i_{N_2}$, and T_l is a period of line voltage and

$$i_{D1}=\begin{cases}i_{N_1}, & t_{1,M1}<t<t_{2,M1}\\ i_{N_1}, & t_{2,M2}<t<t_{3,M2}\\ 0, & \text{else.}\end{cases}$$

The current i_{N1} is inversely proportion to (L_1+L_{N1}), as shown in (4) and (11). Therefore, V_{C2} is also inversely proportion to (L_1+L_{N1}). The value of V_{C2} thus decreases with increasing L_1.

D. Inductor L_1

Two reasons exist for using inductor L_1. The first reason is to reduce the high-frequency harmonics of i_{N1}, while the second is to reduce the voltage across capacitor C_2. Fig. 5 demonstrates that the slope of V_{C2} is zero at time t_1. The total charge transported by i_{N1} during the duty on period thus equals the total charge transported by i_{N2}. Thus, equating the integration of (4) and (5) gives

$$\int_{t_{1,M1}}^{t_{3,M1}} i_{N1}(\tau)d\tau=\int_{t_{0,M1}}^{t_{1,M1}} i_{N2}(\tau)d\tau.$$

The equation above can give the ratio of L_1/L_{N1}

$$\frac{L_1}{L_{N1}}=\frac{(V_{c2}\times n_3-V_o\times n_2)\times(n_2\times T_s)}{L_m\times n_1\times n_3\times\left(\frac{n_3}{n_2}\times 2I_o+T_s\times\frac{n_2\times V_o}{n_3\times L_m}\right)}-1 \quad (21)$$

or

$$L_1=\frac{V_{c2}\times T_s\times\left(1-\frac{V_o\times n_2}{V_{c2}\times n_3}\right)^2\times(V_{c2}-V_m Sin\omega t_1)}{2I_oV_o+V_o^2\times\frac{n_2^2\times T_s}{n_3^2\times L_m}}-L_{N1}. \quad (22)$$

E. Design Procedure

The circuit design methods, namely, the design of control loop and components voltage stress for the proposed converter, resembles the conventional forward converter. However, more design considerations must be performed in the proposed circuit for determining the reset winding and magnetic inductance. Therefore, the design method for transformer is shown as follows.

1) *Windings turns ratio* $n_1/n_2/n_3$*:* Based on (1) and (3), n_1/n_2 can be calculated via given $V_{m,\min}$, V_o, $D_{\max}$, $\omega t_{1,\min}$ and n_2/n_3,. $V_{m,\min}$ denotes the amplitude of

minimum line voltage. Additionally, V_o represents the typical output voltage. $D_{\max}$ is the maximum duty ratio, $0.4 \leqq D_{\max} \leqq 0.45$. The corner angle $\omega t_{1,\min}$, $0 < \omega t_{1,\min} \leq (\pi/4)$, is at $V_{m,\min}$. The turn ratio n_2/n_3 is recommended to be 2/1 in this prototype.

2) *Magnetic inductance L_m and L_{N1}:* Since magnetizing current i_{Lm} stores energy to charge bulk capacitor; Δi_{Lm} is recommended to be 20% of the primary load current

$$L_m = \frac{V_{C2} \times D_{\max} T_s}{\Delta i_{Lm}} \tag{23}$$

where $\Delta i_{Lm} \approx i_{N2}(t_{1,M1}) \times 20\%$.

The inductance L_{N1} can be simply obtained from (24)

$$\frac{L_{N1}}{L_m} = \left(\frac{n_1}{n_2}\right)^2 \tag{24}$$

where n_2 can be obtained by solving Faraday's law

$$n_2 = \frac{(V_{C2} \times D_{\max} T_s)}{(A_e dB)} \tag{25}$$

where A_e is the effective area of core and dB is flux density change in the transformer core.

3) *Series inductance L_1:* The inductance L_1 can be obtained from calculating (22).

V. Experiment Results

The proposed structure has been tested under the specifications of 85∼265-V/ac input voltage range, 50-V/dc output voltage, and 100-W output power. The turns ratio of $n_1/n_2/n_3$ is 27/23/12, and the inductance $L_1 \ll L_{N1}$, where $L_1 = 30\ \mu$H and transformer core PQ32/20 is used. The transformer core used in the previous similar converter should be EER35 in [4] and [6]. Although numerous previous similar converters have a similar transformer core size to the proposed converter in given similar output power and switching frequency, the boost inductors sizes, 58 uH∼240 μH in [4] or 1.4 mH in [6], are several times greater than that of L_1 in the proposed converter. The sizes of the boost inductors employed in [4] and [6] are thus several greater than those of L_1 when flowing through a similar line current. Fig. 9 illustrates the line current in a full line cycle. Experiments have verified that the harmonic distribution complies with the standard IEC 61000-3-2. Table I demonstrates that the detailed harmonic distribution of the prototype design meets the requirements of class D.

Fig. 10 illustrates dynamic response switching between a half and a full load under 110-V/ac input voltage. The output voltage of the prototype displays a fast response and stable regulation. Moreover, Fig. 11 illustrates the voltages across the bulk capacitor for different input voltages under a full load. The voltage of the bulk capacitor depends on $V_{\rm ac}$ and turn-ratio n_1/n_3 but it is almost independent of load current. The maximum voltage can be held below 450 V/dc, a popular commercial voltage in the market for electrolytic capacitors, by adjusting turns ratio n_1/n_3.

Table II displays the voltage stress in S_1, voltage across bulk capacitor C_2, and efficiency η. The voltage stress in S_1 exceeds

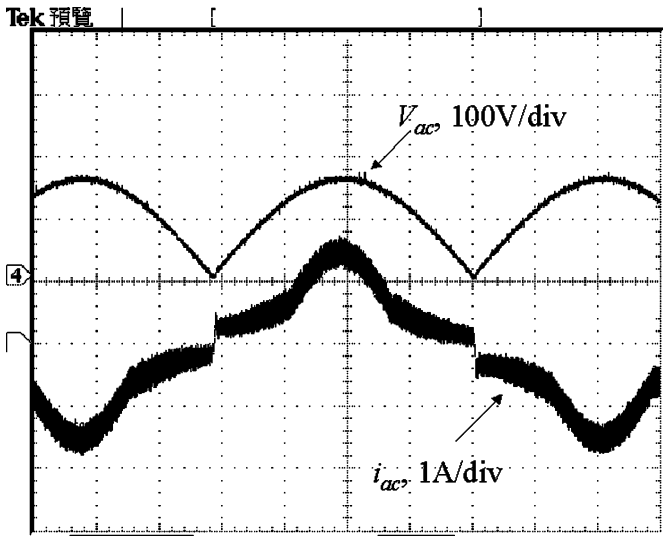
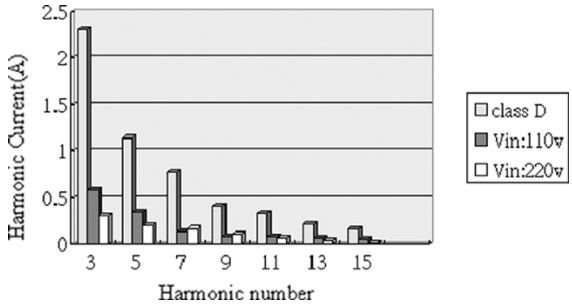


Fig. 9. $i_{\rm ac}$ and $V_{\rm ac}$ waveforms at $V_{\rm ac} = 110$ V, $I_o = 1.5$ A.

TABLE I
HARMONIC MAIN CONTENTS OF THE LINE CURRENT $i_{\rm ac}$



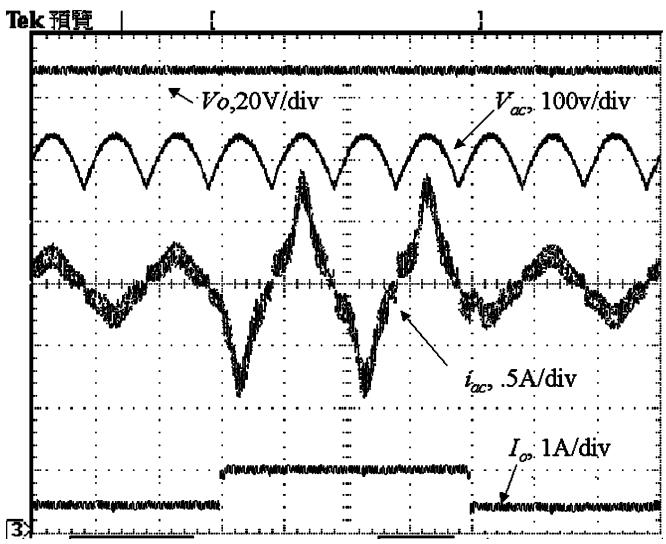


Fig. 10. Dynamic response waveforms for $V_{\rm ac}$, $i_{\rm ac}$, V_o, and I_o when $V_{\rm ac} = 110$ V, $V_o = 50$ V and $I_o = 0.5$ A/1 A.

500 V when input voltage $V_{\rm in}$ surpasses 130 V. Therefore, an extended type forward converter with two switches [10] can be considered as a solution if the user wants to reduce the voltage stress in S_1. The efficiency is penalized due to a part of the power processed twice. Moreover, it operates in DCM at the current i_{N1} so the efficiency is slightly decreased.

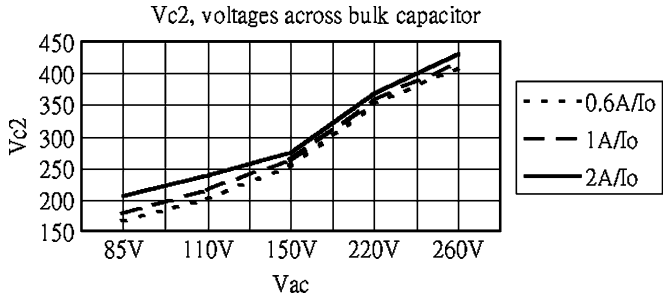


Fig. 11. Voltage stress of bulk capacitor V_{C2} and line voltage $V_{\rm ac}$.

TABLE II
VOLTAGE STRESS OF S_1, VOLTAGE ACROSS BULK CAPACITOR C_2 AND EFFICIENCY η

$V_{\rm in}$ [V]	$V_{\rm S1}$ [V]	$V_{\rm B}$ [V]	η [%]
90	442	221	74.5
110	481	241	75
130	515	258	75.4
220	742	371	76
230	781	389	76.5
260	849	425	76.1

VI. CONCLUSION

This paper has proposed a new ac/dc converter structure. The proposed converter has harmonic current correction and fast output voltage regulation. The proposed converter is implemented with a single-switch–single-stage topology and single control loop and, thus, is simple. Synchronously, the structure markedly reduces the volume and weight of magnetic material compared to the conventional S^4IP^2 converters by employing reset winding in transformer. The reset winding N_1 replaces the bulk inductor used in boost-based S^4IP^2 converters. The line current of the proposed converter complies with standard IEC 61000-3-2 and the voltage is tightly regulated under load change, as experimentally verified. The voltage across bulk capacitor can be held below 450 V by adjusting the turns ratio n_1/n_3 in full range input (85∼265 V/ac). The proposed structure also can be extended to other types of converters.

However, this new converter bears a high voltage stress in S_1 and a penalized efficiency because a part of the power is processed twice. Alternatively, an extended type forward converter with two switches can reduce the high voltage stress. The proposed converter can operate in CCM at line current by increasing the inductance L_1. Moreover, the efficiency can be improved in CCM operation.

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